Reference Schematics For RK3528

RK3528_BOX_REF_SCH_V10

Main Functions Introduction

1) Power: DiscretePower:BUCK+LDO or PMIC RK805-6
2) RAM: DDR3 4x16bit
   DDR4 2x16Bit
   DDR4 4x16Bit
   LPDDR3 1x32bit
   LPDDR4/LPDDR4X 1x32bit
3) ROM: eMMC5.1 or FSPI Flash
4) Support: Micro SD Card3.0
5) Support: 1 x USB3.0 OTG + 1 x USB2.0 HOST
6) Support: 1 x HDMI2.0 TX
7) Support: 1 x AV OUT
8) Support: SDIO WiFi5 + UART/PCM BT
   PCIE WIFI5 + UART/PCM BT
9) Support: 1 x Ethernet(Embed PHY) + 1x Ethernet(RGMII or RMII)
10) Support: Optical S/PDIF TX
11) Support: IR Receiver
12) Support: Audio-MicArray 2xI2S-DMIC or 4xPDM-DMIC
13) Support: RECOVER/RESET/SARADC_BOOT_KEY,HW_ID
14) Support: 1 x PCIE2.0 Slot
15) Support: Debug UART

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	00.Cover Page				
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Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip	Rockchip Electronics Co., Ltd				
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File:	01.Index and Notes				
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Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2023-05-25	HXS	1:Revision preliminary version	

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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	02.Revision History				
Date:	Friday, May 26, 2023			Rev:	V1.0
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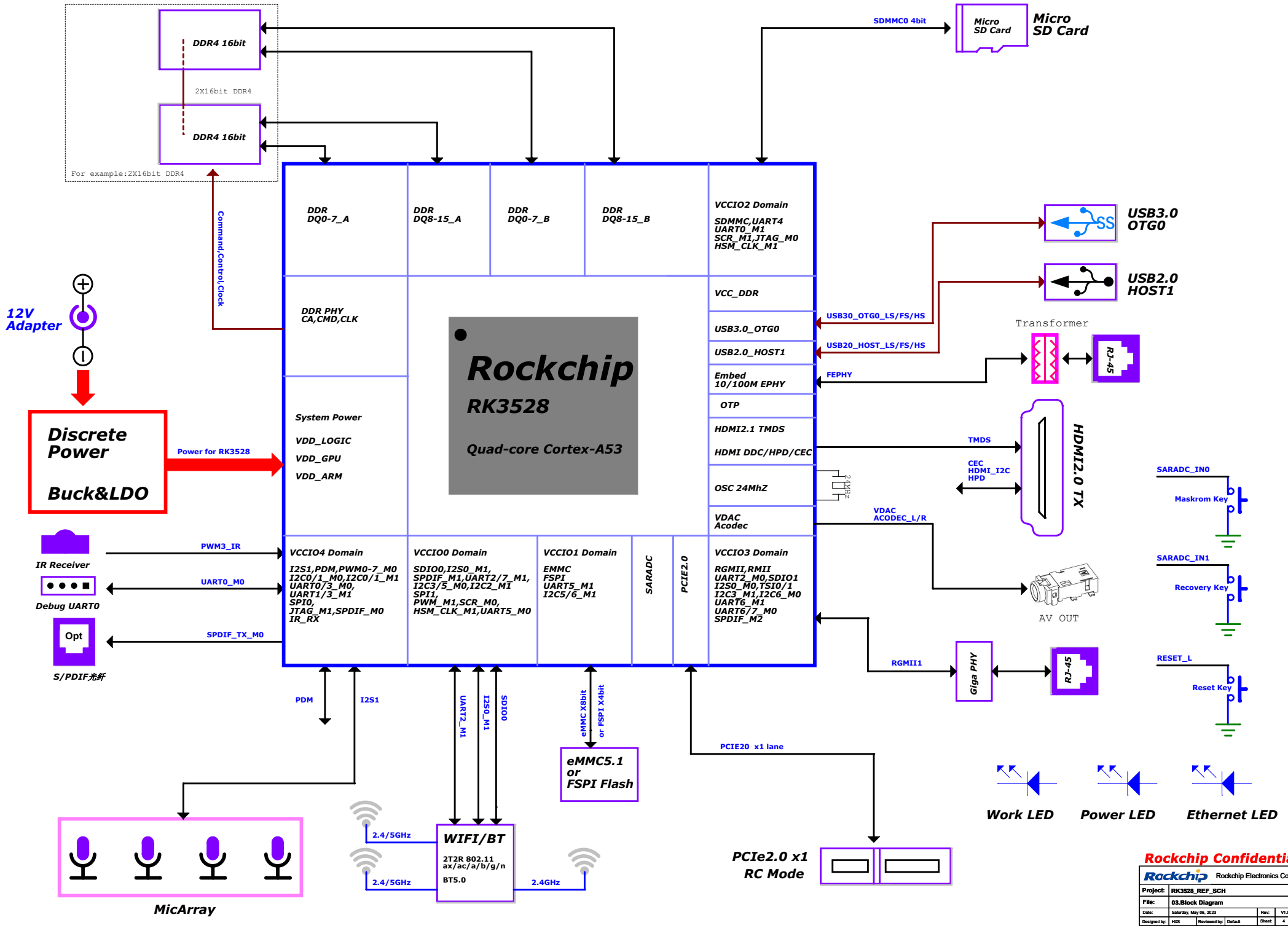
RK3528 Block Diagram



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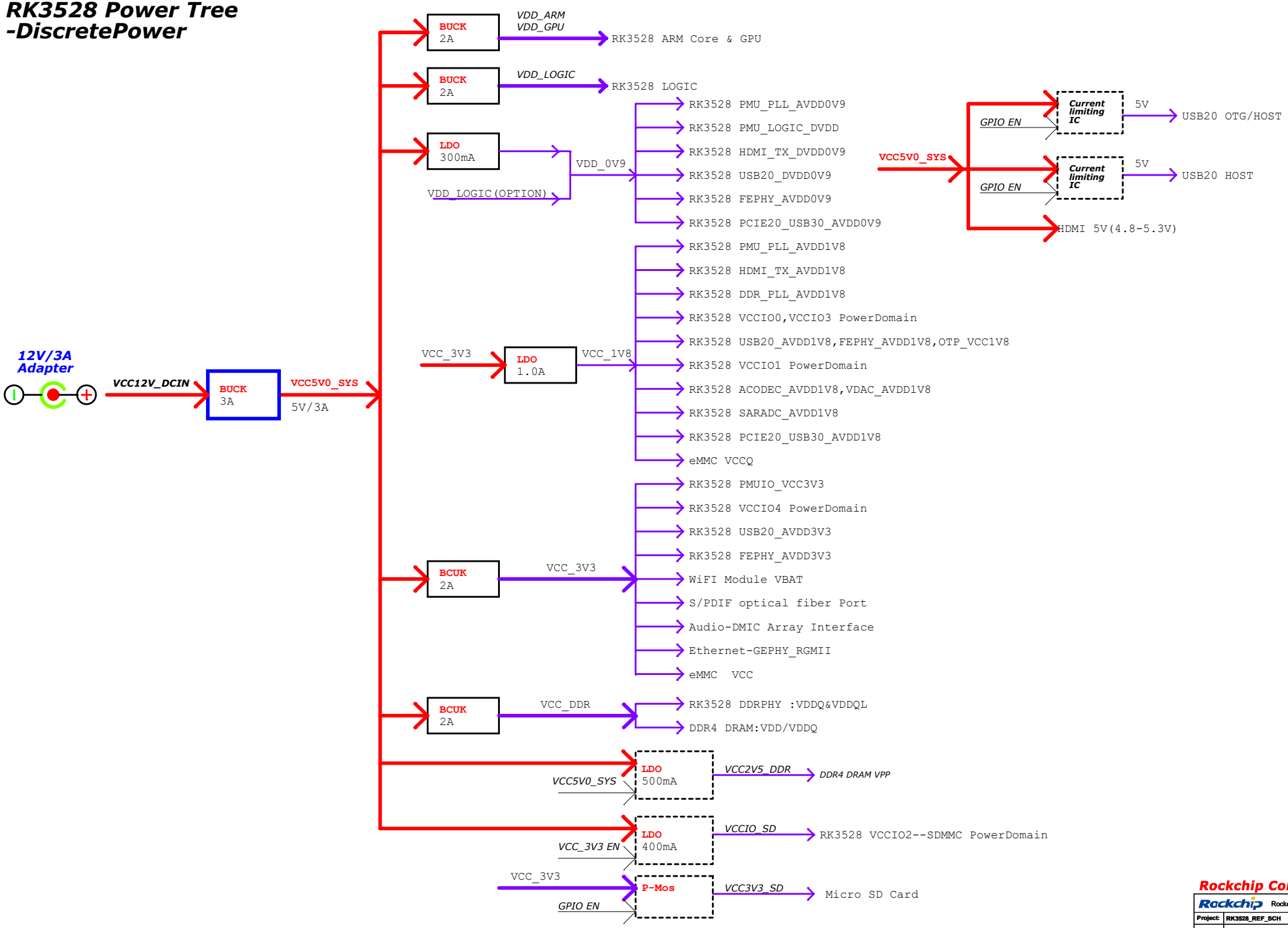
RK3528 Power Tree -DiscretePower



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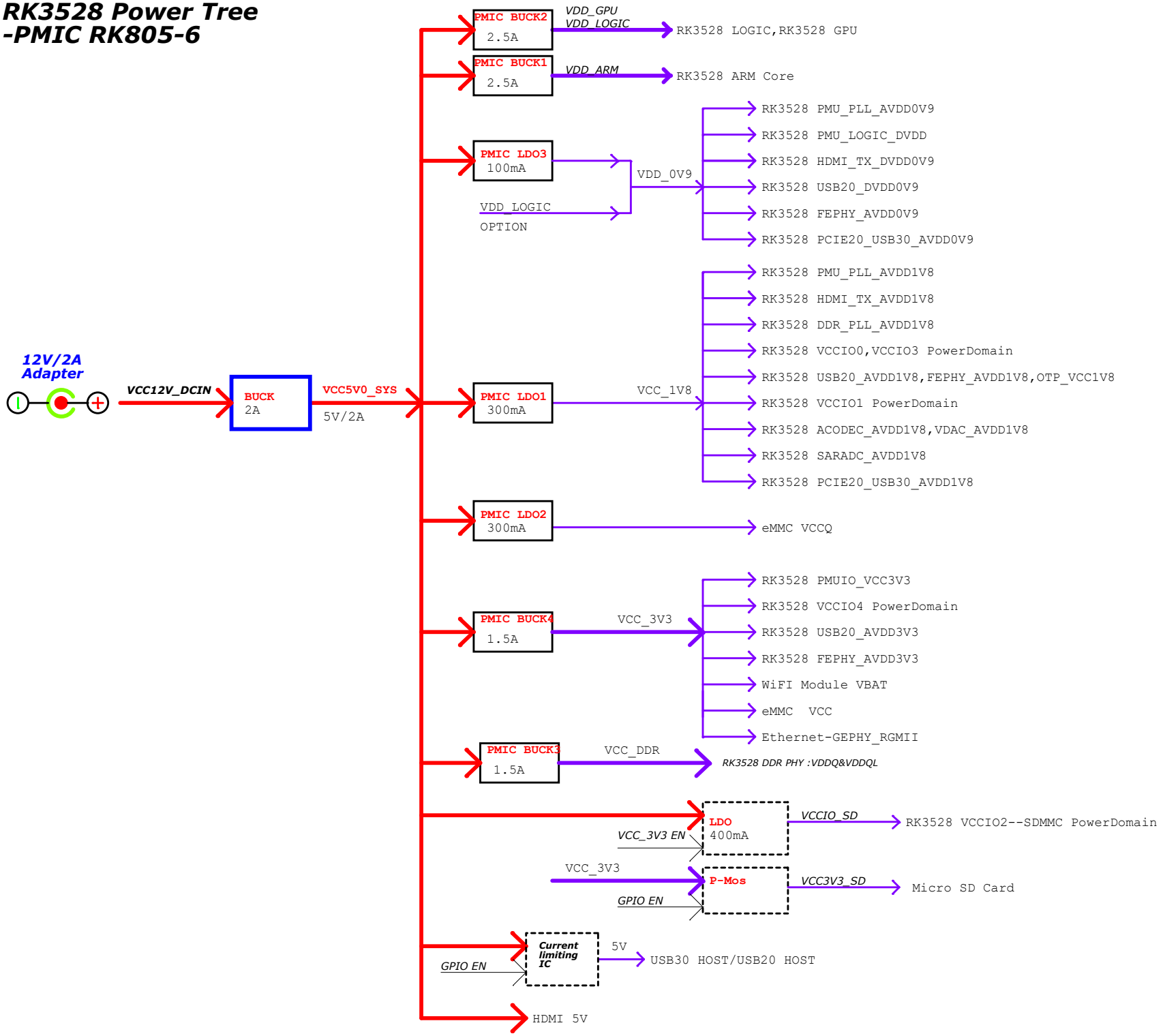
RK3528 Power Tree -PMIC RK805-6



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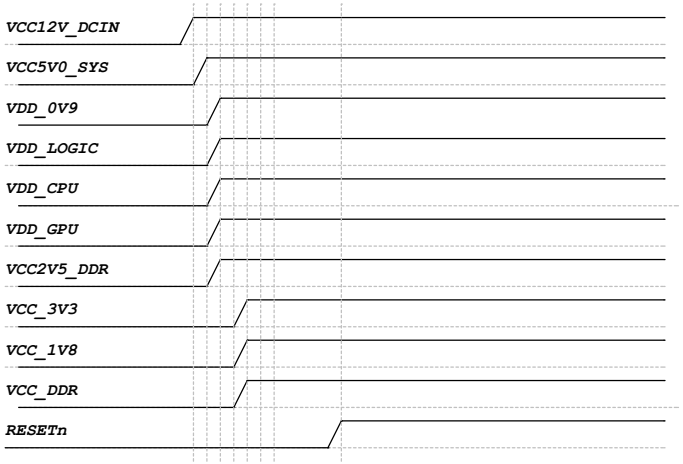
DiscretePower Power Sequence



Power Supply	EXT BUCK&LDO	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	BUCK1	2.0A	VDD_LOGIC VDD_GPU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK2	2.0A	VDD_ARM	Slot:1	0.95V	ON	ON	TBD	TBD
VCC5V0_SYS	LDO1	0.3A	VDD_0V9	Slot:1	0.9V	ON	ON	TBD	TBD
VCC_3V3	LDO2	1.0A	VCC_1V8	Slot:2	1.8V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK3	2.0A	VCC_3V3	Slot:2	3.3V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK4	2.0A	VCC_DDR	Slot:2	ADJ FB=0.6V	ON	ON	TBD	TBD
VCC12V_DCIN	BUCK5	3.0A	VCC5V0_SYS	Slot:0	5.2V	ON	ON	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO	Pin 1J13	✓	✗	VCCIO_PMU	VCC_3V3	3.3V	
VCCIO0	Pin 1N6	✓	✓	VCCIO0	VCCIO_WL	1.8V	
VCCIO1	Pin 1P8	✓	✓	VCCIO1	VCCIO_FLASH	1.8V/3.3V	Select as required
VCCIO2	Pin 1B14	✓	✓	VCCIO2	VCCIO_SD	1.8V/3.3V	SD3.0 Voltage=1.8V SD2.0 Voltage=3.3V 3.3V-->1.8V
VCCIO3	Pin 1M13	✓	✓	VCCIO3	VCC_1V8 VCC_3V3	1.8V 3.3V	Select as required
VCCIO4	Pin 1J3	✓	✓	VCCIO4	VCC_3V3	3.3V	

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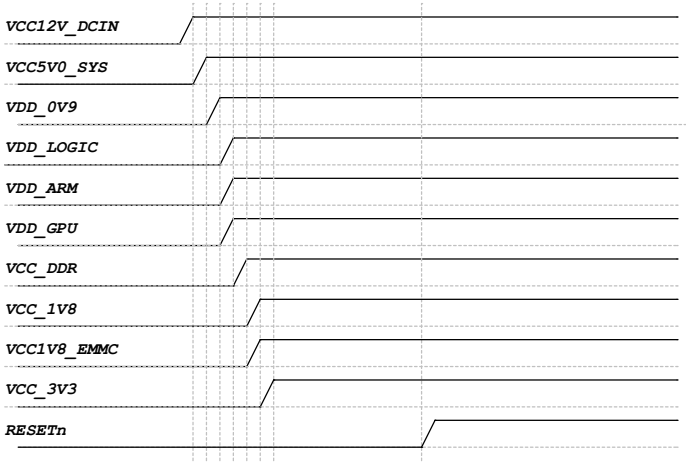
RK805-6 Power Sequence



Power Supply	EXT BUCK&LDO	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	PMIC LDO3	0.1A	VDD_0V9	Slot:1	0.9V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC BUCK2	2.5A	VDD_LOGIC VDD_GPU	Slot:2	0.9V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC BUCK1	2.5A	VDD_ARM	Slot:2	0.9V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.6V	ON	ON	TBD	TBD
VCC_3V3	PMIC LDO1	0.3A	VCC_1V8	Slot:4	1.8V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC LDO2	0.3A	VCC1V8_EMMC	Slot:4	1.8V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC BUCK4	1.5A	VCC_3V3	Slot:5	3.3V	ON	ON	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.2V	ON	ON	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO	Pin 1J13	✓	✗	VCCIO_PMU	VCC_3V3	3.3V	
VCCIO0	Pin 1N6	✓	✓	VCCIO0	VCCIO_WL	1.8V	
VCCIO1	Pin 1P8	✓	✓	VCCIO1	VCCIO_FLASH	1.8V/3.3V	Select as required
VCCIO2	Pin 1B14	✓	✓	VCCIO2	VCCIO_SD	1.8V/3.3V	SD3.0 Voltage=1.8V SD2.0 Voltage=3.3V 3.3V-->1.8V
VCCIO3	Pin 1M13	✓	✓	VCCIO3	VCC_1V8	1.8V 3.3V	Select as required
VCCIO4	Pin 1J3	✓	✓	VCCIO4	VCC_3V3	3.3V	

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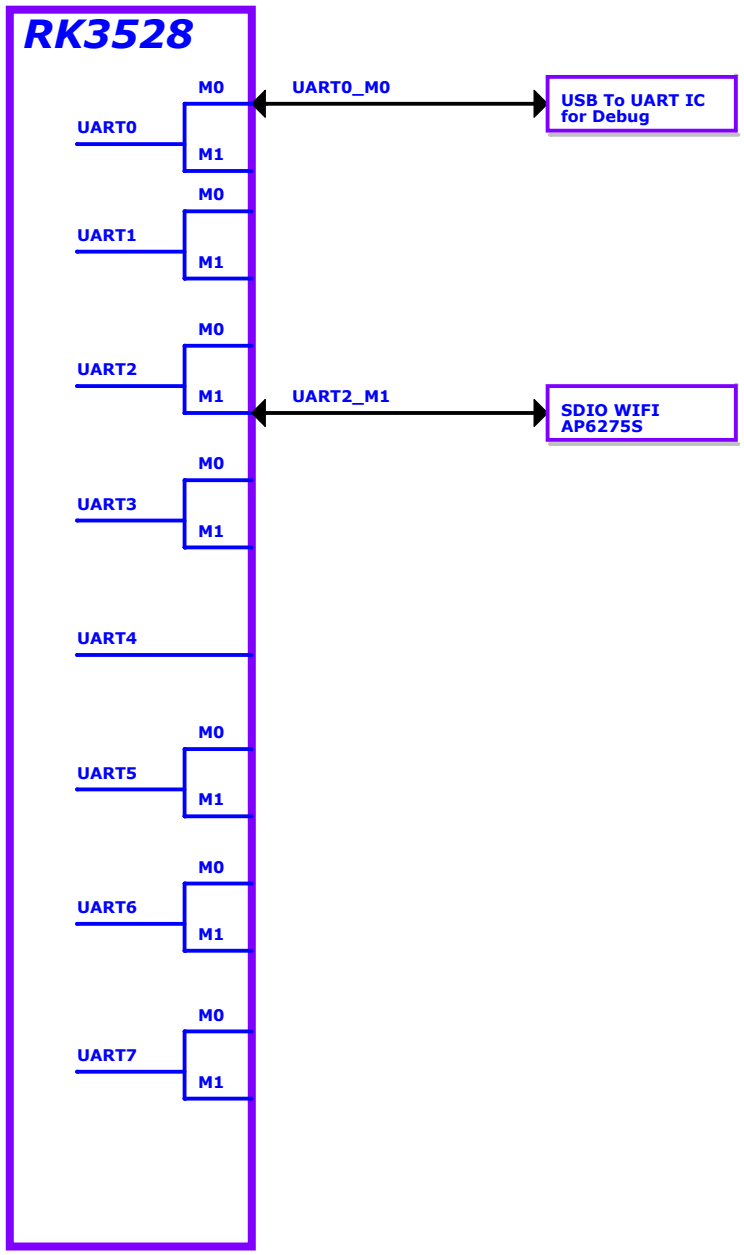
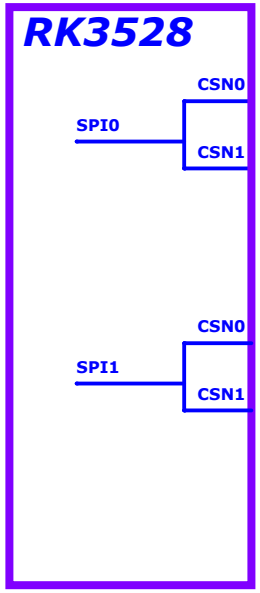
UART MAP

RK3528



SPI MAP

RK3528



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File:	06.UART Map				
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I2C MAP

RK3528

I2C0 — M0 / M1

I2C1 — M0 / M1

I2C2 — M1

I2C3 — M0 / M1

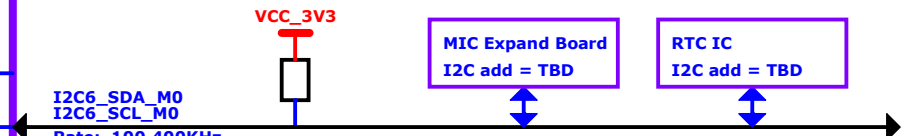
I2C4

I2C5 — M0 / M1

I2C6 — M0 / M1

I2C7

I2C_HDMI



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File:	07.I2C Bus Map				
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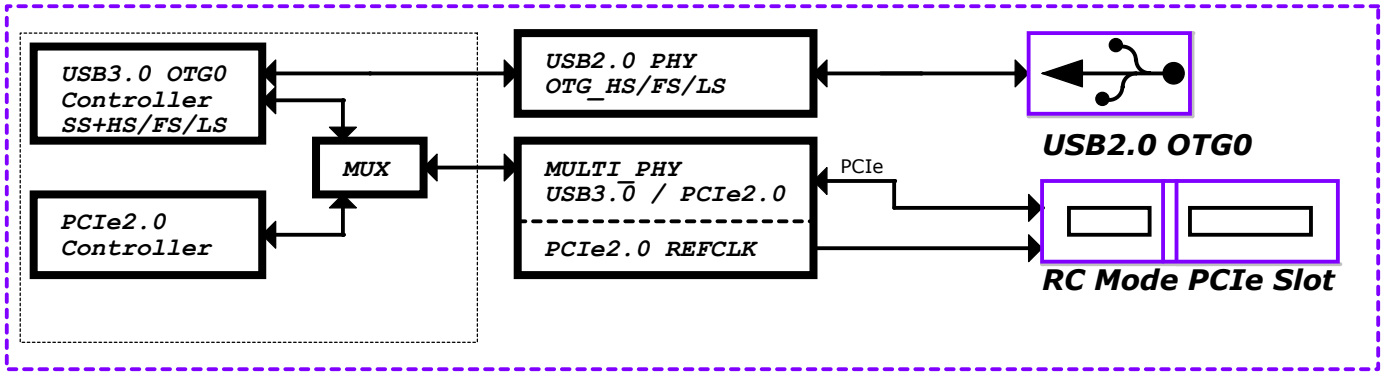
USB3/PCIE Fun Map

Case1: USB2.0 OTG0 + PCIe2.0 x1 Lane



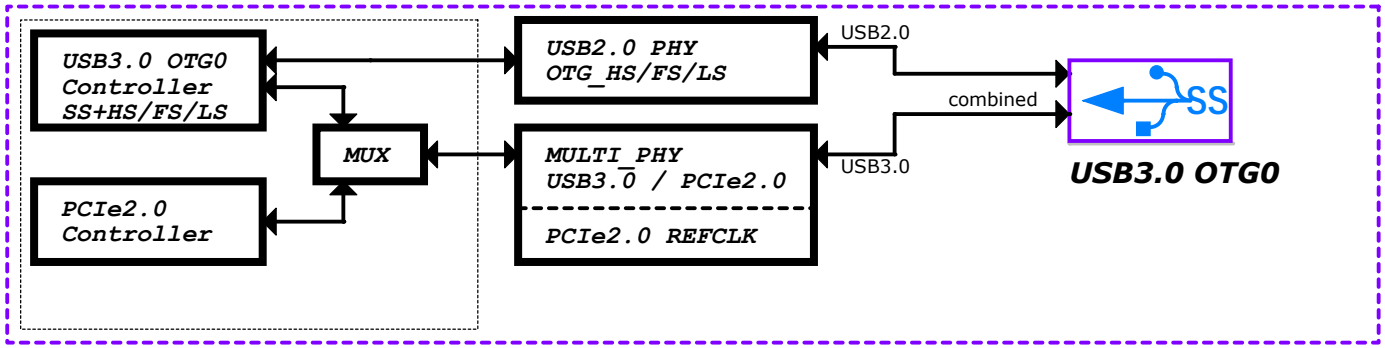
Note 1:

USB3.0 OTG is backward compatible with USB2.0, it needs to occupy the USB2.0 OTG signal pair.

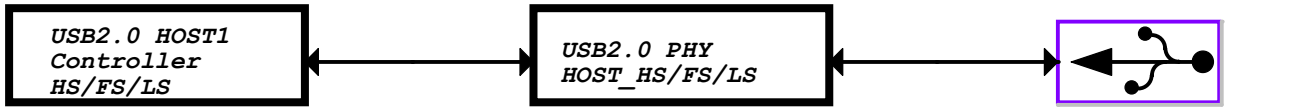
Note 2:

MULTI PHY can be configured for PCIe2.0 or USB3.0 interface.
PCIe2.0 only work in RC mode, and support both internal/external clock.

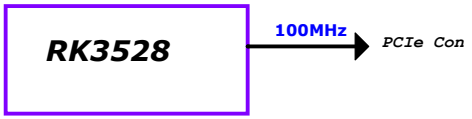
Case2: USB3.0 OTG0



USB2.0 HOST1



PCIe2.0 REFCLK



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
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Date:	Sunday, May 07, 2023			Rev:	V1.0
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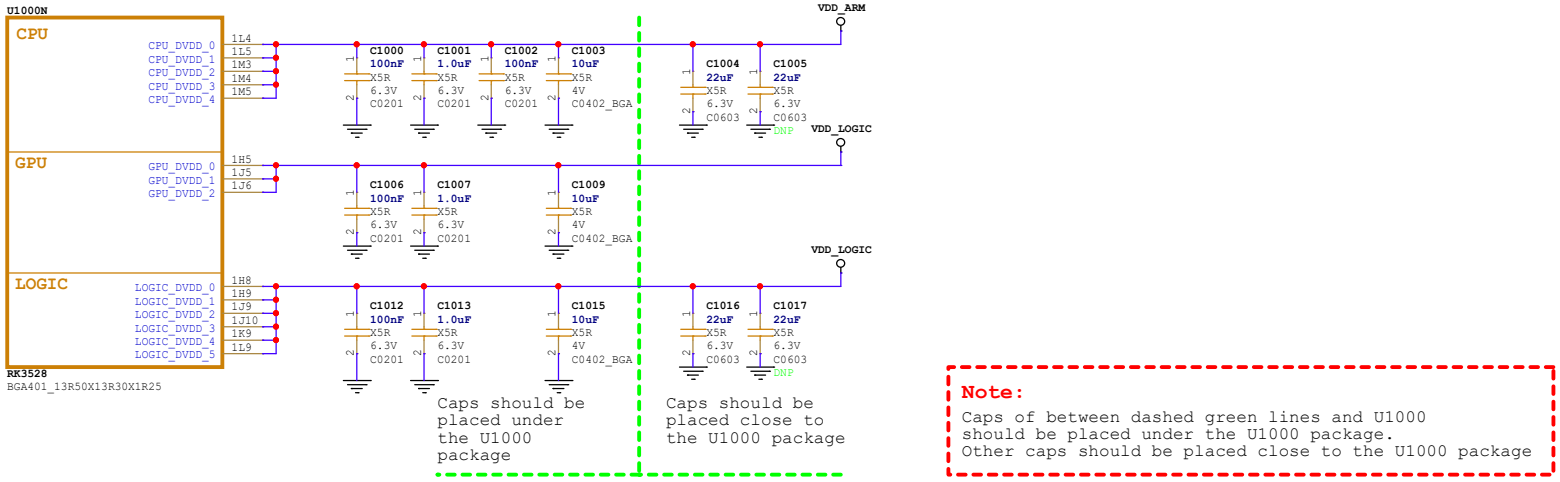
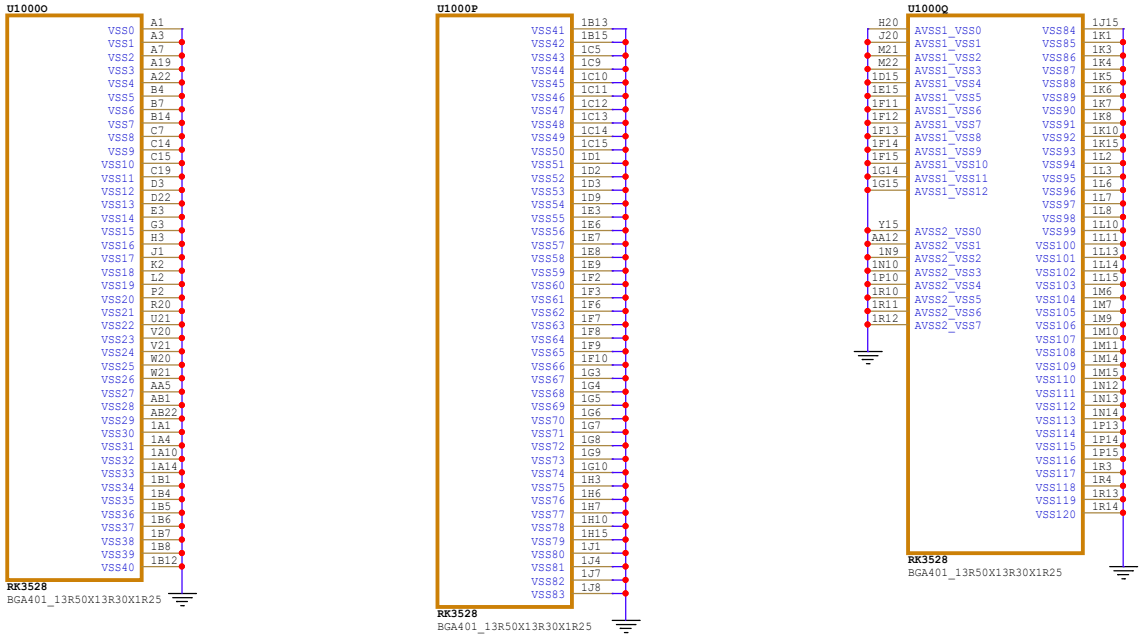
RK3528_N(POWER)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_O/P/Q(GND)



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Project:	RK3528_REF_SCH				
File:	10.RK3528 Power/GND				
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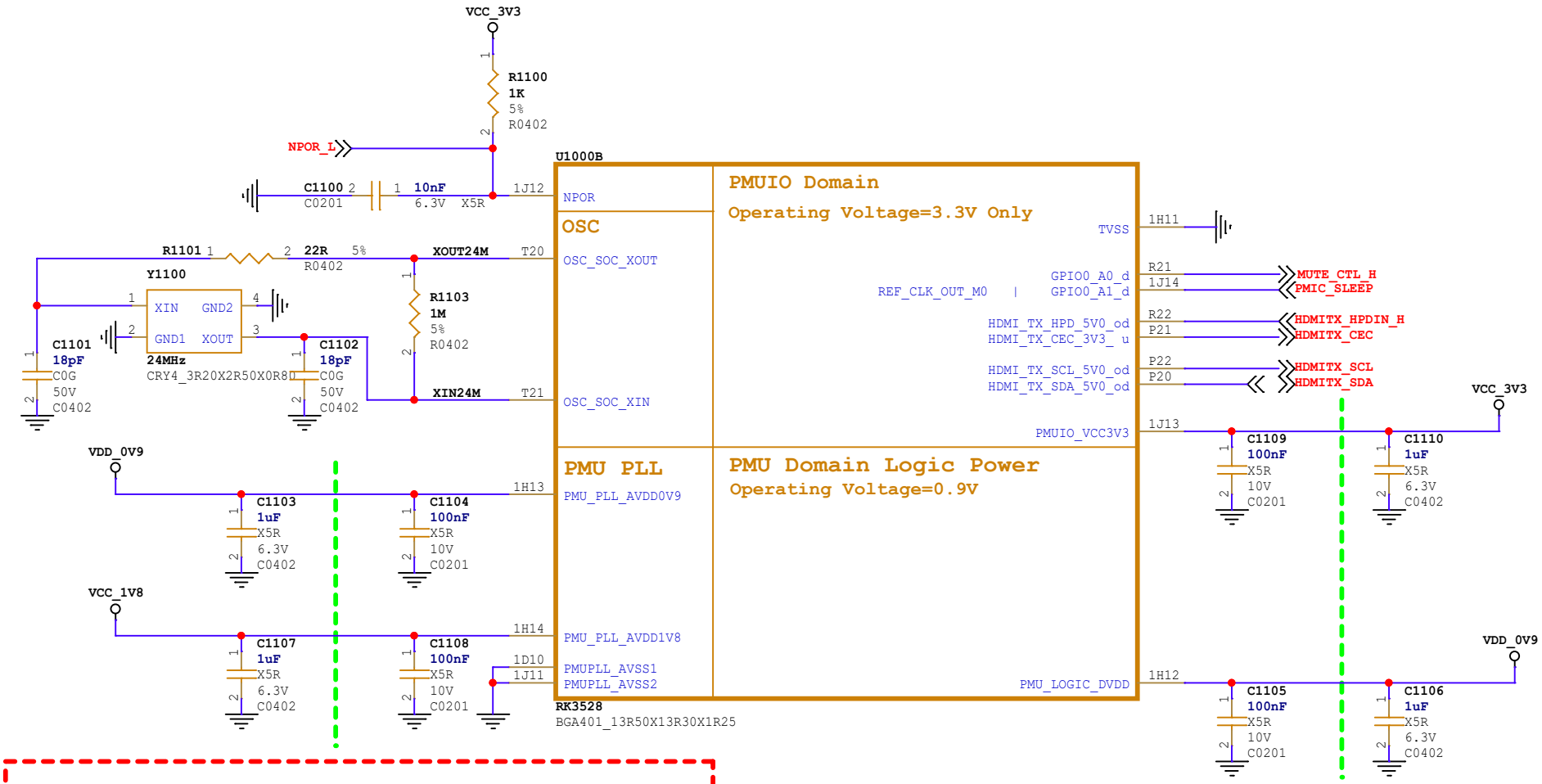
RK3528_B(OSC/PLL/PMUIO Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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Project:	RK3528_REF_SCH				
File:	11.RK3528 OSC/PLL/PMUIO				
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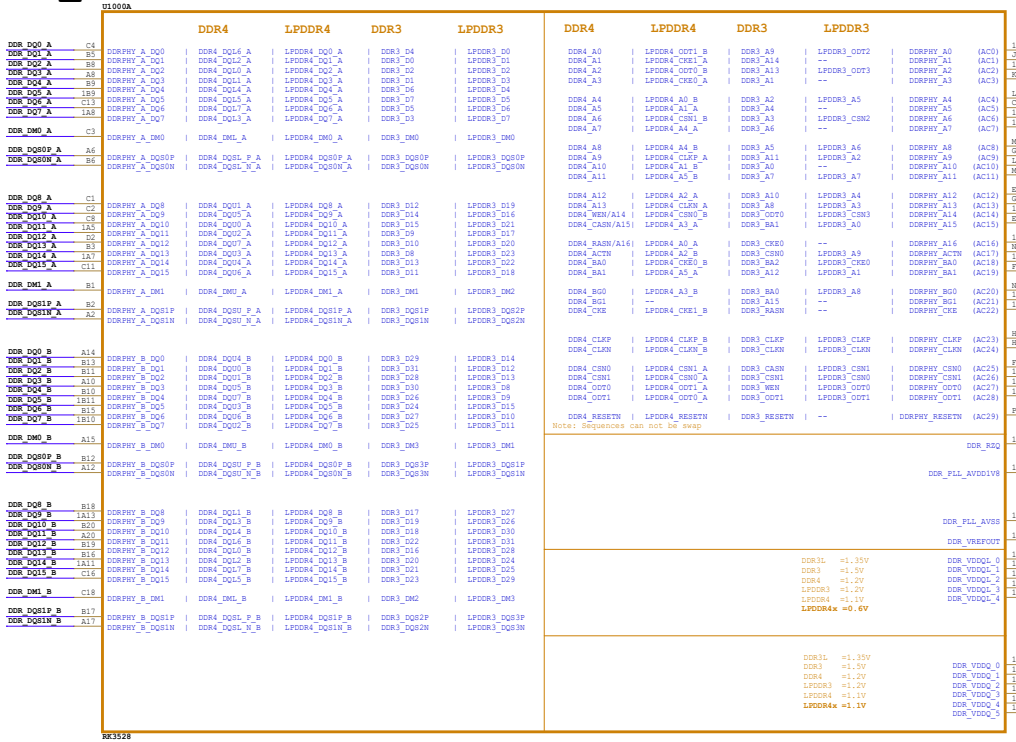
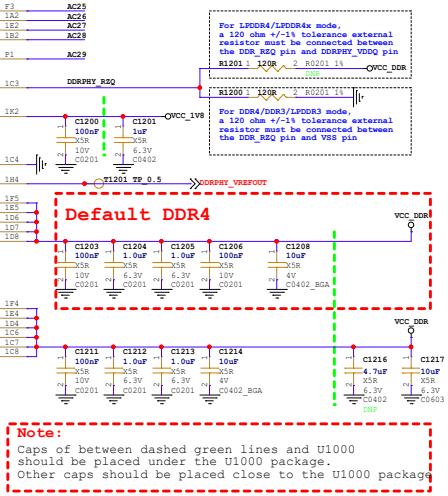
RK3528_A(DDR PHY)





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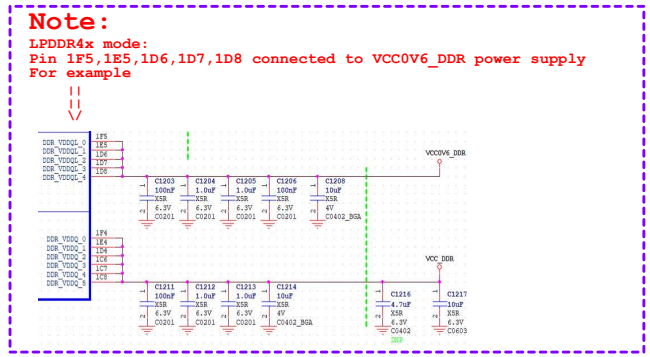
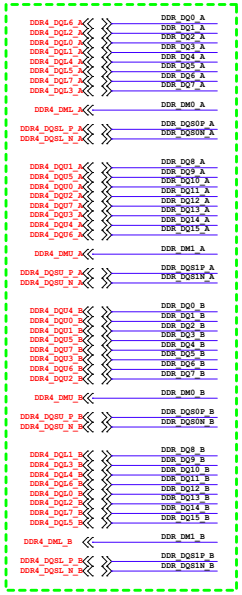
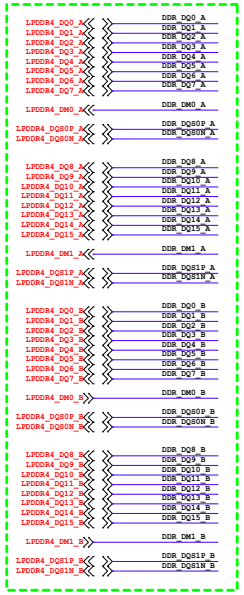


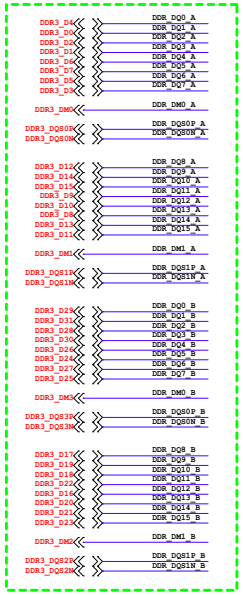
Default DDR4 DQ



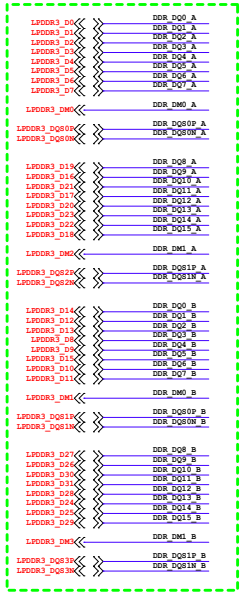
LPDDR4/4x DQ



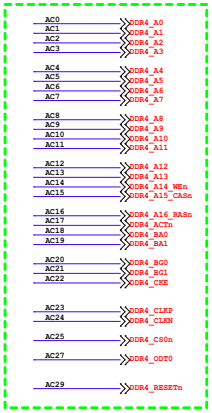
DDR3 DQ



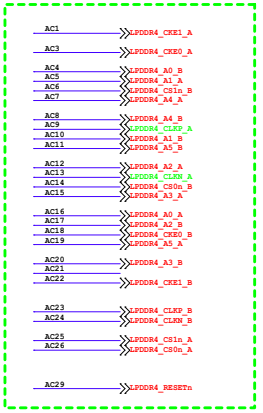
LPDDR3 DQ



Default DDR4 AC



LPDDR4/4x AC



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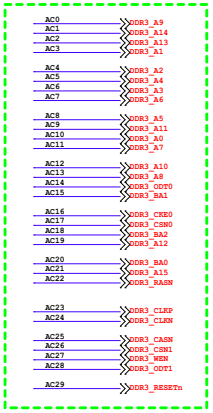
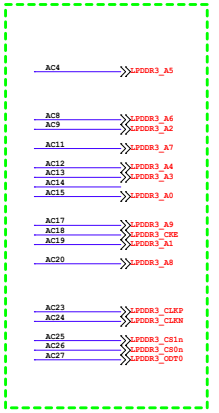


LPDDR3 AC



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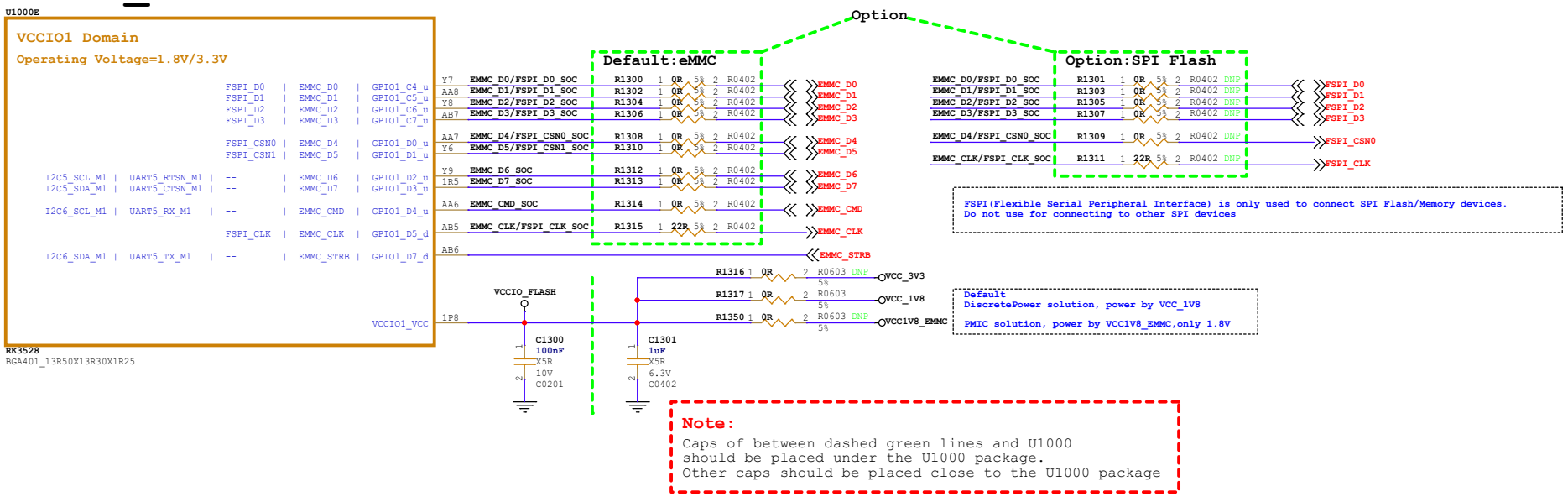
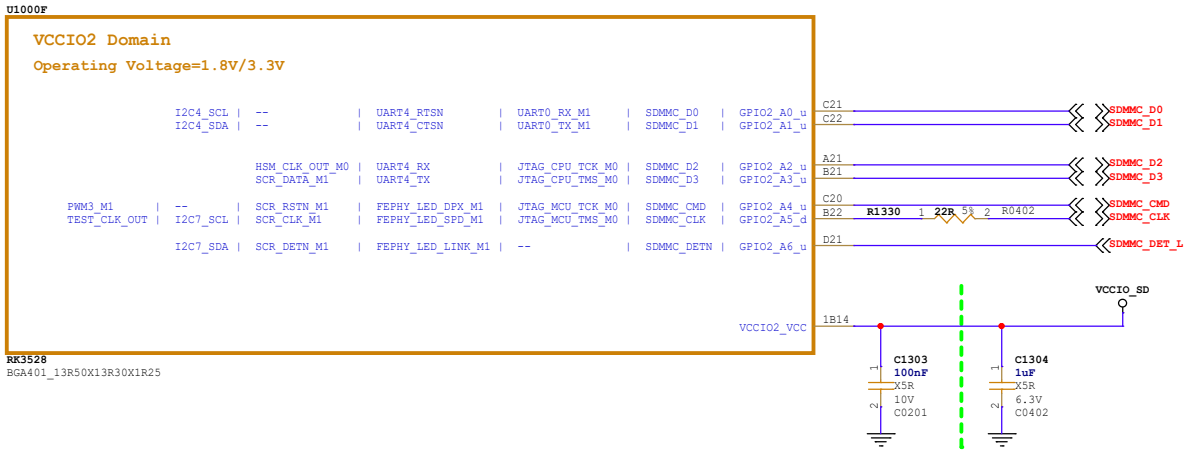
RK3528_E(VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_F(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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Project:	RK3528_REF_SCH		
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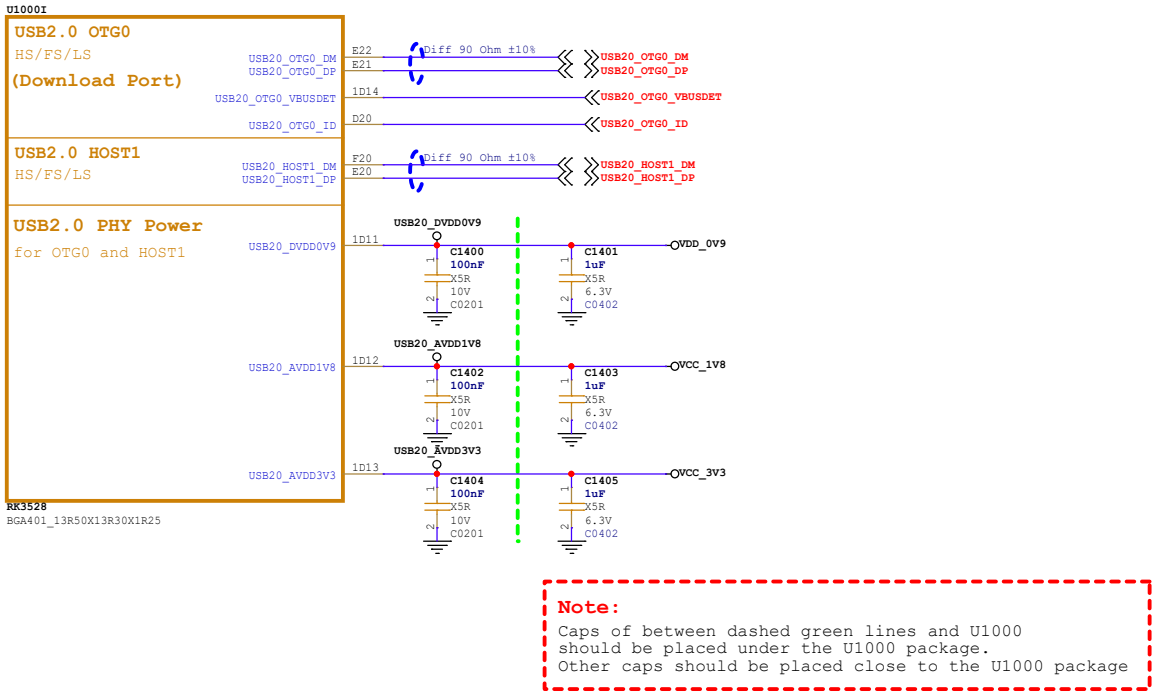
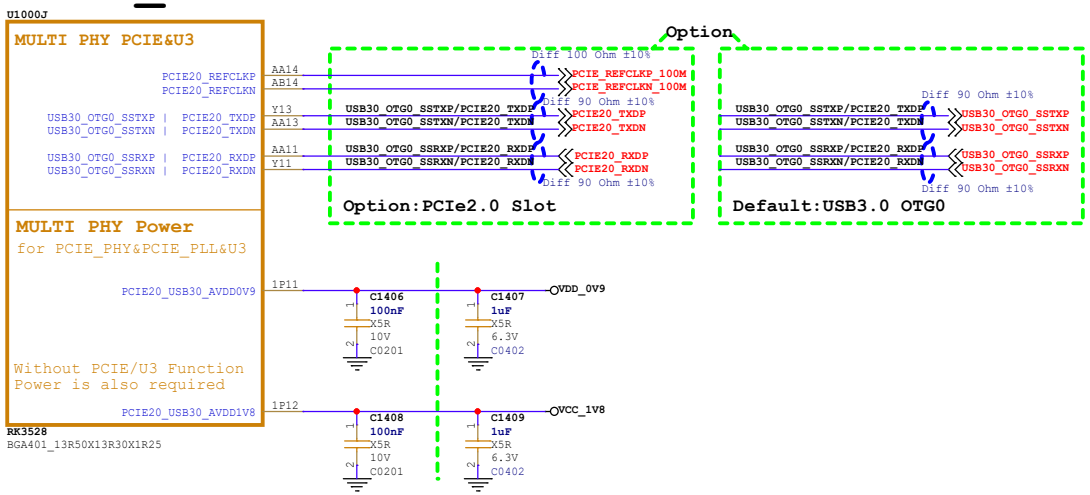
RK3528_I(USB2.0 OTG/HOST)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_J(PCIE2.0/U3 PHY)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
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Project:	RK3528_REF_SCH				
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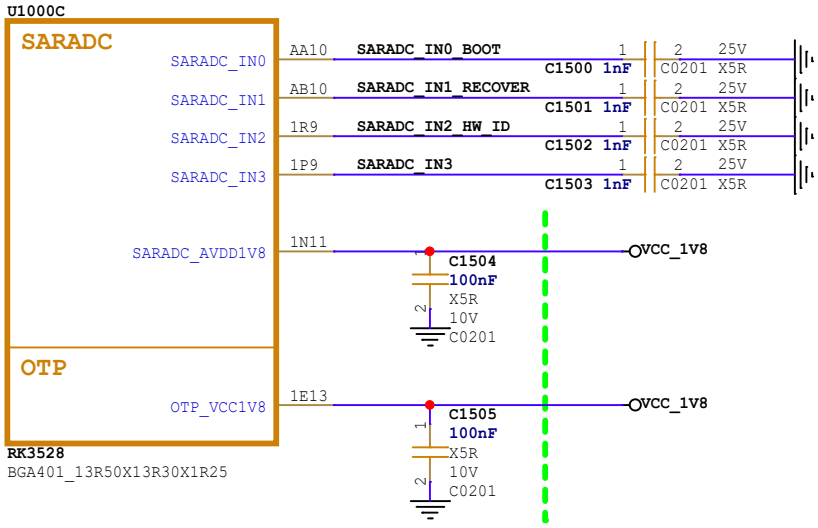
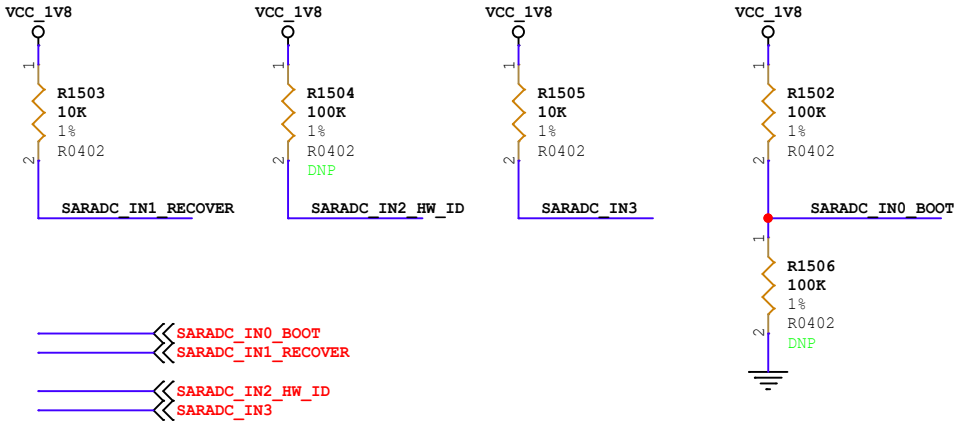
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	16 of 50

RK3528_C(Saradc/OTP)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



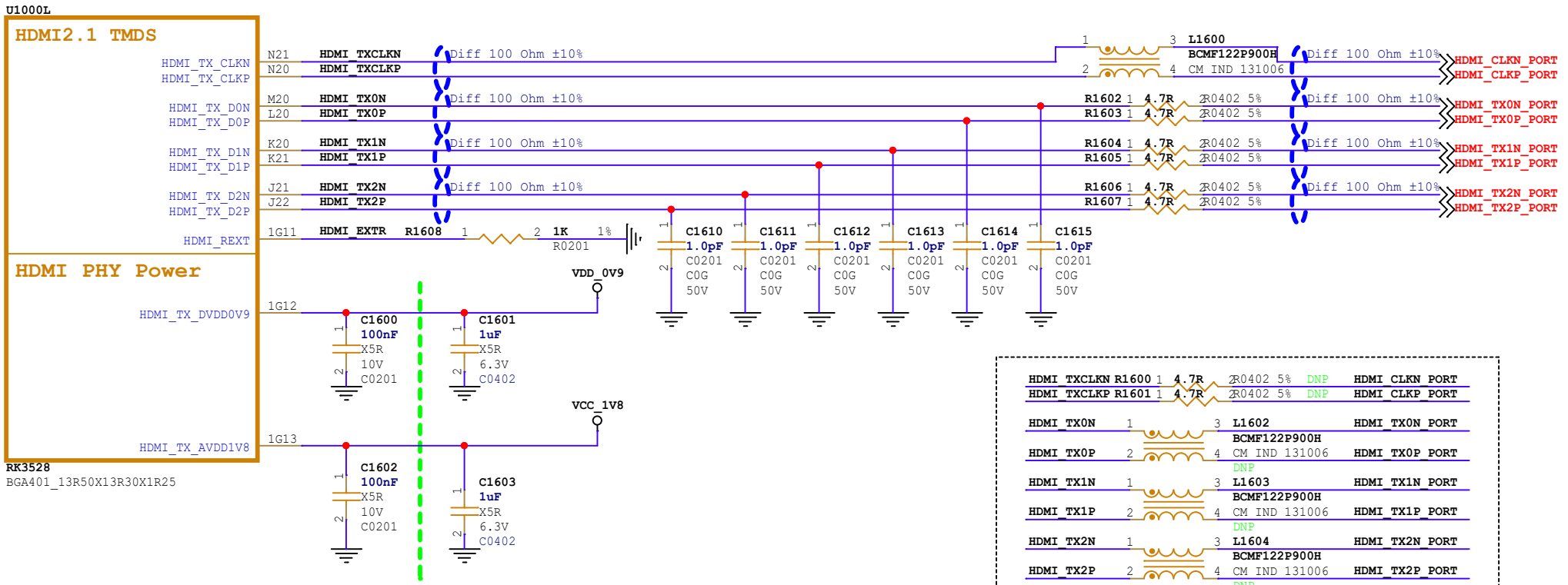
TABLE

Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	12K	114	
LEVEL3	100K	27K	228	FSPI--USB
LEVEL4	100K	51K	342	
LEVEL5	100K	82K	456	
LEVEL6	100K	120K	570	EMMC--USB
LEVEL7	100K	200K	683	EMMC--SD Card--USB
LEVEL8	100K	330K	796	SD Card--USB
LEVEL9	100K	820K	910	
LEVEL10	100K	DNP	1023	FSPI--EMMC--SD Card--USB

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	15.RK3528 SARADC/OTP				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	17 of 50

RK3528_L(HDMI PHY)

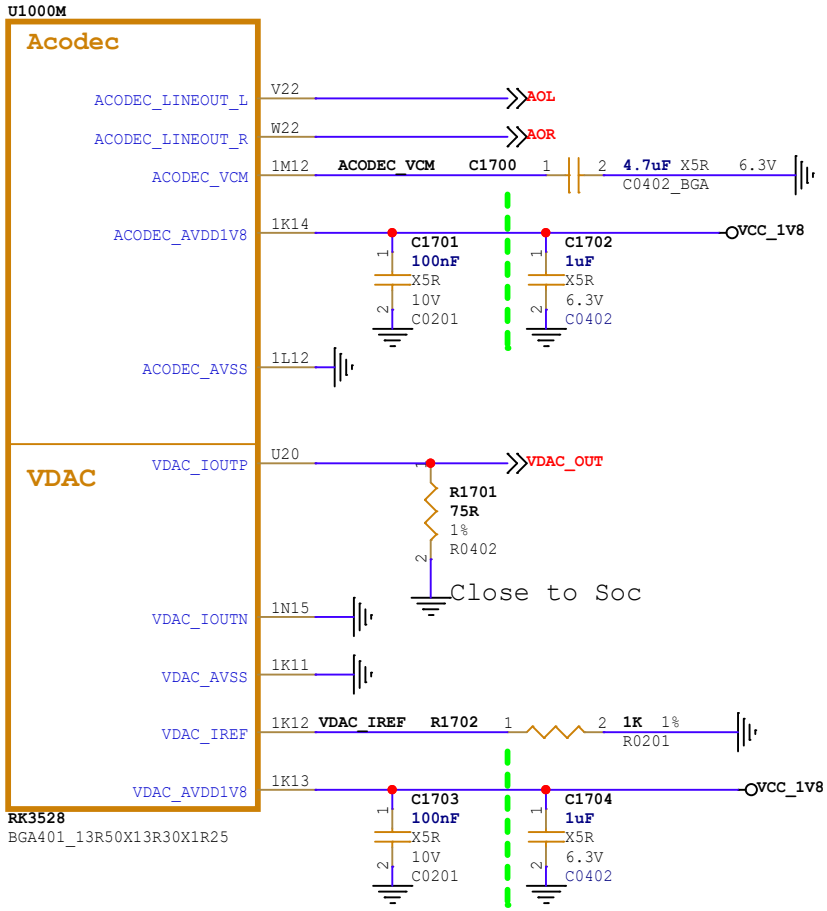


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	16.RK3528 HDMI Interface				
Date:	Saturday, May 27, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	18 of 50

RK3528_M(Acodec/VDAC)



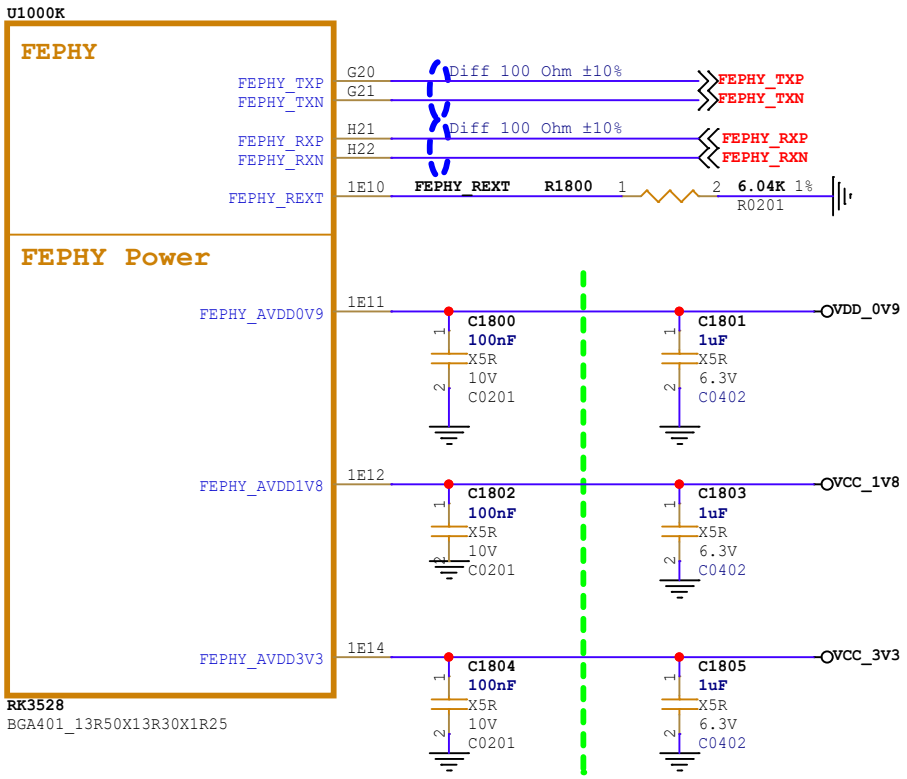
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	17.RK3528 AV OUT				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	19 of 50

RK3528_K(Embed FEPHY)



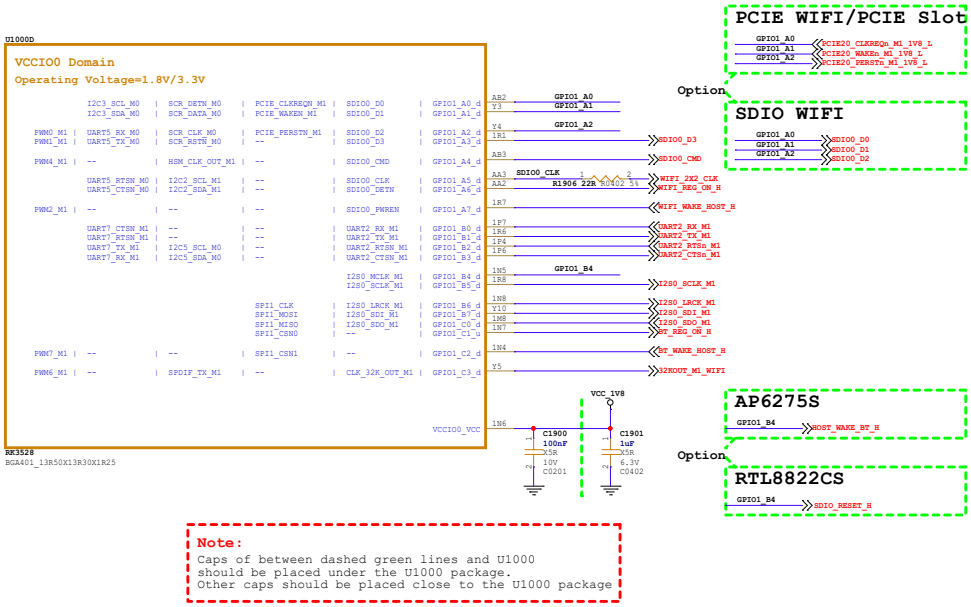
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

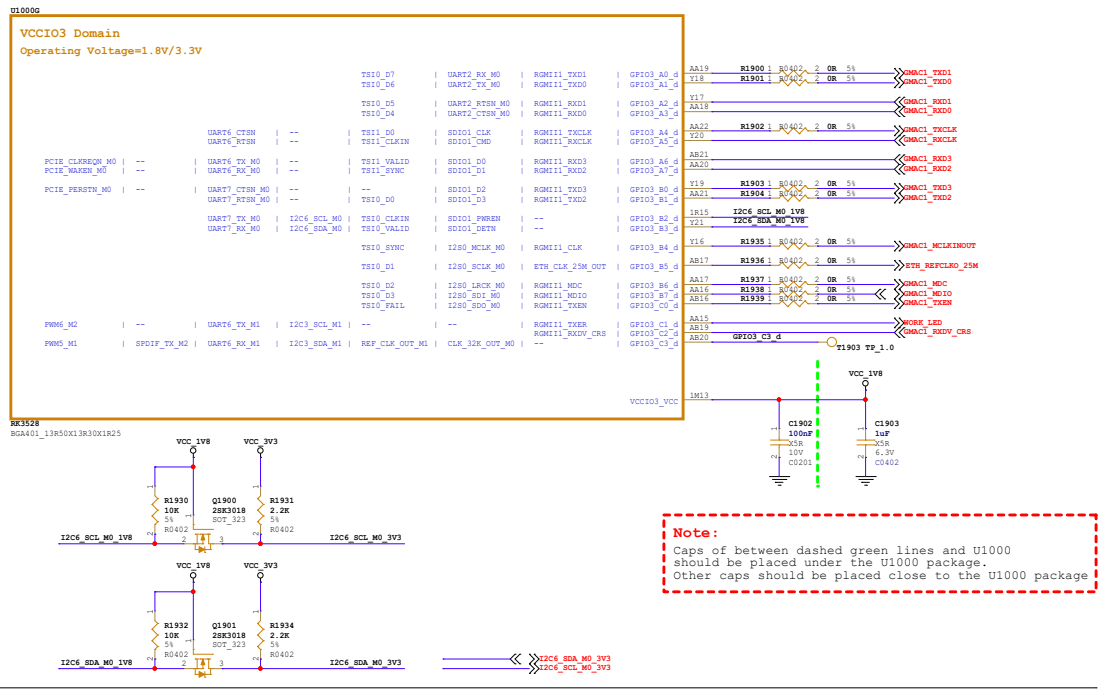
Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	18.RK3528 Embed FEPHY				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	20 of 50

RK3528_D(VCCIO0 Domain)



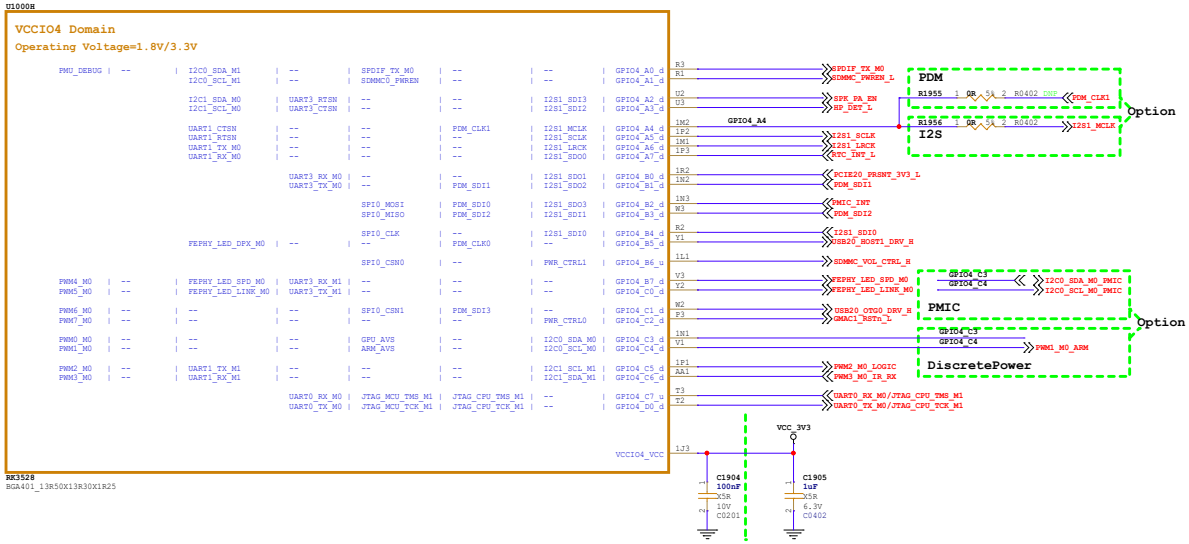
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_G(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3528_H(VCCIO4 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3528_REF_SCH
File:	19.RK3528_1.8V/3.3V GPIO
Date:	Saturday, May 06, 2023
Rev:	V1.0
Designed by:	HKS
Reviewed by:	Default
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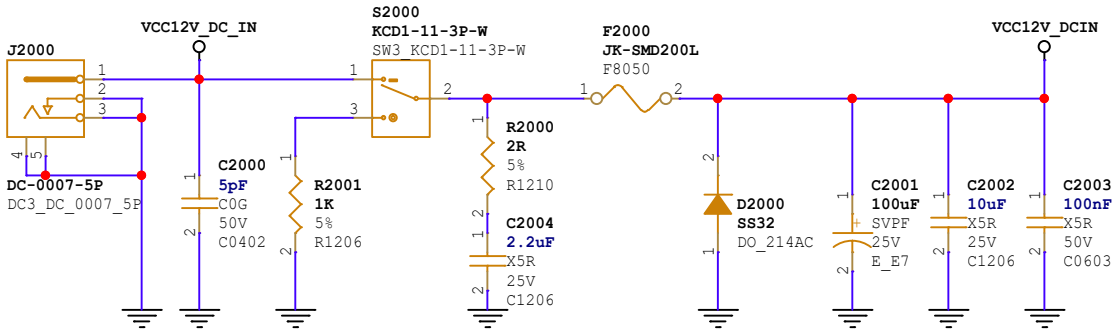
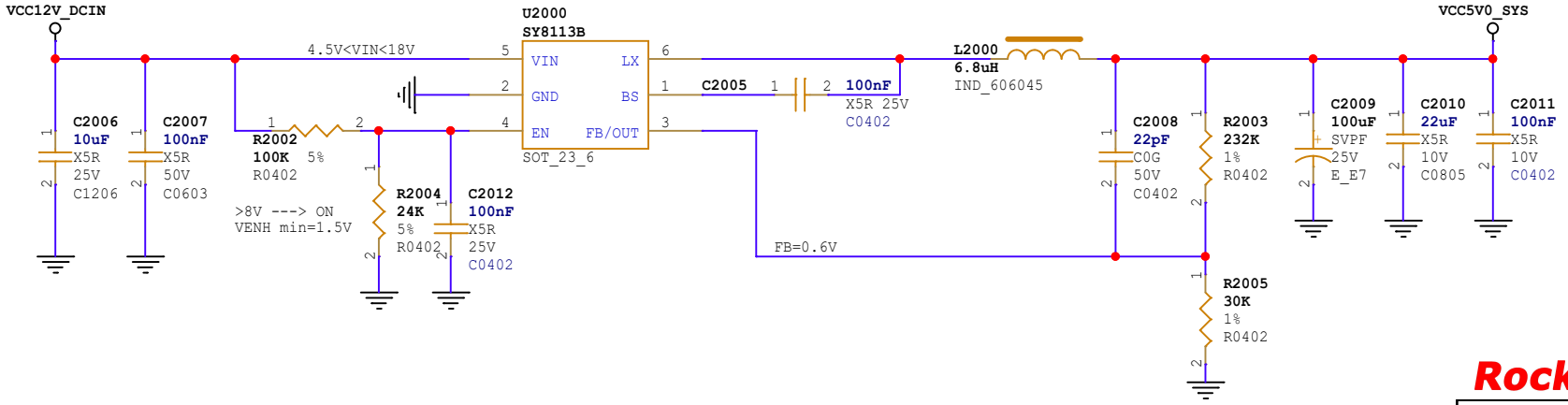
12V/3A DCIN



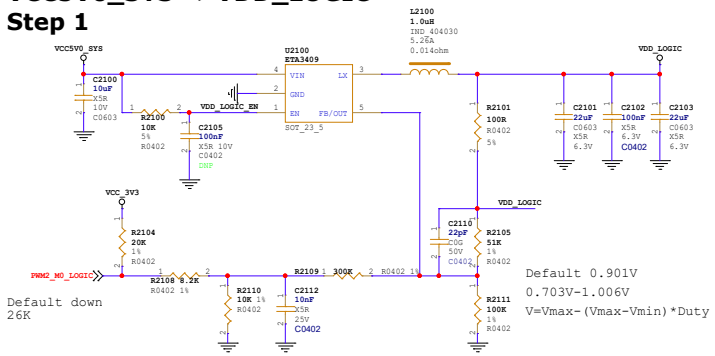
VCC5V0_SYS



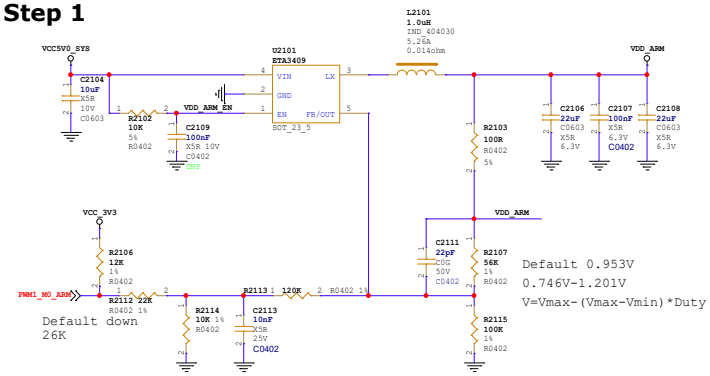
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	20.Power-DCIN				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	22 of 50

VCC5V0_SYS-->VDD_LOGIC
Step 1

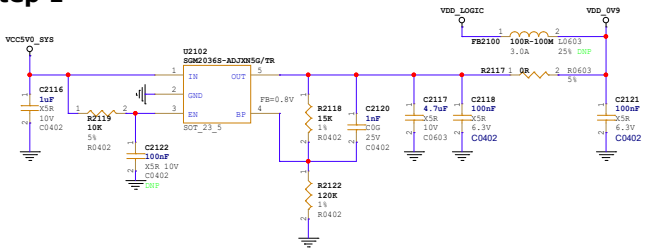


VCC5V0_SYS-->VDD_ARM
Step 1

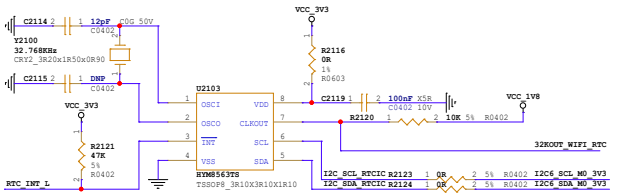


VCC5V0_SYS-->VDD_0V9
Step 1

Note:
When LAYOUT, a star must be used,
Branch to each load

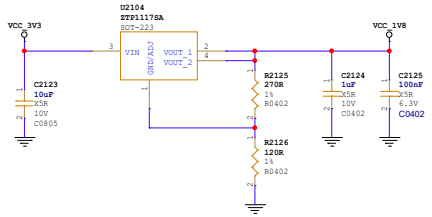


RTC IC

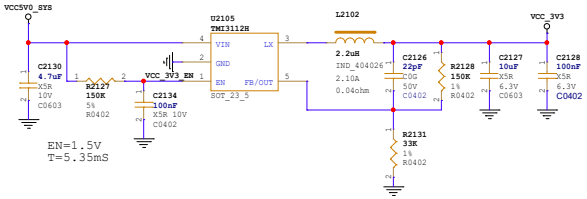


VCC_3V3->VCC_1V8(LDO)
Step 2

Note:
When LAYOUT, a star must be used,
Branch to each load

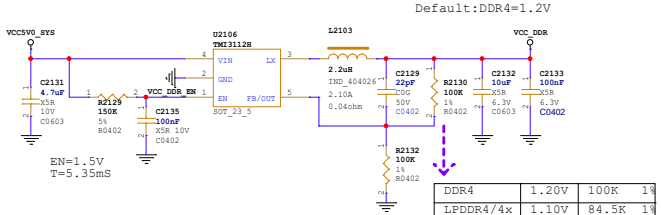


VCC5V0_SYS-->VCC_3V3
Step 2



VCC5V0_SYS-->VCC_DDR
Step 2

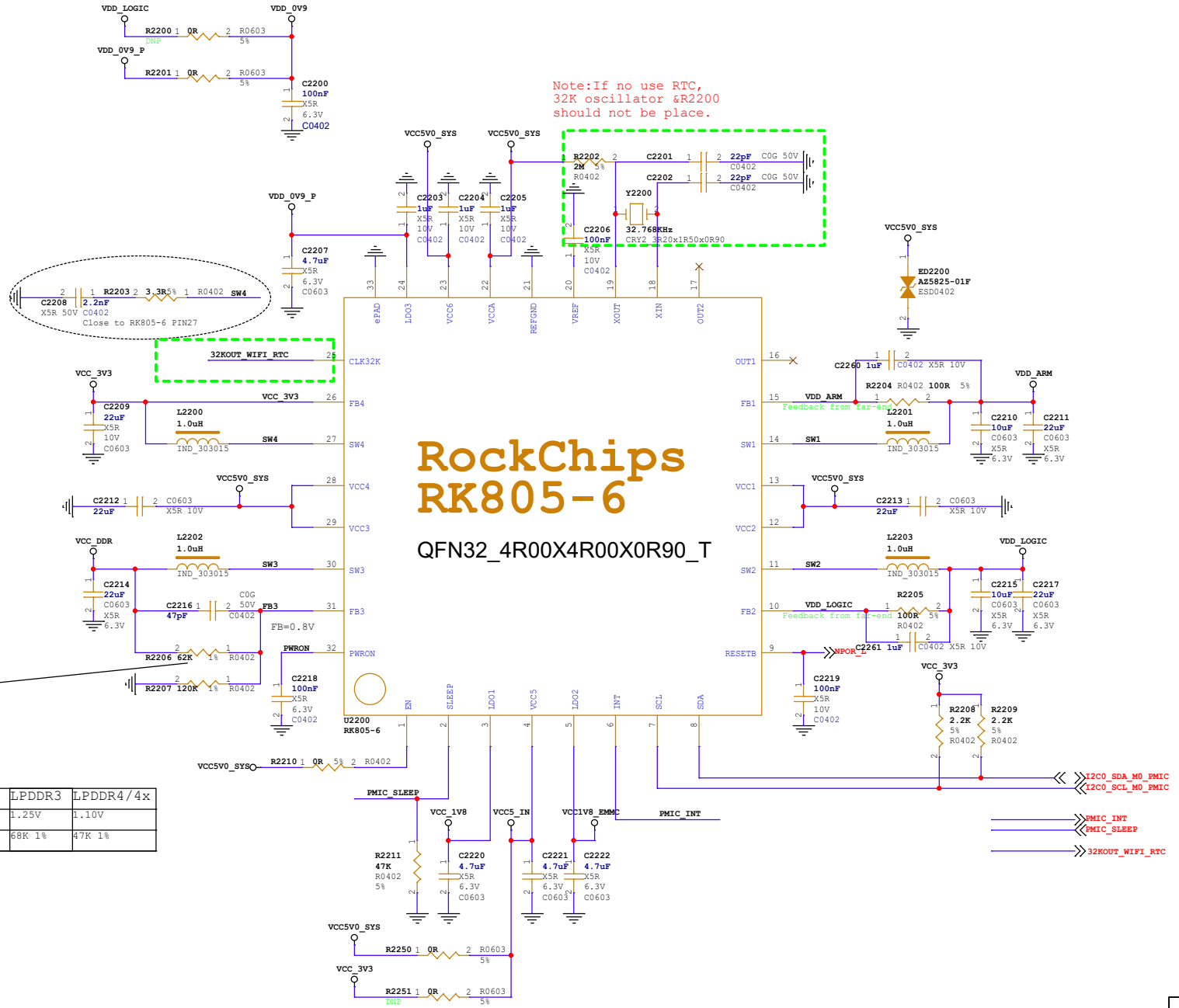
Default:DDR4=1.2V



DDR4	1.20V	100K 1%
LPDDR4/4x	1.10V	84.5K 1%
DDR3	1.5V	150K 1%
DDR3L	1.35V	127K 1%
LPDDR3	1.25V	110K 1%

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3528_REF_SCH		
File:	21.Power-DiscretePower		
Date:	Tuesday, May 23, 2023	Rev:	V1.0
Designed by: HKS	Reviewed by: Default	Sheet:	23 of 50

PMIC RK805-6



VCC_DDR

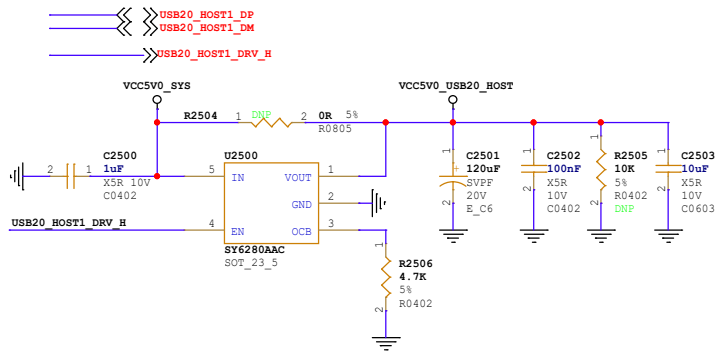
Default:DDR4=1.2V

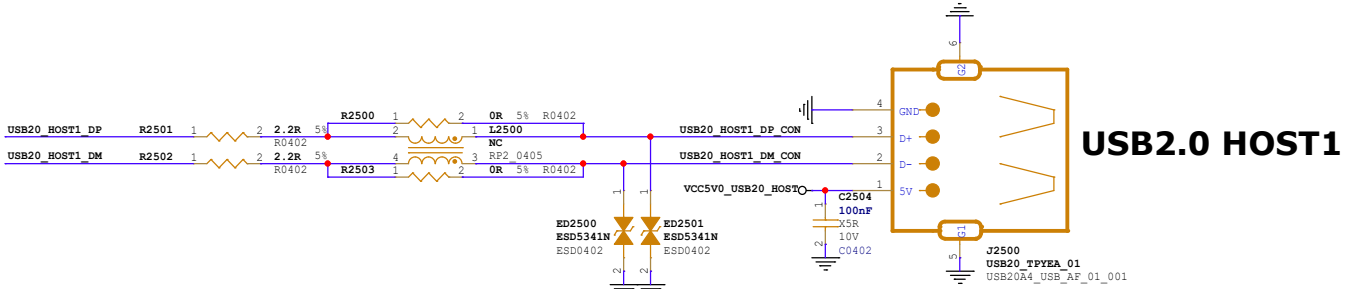
	DDR3	DDR3L	DDR4	LPDDR3	LPDDR4/4x
VCC_DDR	1.53V	1.35V	1.2V	1.25V	1.10V
R2206	110K 1%	82K 1%	62K 1%	68K 1%	47K 1%

Rockchip Confidential

Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH			
File:	22.Power-PMIC-RK805-6(OPTION)			
Date:	Saturday, May 27, 2023		Rev:	V1.0
Designed by:	HXS	Reviewed by: Default	Sheet:	24 of 50

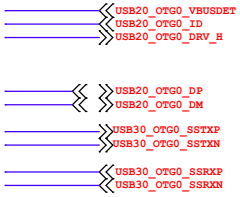
USB2.0_HOST1

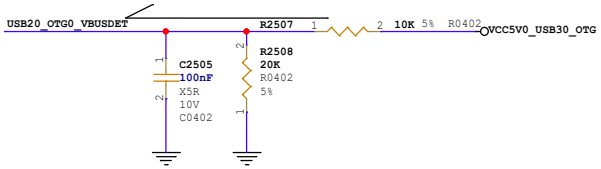


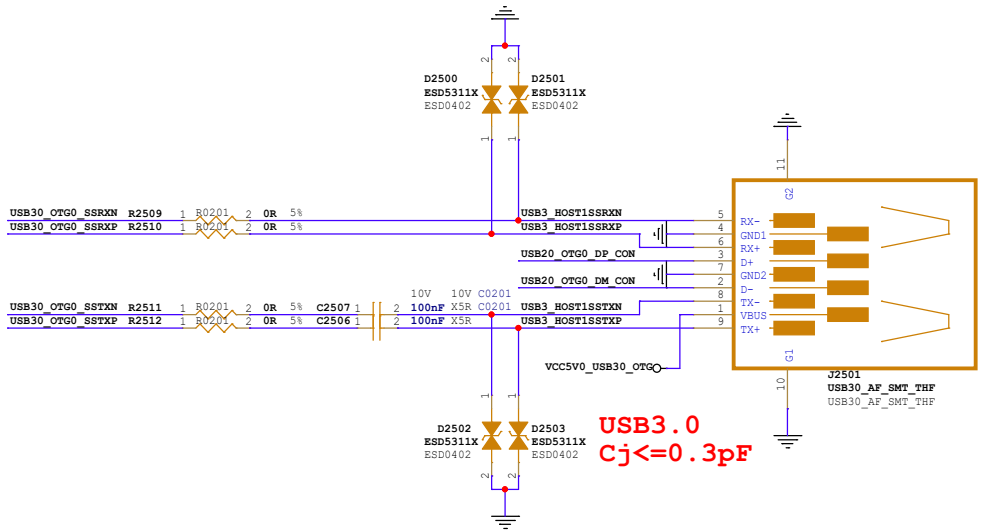


USB2.0 HOST1

USB3.0 OTG

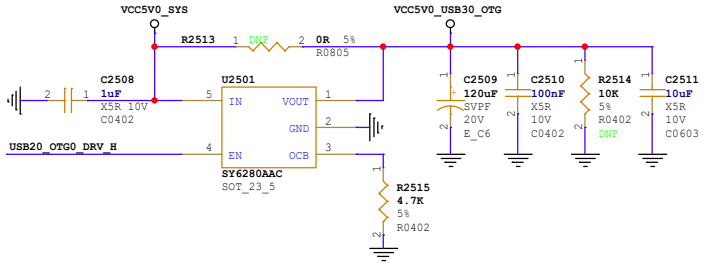


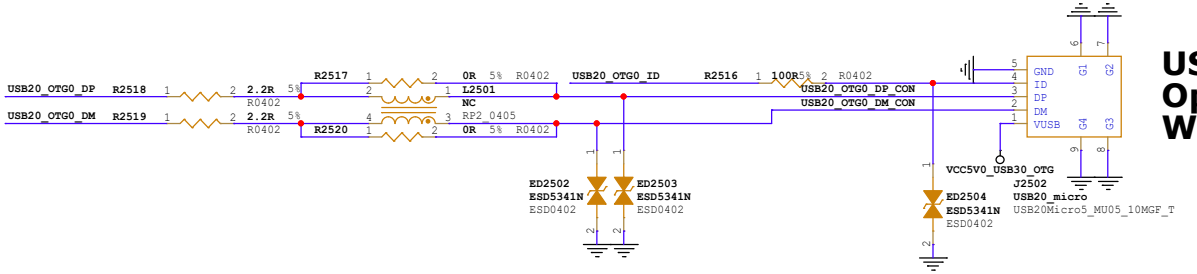




Default

USB3.0 OTG

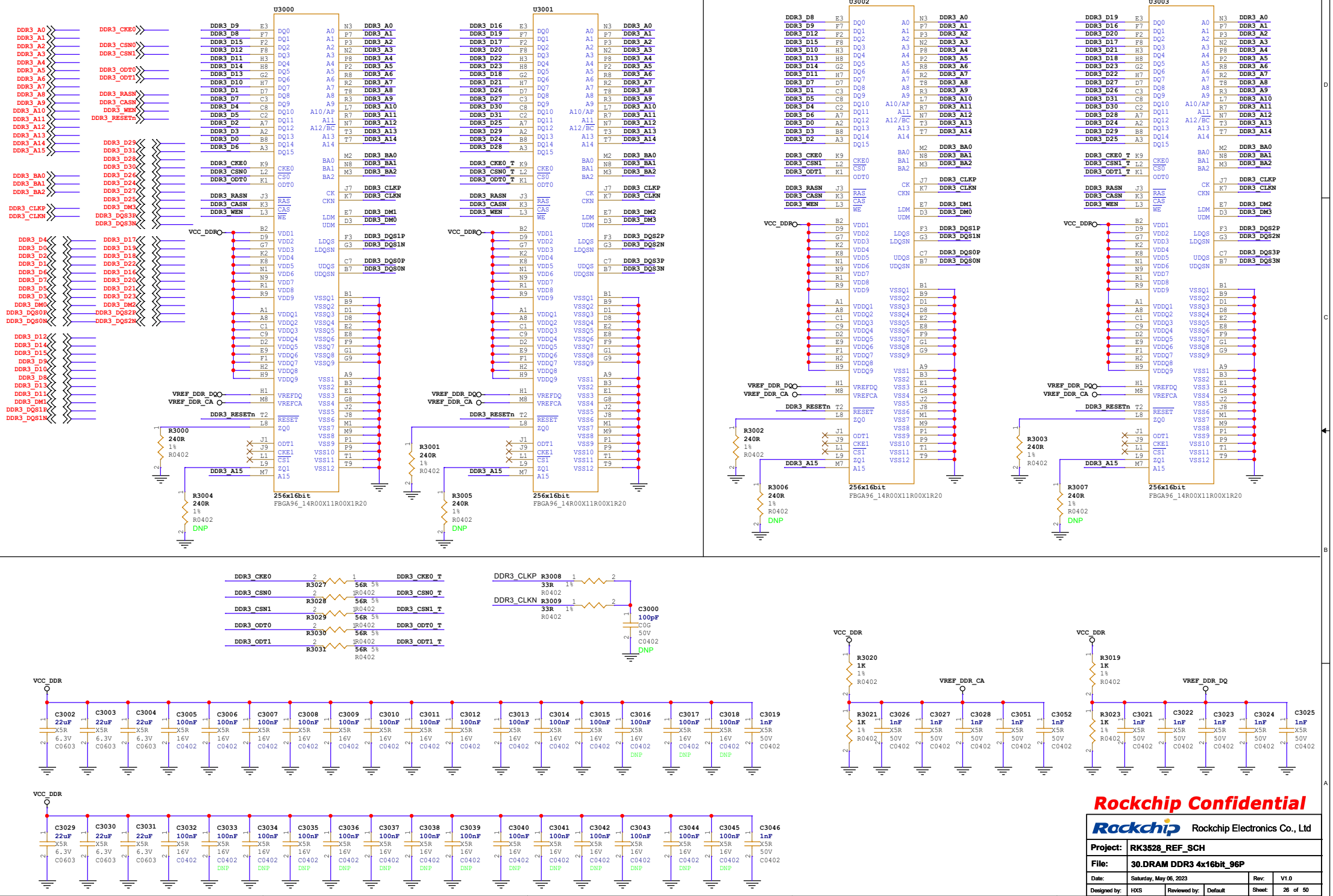




USB2.0 OTG Option With USB ID

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3528_REF_SCH		
File:	25.USB2/USB3 Port		
Date:	Saturday, May 06, 2023	Rev:	V1.0
Designed by:	HXS / Reviewed by: Default	Sheet:	25 of 50

4X16bit DDR3



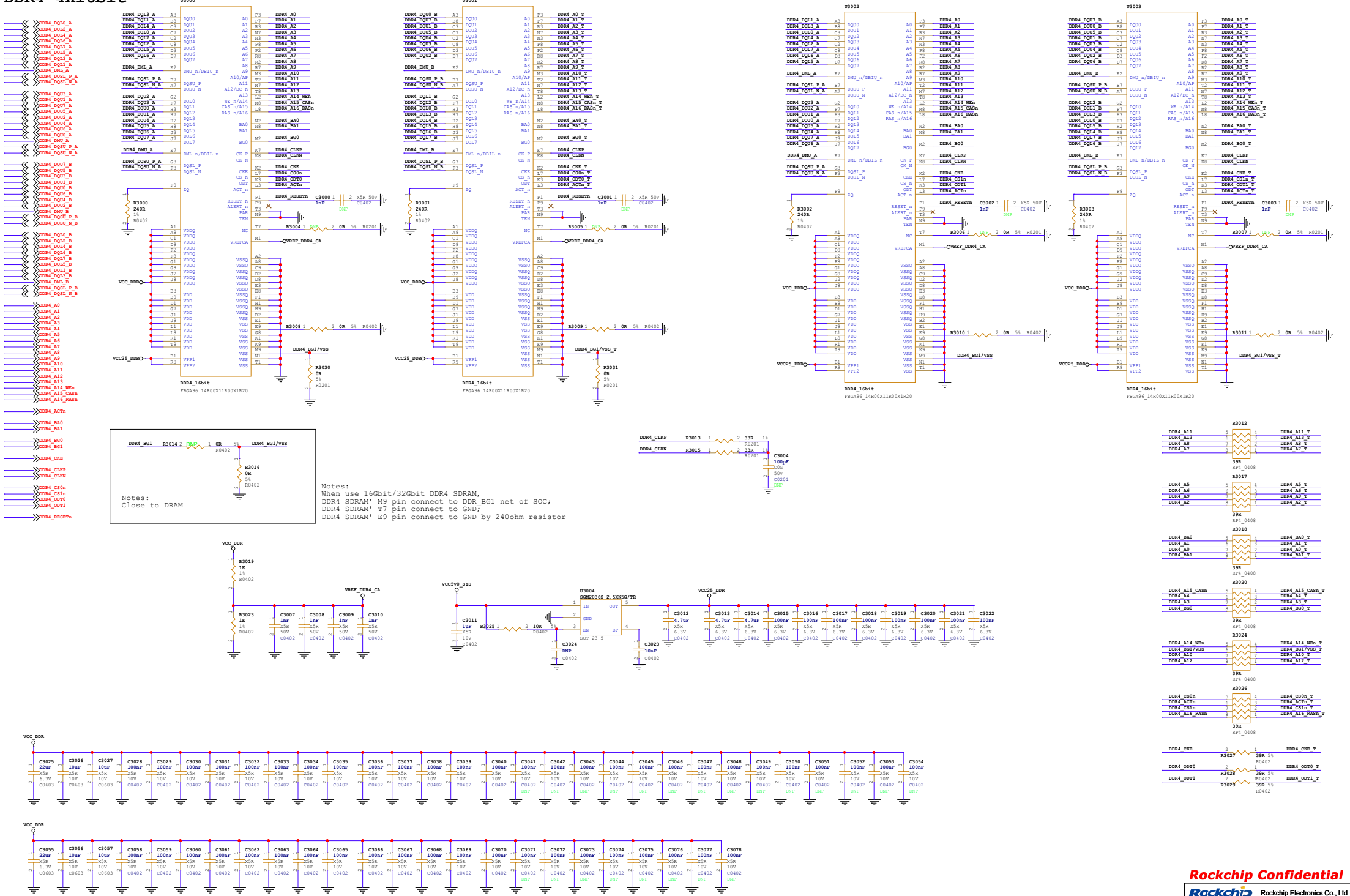
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	30.DRAM DDR3 4x16bit_96P				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	26 of 50

DDR4 2X16bit

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3528_REF_SCH		
File:	30.DRAM-DDR4_2x16Bit_96P		
Date:	Saturday, May 06, 2023	Rev:	V1.0
Designed by: HKS	Reviewed by: Default	Sheet:	27 of 50

DDR4 4X16bit



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3528_REF_SCH
File:	30.DRAM-DDR4_4x16Bit_96P
Date:	Saturday, May 06, 2023
Rev:	V1.0
Designed by:	HKS
Reviewed by:	Default
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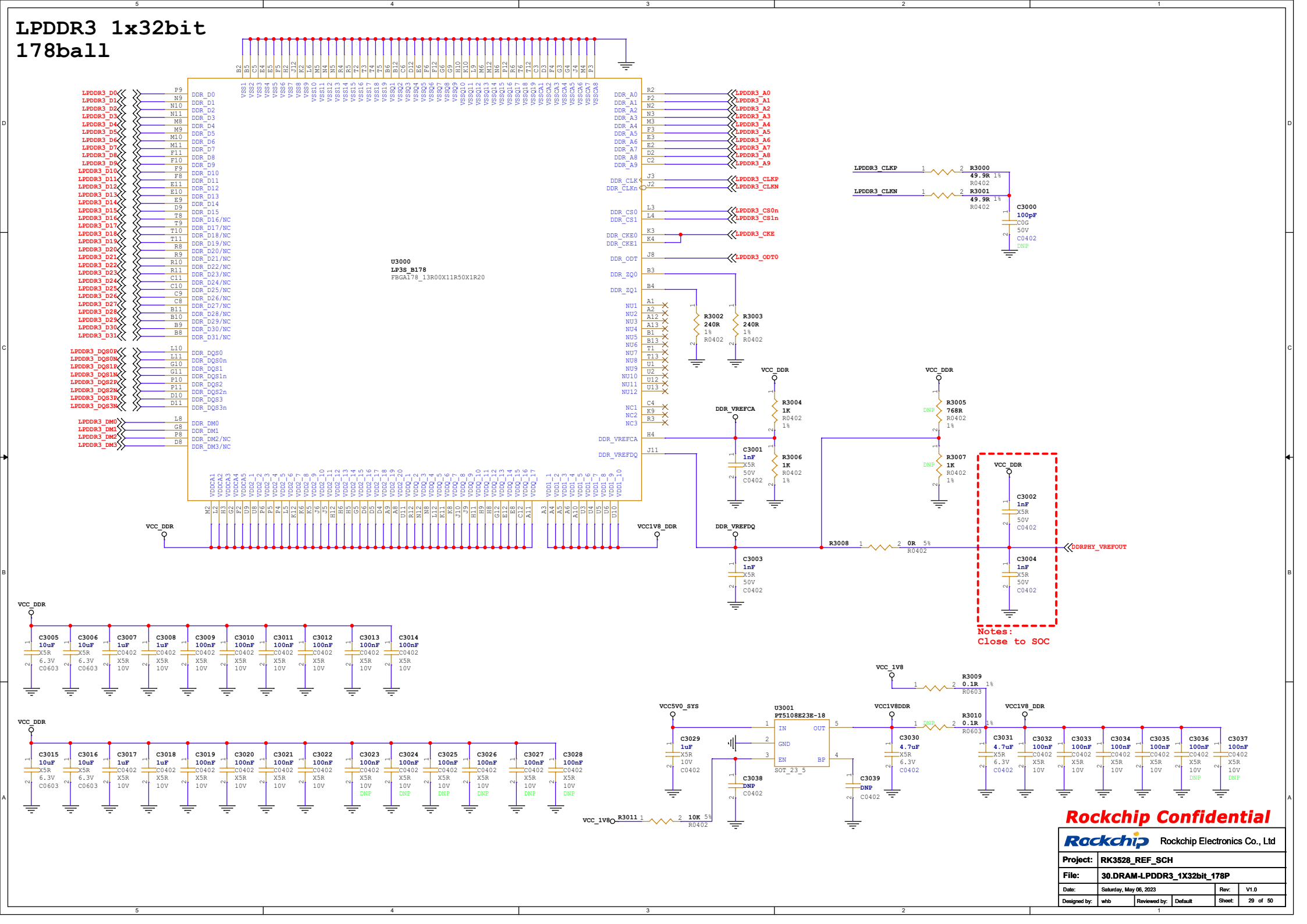
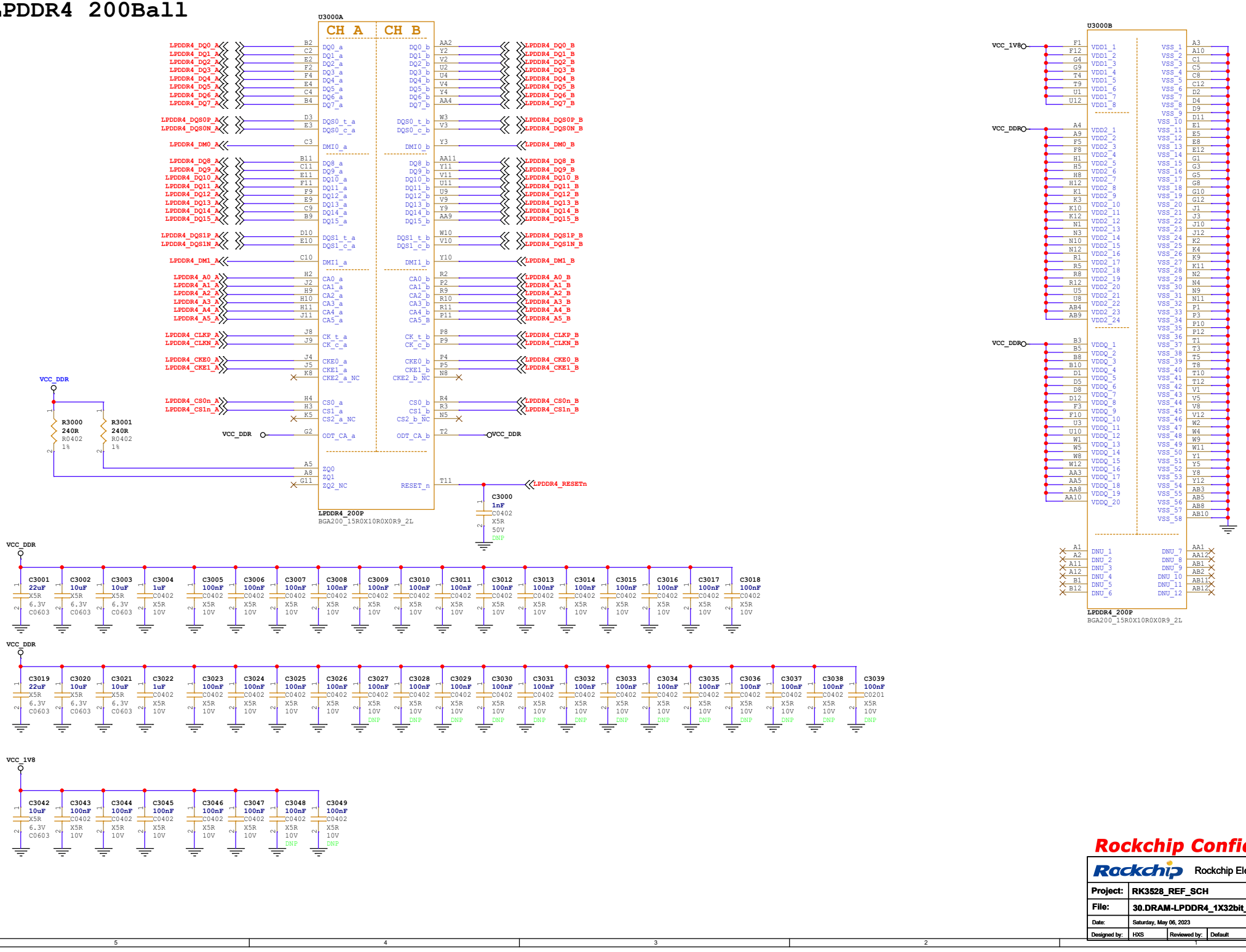
LPDDR3 1x32bit 178ball



Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	30.DRAM-LPDDR3_1X32bit_178P				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	whb	Reviewed by:	Default	Sheet:	29 of 50

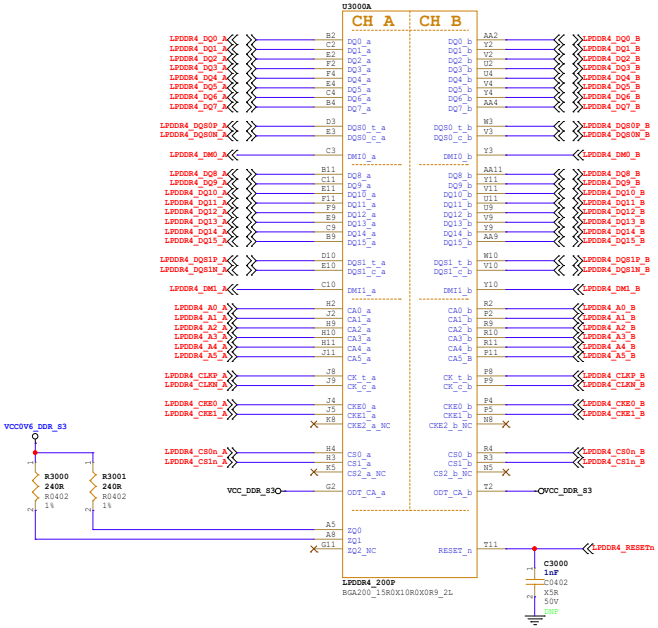
LPDDR4 200Ball

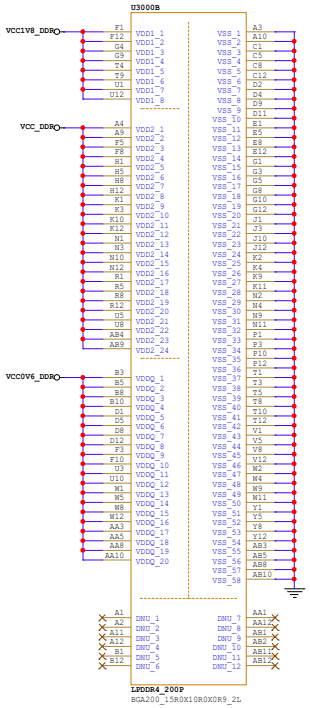


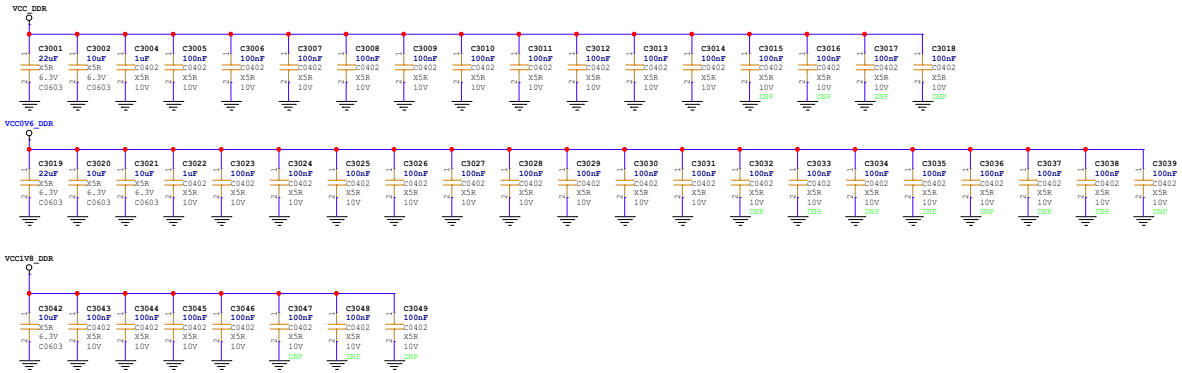
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3528_REF_SCH		
File:	30.DRAM-LPDDR4_1X32bit_200P		
Date:	Saturday, May 06, 2023	Rev:	V1.0
Designed by: HXS	Reviewed by: Default	Sheet:	30 of 50

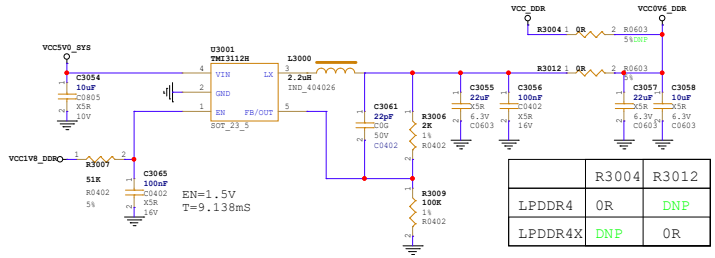
LPDDR4X 200Ball





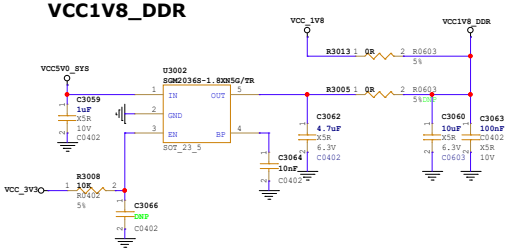


VCC0V6_DDR



	R3004	R3012
LPDDR4	0R	DNP
LPDDR4X	DNP	0R

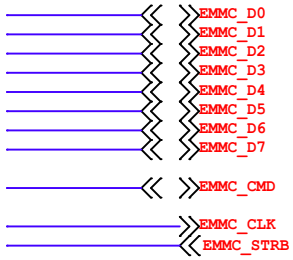
VCC1V8_DDR

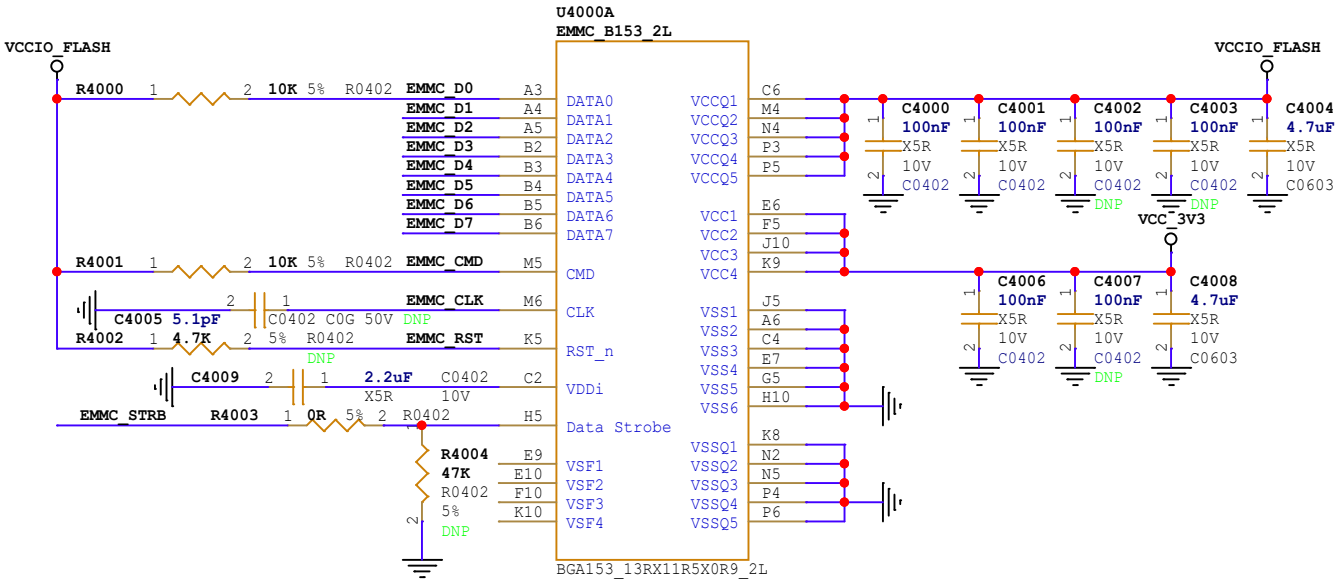


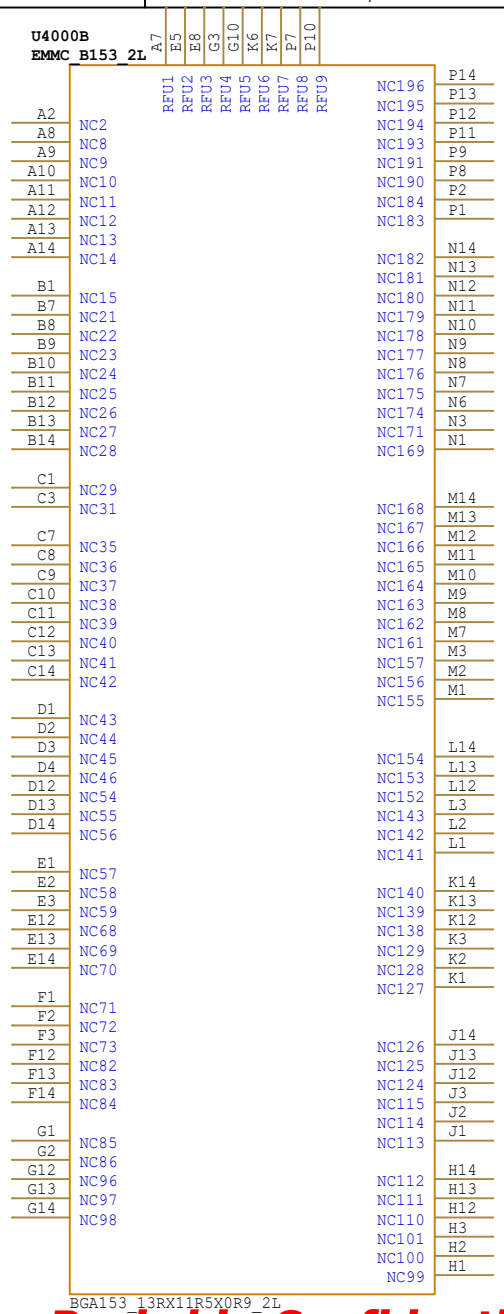
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3528_REF_SCH
File:	30.DRAM-LPDDR4X_1X32bit_200P
Date:	Saturday, May 06, 2023
Rev:	V1.0
Designed by:	HKS
Reviewed by:	Default
Sheet:	31 of 50

EMMC



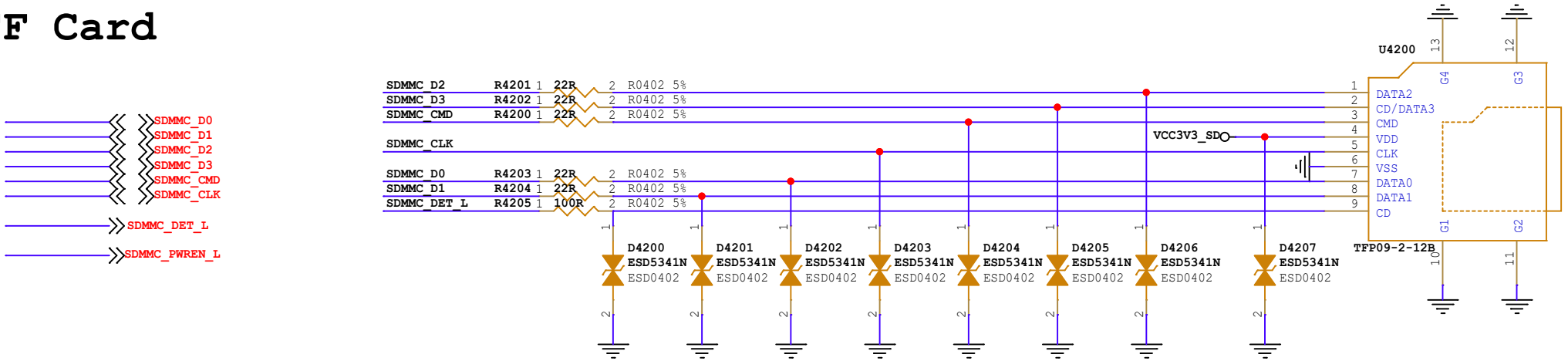




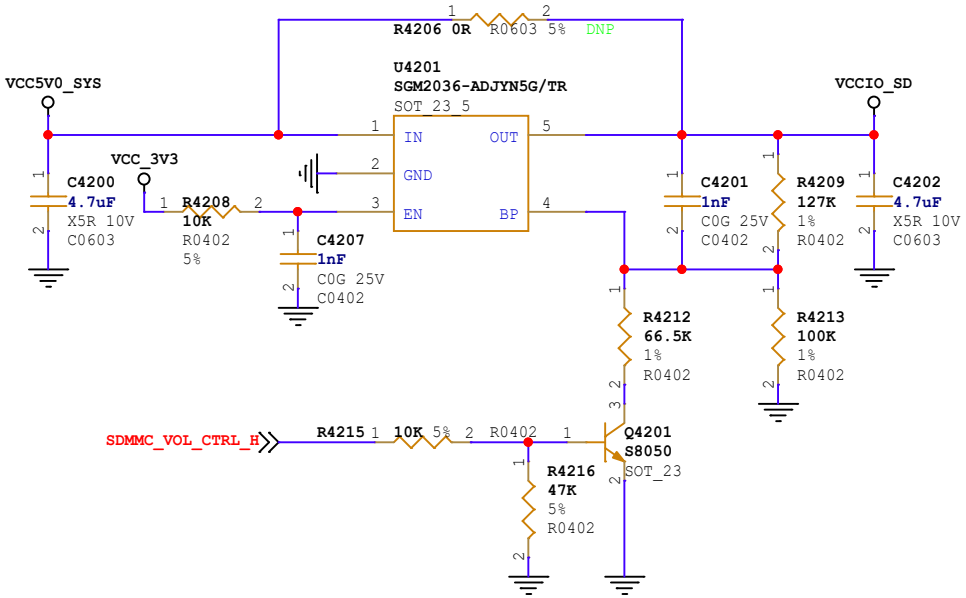
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	40.Flash-eMMC				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	32 of 50

TF Card

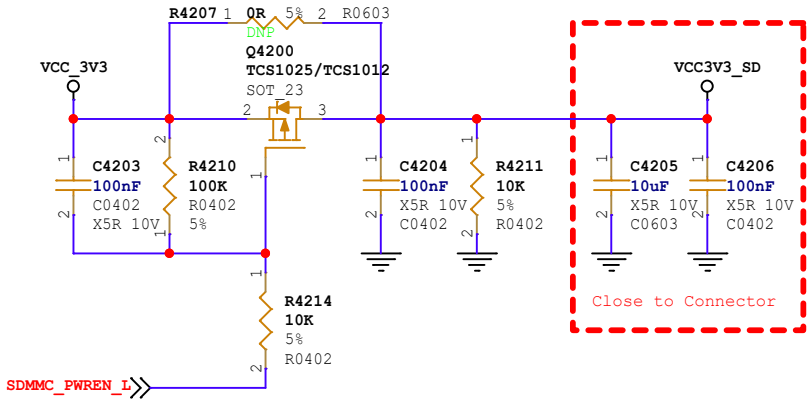


VCCIO_SD



SDIO2.0 SDMMC0_VOL_CTRL=H VCCIO_SD=3.34V(Default)
SDIO3.0 SDMMC0_VOL_CTRL=L VCCIO_SD=1.816V

VCC3V3_SD



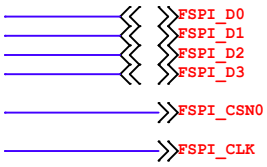
SDMMC_PWREN=L VCC_SD=3.3V(Default)
SDMMC_PWREN=H VCC_SD=0V

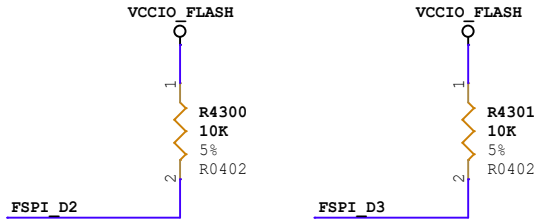
Rockchip Confidential

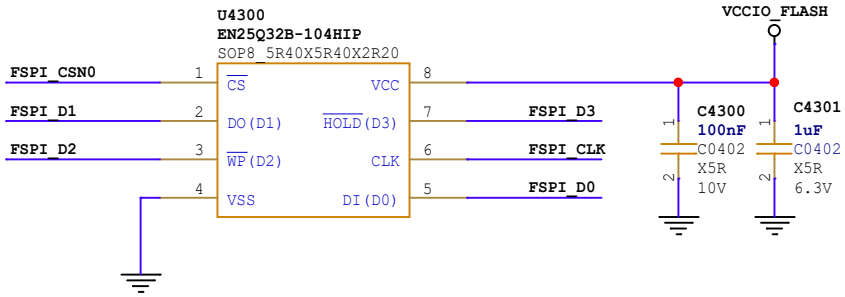
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	42.Flash-Micro-SD Card				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	33 of 50

FSPI

Default VCC = 1.8V

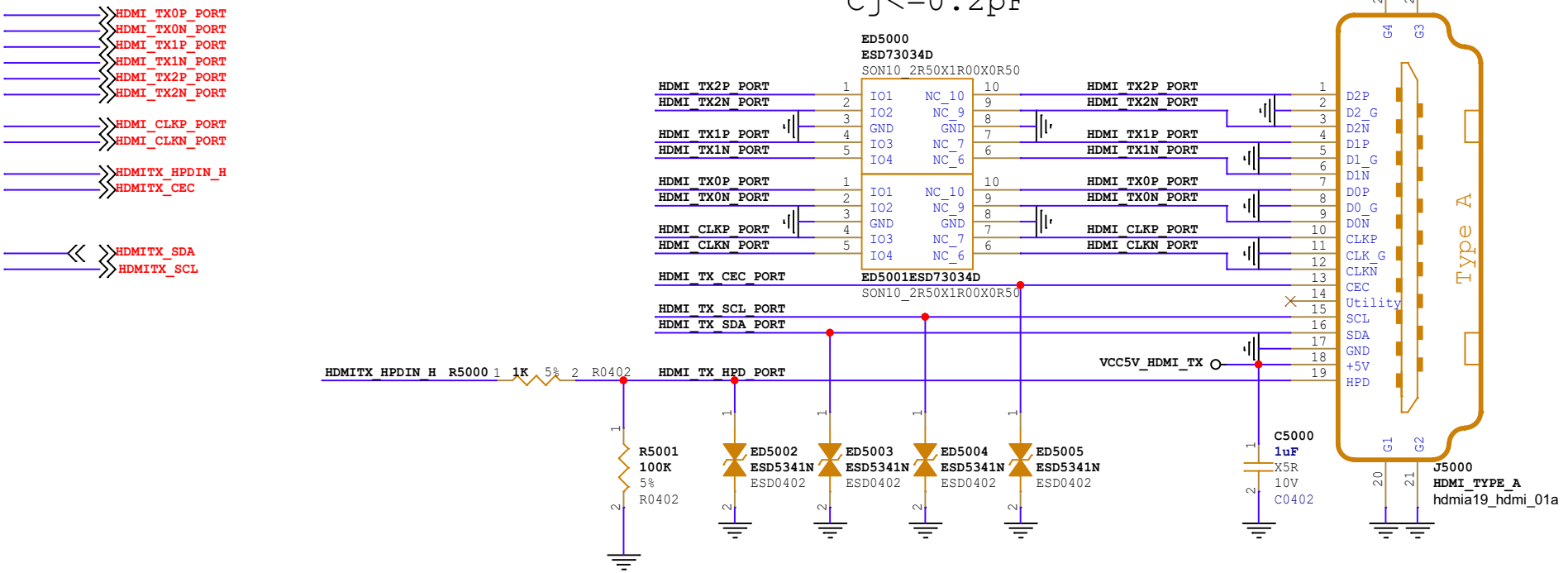




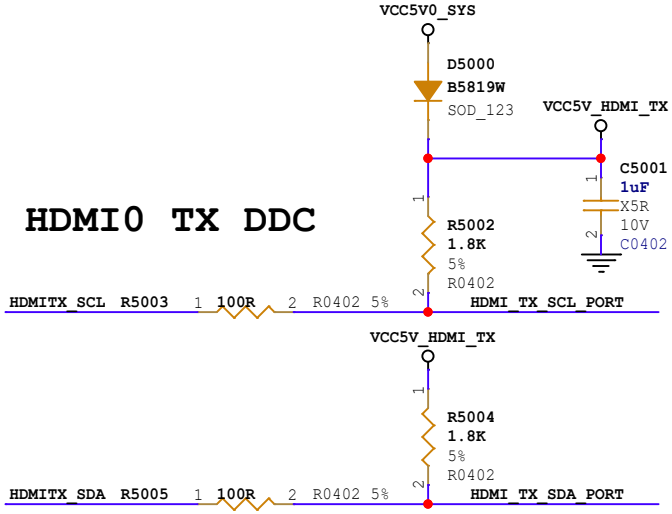


Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	43.Flash-SPI FLASH(Option)				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	34 of 50

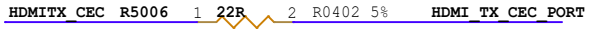
HDMI2.0 TX



HDMI0 TX DDC



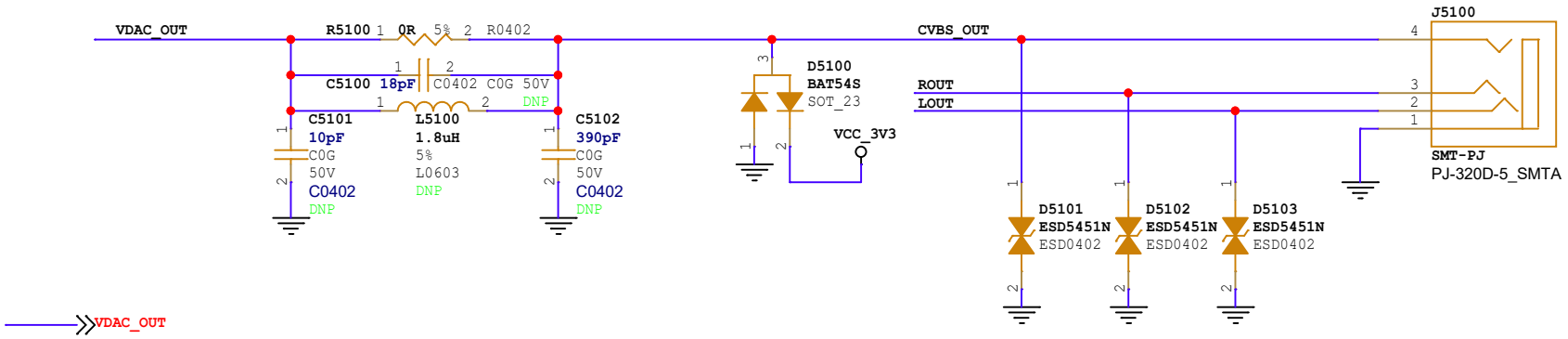
HDMI0 TX CEC



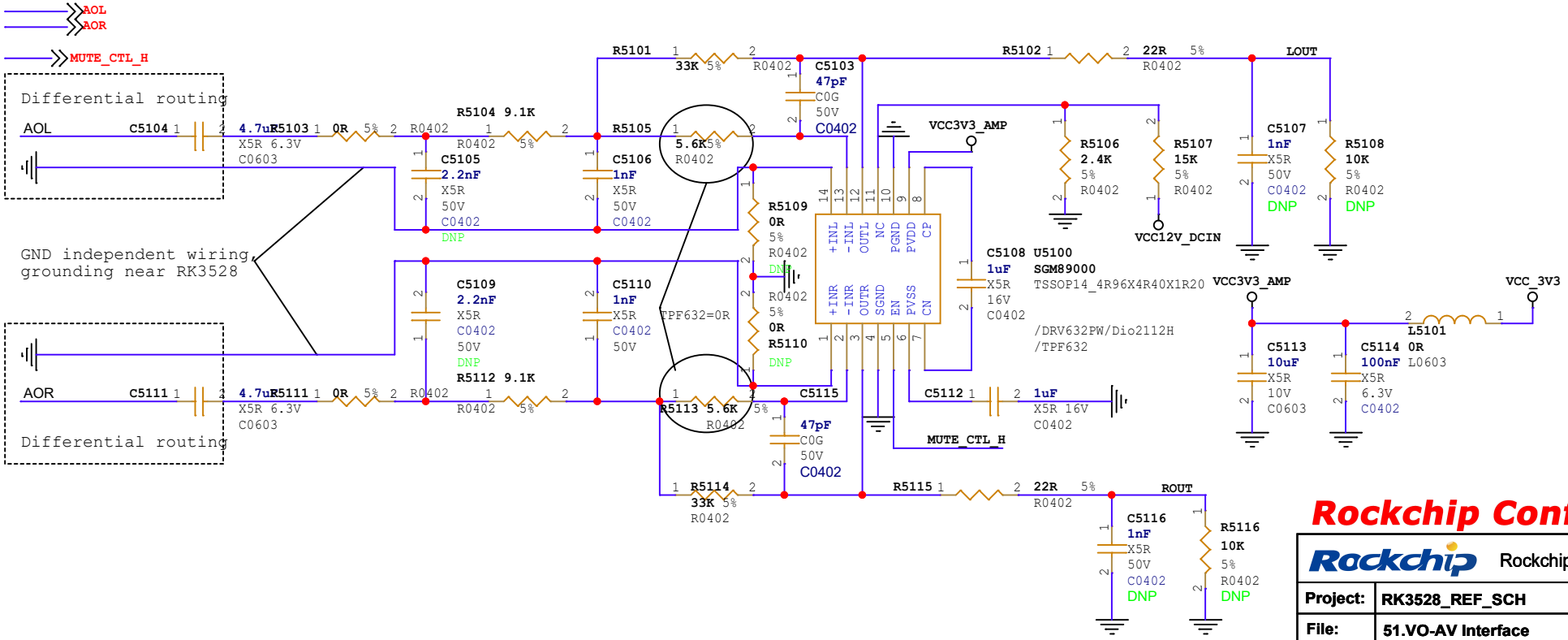
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	50.VO-HDMI TX				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	35 of 50

AV_OUT



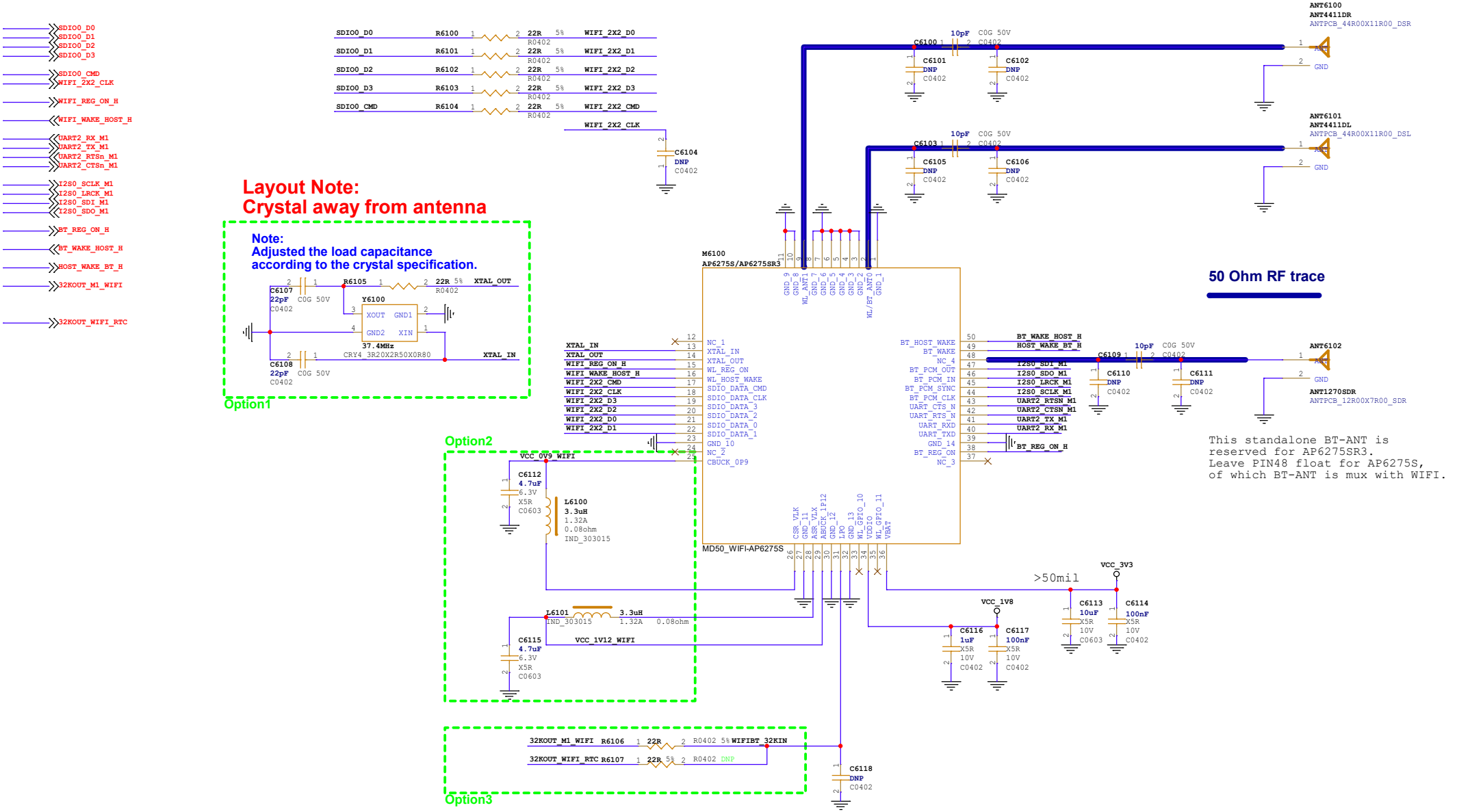
2-Vrms Audio Line Driver



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	51.VO-AV Interface				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	36 of 50

SDIO WIFI/BT



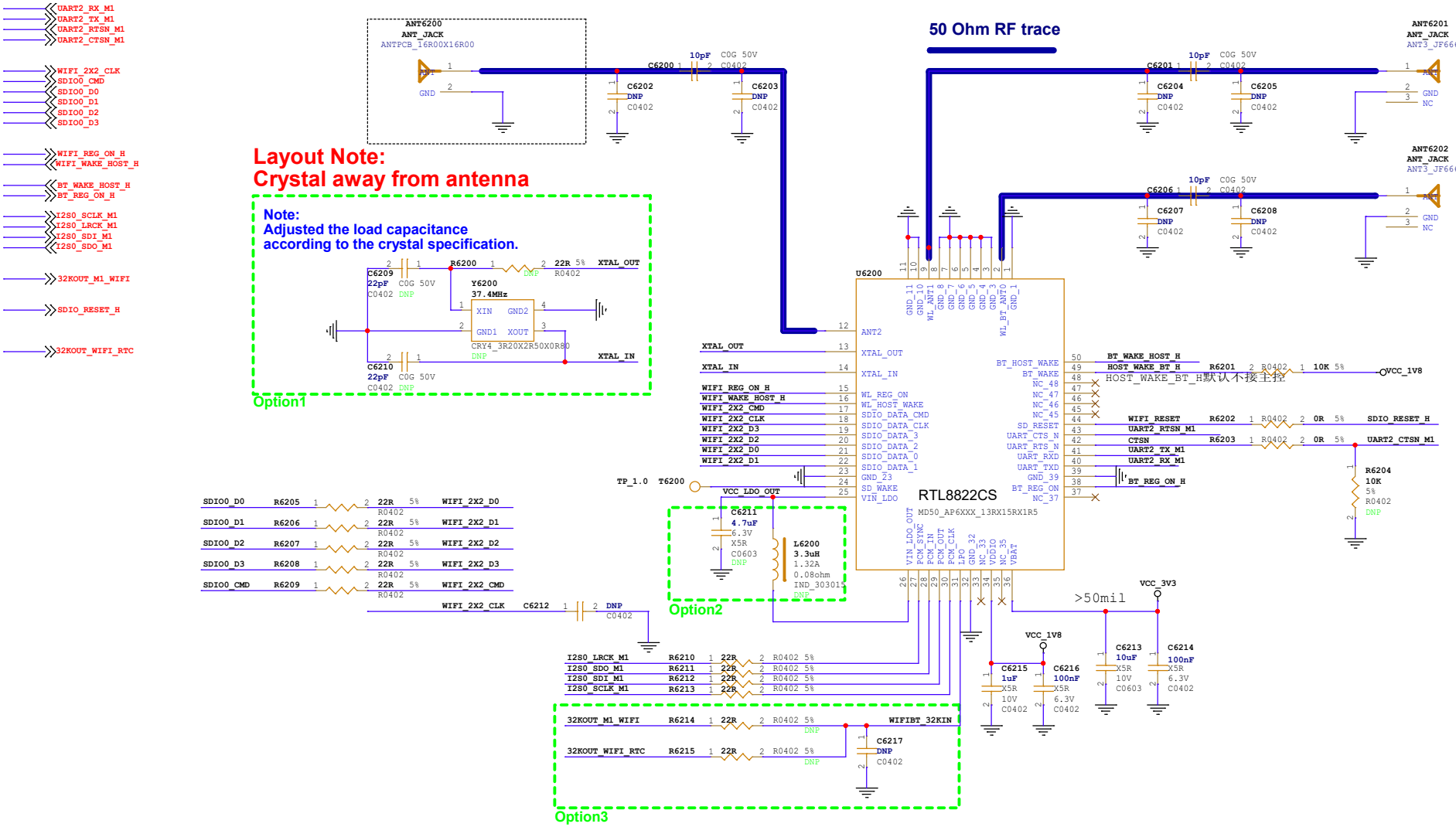
OPTION	WIFI					BT	Crystals	VDDIO	Option1	Option2	Option3
	a	b/g/n	ac	ax	5GHz						
AP6275S /AP6275SR3	Yes	Yes	Yes	Yes	Yes	5.0	37.4MHz	1.71-3.6V	Yes	Yes	Yes

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3528_REF_SCH		
File:	61.WIF/BT-SDIO_2T2R_AP6275S		
Date:	Saturday, May 06, 2023	Rev:	V1.0
Designed by: HXS	Reviewed by: Default	Sheet:	37 of 50

SDIO WIFI/BT



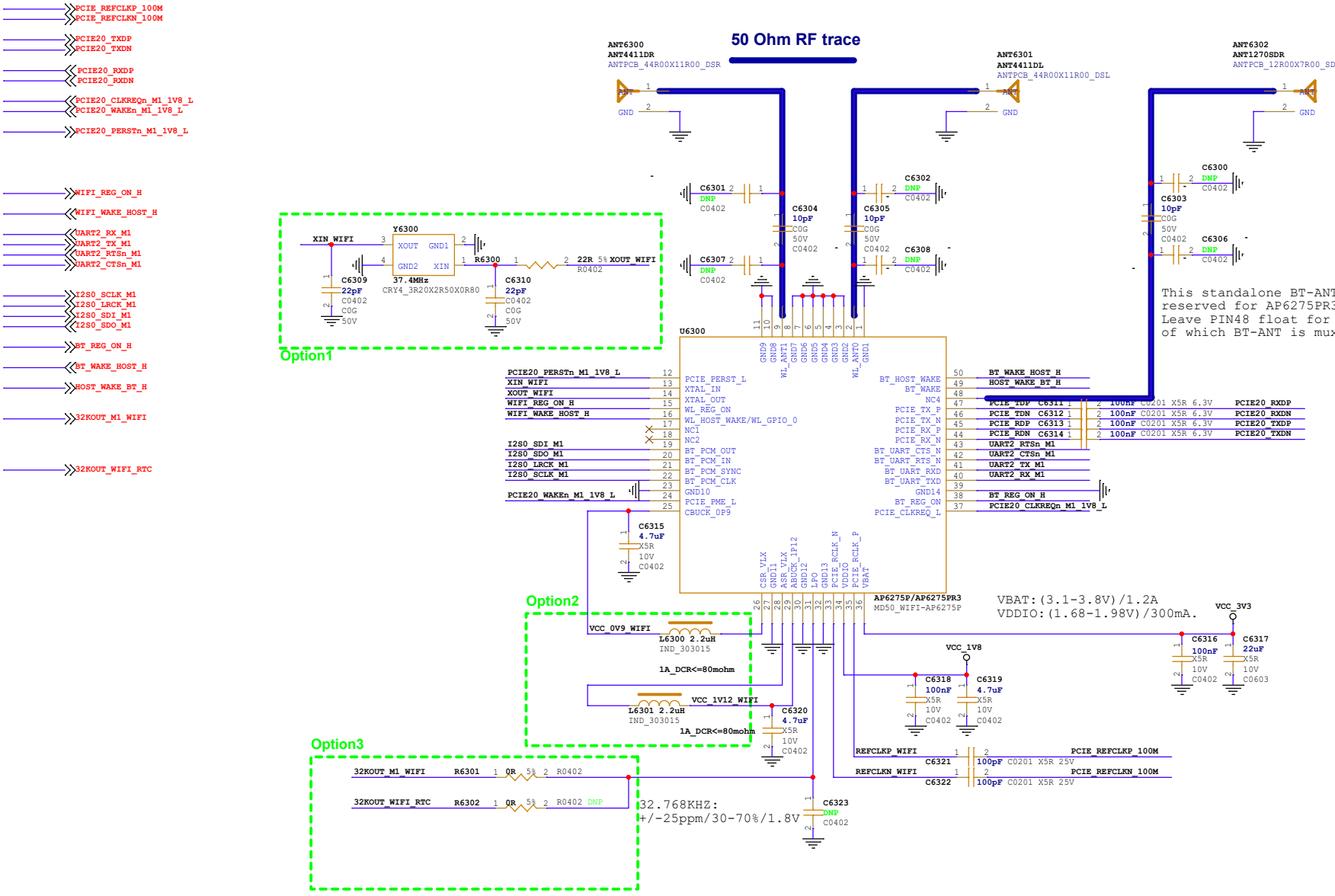
OPTION	WIFI					BT	Crystals	VDDIO	Option1	Option2	Option3
	a	b/g/n	ac	ax	5GHz						
RTL8822CS UWE5621DS	Yes	Yes	Yes	NO	Yes	5.1	/	1.71-3.6V	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3528_REF_SCH		
File:	62.WIF/BT-SDIO_2T2R_RTL8822CS		
Date:	Saturday, May 06, 2023	Rev:	V1.0
Designed by: HXS	Reviewed by: Default	Sheet:	38 of 50

PCIe WIFI6/BT



OPTION	WIFI					BT	Crystals	VDDIO	Option1	Option2	Option3
	a	b/g/n	ac	ax	5GHz						
AP6275P /AP6275PR3	Yes	Yes	Yes	Yes	Yes	5.0	37.4MHz	1.71-3.6V	Yes	Yes	Yes

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3528_REF_SCH		
File:	63.WIFI6/BT-PCIe_2T2R_AP6275P		
Date:	Saturday, May 06, 2023	Rev:	V1.0
Designed by: HXS	Reviewed by: Default	Sheet:	39 of 50

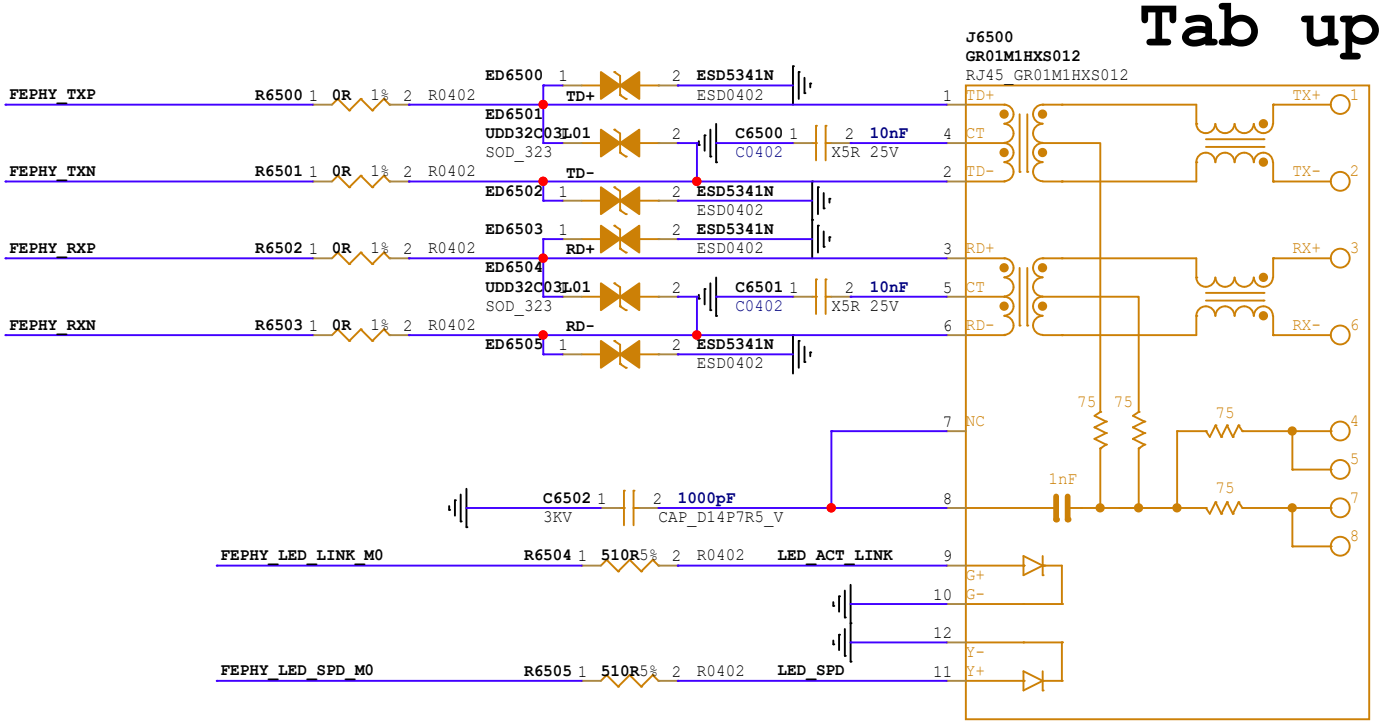
10/100M Embed FEPHY

FEPHY_TXP
FEPHY_TXN

FEPHY_RXP
FEPHY_RXN

FEPHY_LED_SPD_M0
FEPHY_LED_LINK_M0

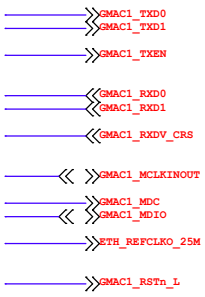
Tab up

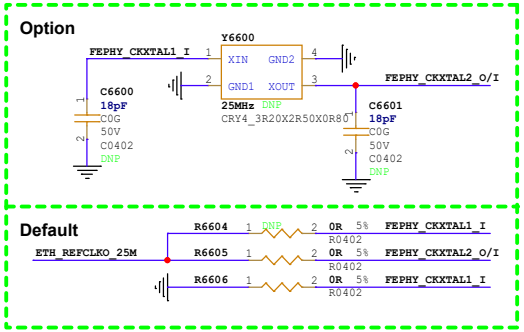


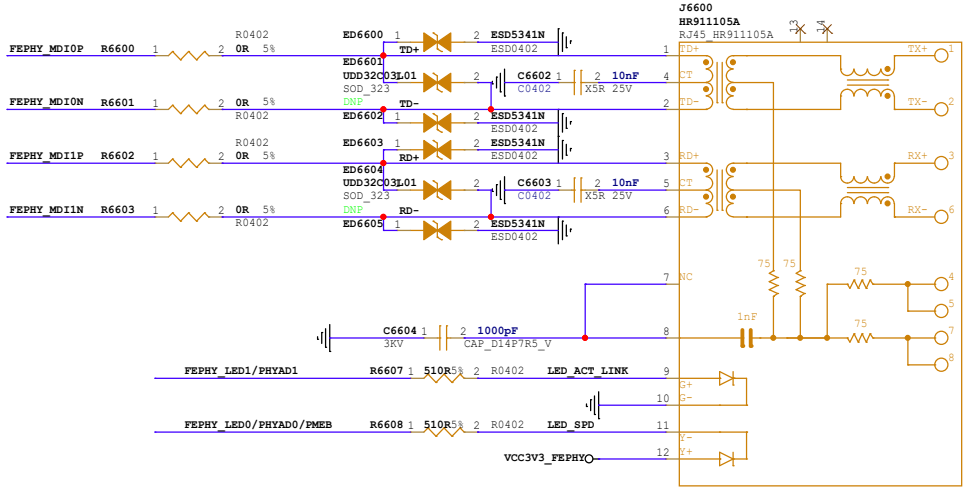
Rockchip Confidential

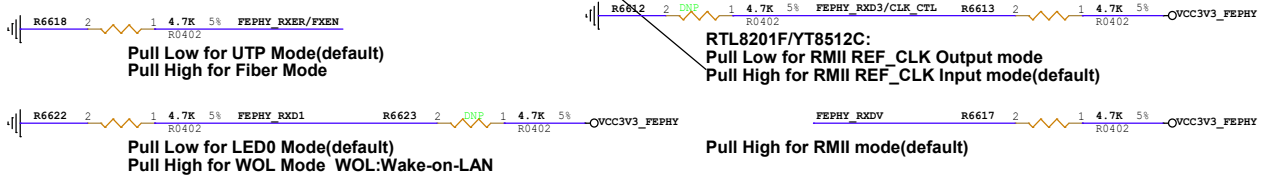
Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	65.10/100M-Embed PHY				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	40 of 50

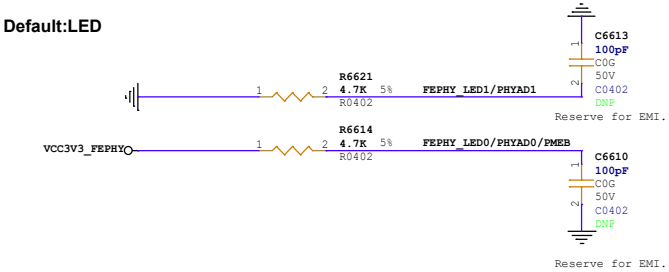
FE PHY





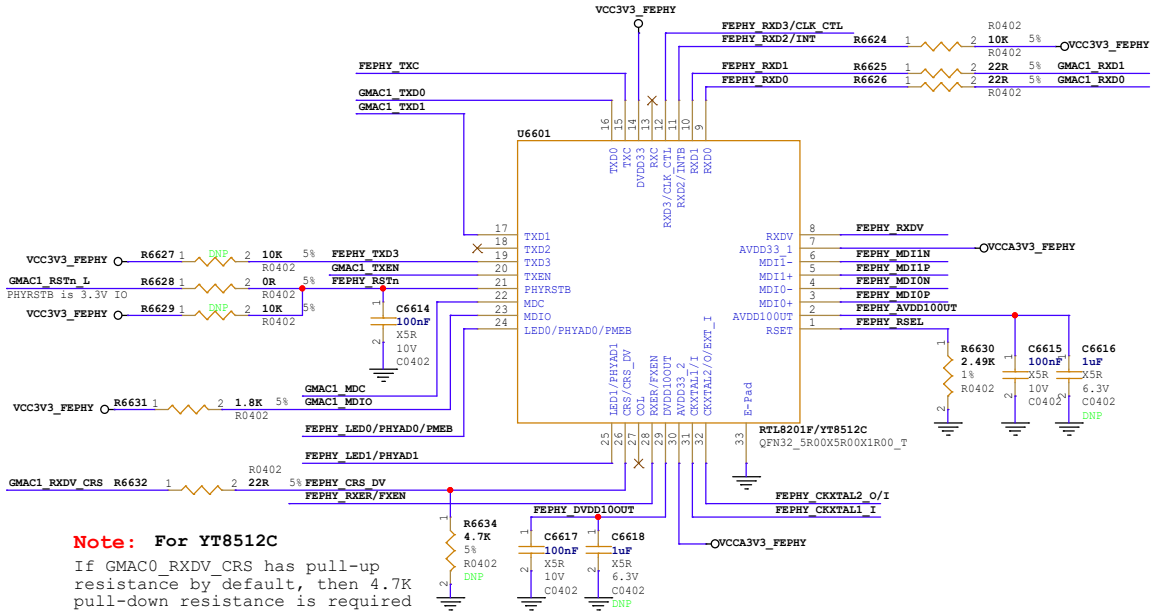






PHY Address Config

PHY Address	PHYAD[1:0]
1 (default)	2'b01

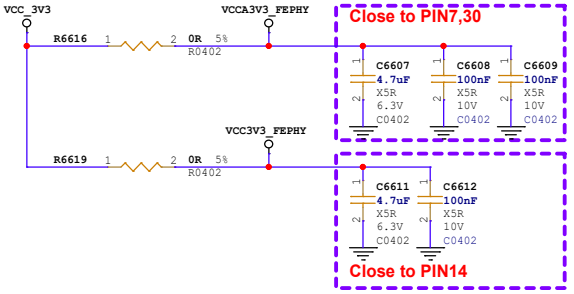


Note: For YT8512C

If GMAC0_RXDV_CRS has pull-up resistance by default, then 4.7K pull-down resistance is required

Note:

RTL8201F/YT8512C only support 3.3V IO
VCCIO3 must be changed to 3.3V power supply



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	66.Ethernet-FEPHY_RMII				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	41 of 50

RGMII

GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_TXEN
GMAC1_TXCLK
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_RXDV_CRS
GMAC1_RXCLK
ETH_REFCLKO_25M
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO
GMAC1_RSTn_L

PHY_XTALOUT — Y6700 (XIN GND2 / GND1 XOUT) 25MHz CRY4_3R20X2R50X0R80 — PHY_XTALIN
C6700 18pF C0G 50V C0402
C6701 18pF C0G 50V C0402
R6701 0R 5% R0402 DNP
ETH_REFCLKO_25M — R6708 DNP 0R 5% R0402 — PHY_XTALOUT

GMAC1_MCLKINOUT — R6710 100R 5% R0402 — PHY_CLKOUT125
C6703 DNP C0402
R6712 120R 5% R0402
3.3Vpp
MAC <----- PHY

VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R

Default

PHY_MDI3- R6700 0R R0402 — PHY_MDI_3-
PHY_MDI3+ R6704 0R R0402 — PHY_MDI_3+
PHY_MDI2- R6702 0R R0402 — PHY_MDI_2-
PHY_MDI2+ R6703 0R R0402 — PHY_MDI_2+
PHY_MDI1- R6705 0R R0402 — PHY_MDI_1-
PHY_MDI1+ R6706 0R R0402 — PHY_MDI_1+
PHY_MDI0- R6707 0R R0402 — PHY_MDI_0-
PHY_MDI0+ R6709 0R R0402 — PHY_MDI_0+

PHY_MDI_3+ / PHY_MDI_3- — ED6700 ESD5341N ESD0402 DNP
PHY_MDI_2+ / PHY_MDI_2- — ED6701 ESD5341N ESD0402 DNP
PHY_MDI_1+ / PHY_MDI_1- — ED6702 ESD5341N ESD0402 DNP
PHY_MDI_0+ / PHY_MDI_0- — ED6703 ESD5341N ESD0402 DNP
ED6704 ESD5341N ESD0402 DNP
ED6705 ESD5341N ESD0402 DNP
ED6706 ESD5341N ESD0402 DNP
ED6707 ESD5341N ESD0402 DNP

J6700
MDI3- / MDI3+ / MDI2+ / MDI2- / MDI1+ / MDI1- / MDI0+ / MDI0- / TCT / Earth / G+ / G- / Y+ / Y-
HR911130C
RJ45_HR911130C
Tab down

C6702 10nF X5R C0402 25V — PHY_CHASSIS_GND
PHY_LED1/CFG_LDO0
VCC3V3_PHY
R6711 510R 5% R0402
R6713 510R 5% R0402
R6714 DNP 0R 5% R0402
PHY_LED2/CFG_LDO1
R6715 0R 5% R0402
R6716 DNP 510R 5% R0402
C6704 1000pF 2KV C1206 — PHY_CHASSIS_GND

HR915330CE: -40~85

U6700
RK631
QFN40_5R00X5R00X0R90_T

VDD10_PHY
R6722 2.49K 1% R0402
VCC3V3_PHY
T6700 TP_1.0

E_Pad
RSTn
PHY_XTALOUT
PHY_XTALIN
PHY_CLKOUT125
PHY_LED2/CFG_LDO1
PHY_LED1/CFG_LDO0
PHY_LED0/CFG_EXT
AVDD33
REGO
AVDD10
XTAL_IN/EXT_CLKIN
XTAL_OUT
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB

PHY_MDI0+ / PHY_MDI0- — MDI[0]+ / MDI[0]-
VDD10_PHY — AVDD10
PHY_MDI1+ / PHY_MDI1- — MDI[1]+ / MDI[1]-
PHY_MDI2+ / PHY_MDI2- — MDI[2]+ / MDI[2]-
VDD10_PHY — AVDD10
PHY_MDI3+ / PHY_MDI3- — MDI[3]+ / MDI[3]-

REG_OUT — PHY_REG_OUT
DVDD33 — VCC3V3_PHY
DVDD_RG — VCCIO_PHY
RXC/PHYAD1 — PHY_RXCLK/PHYAD1
RXCTL/PHYAD2 — PHY_RXDV/PHYAD2
RXD0/RXDLY — PHY_RXD0/RXDLY
RXD1/TXDLY — PHY_RXD1/TXDLY
RXD2/PLLOFF — PHY_RXD2/PLLOFF
RXD3/PHYAD0 — PHY_RXD3/PHYAD0
DVDD10 — VDD10_PHY

AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC

VCC3V3_PHY
PHY_RSTn
GMAC1_MDC
GMAC1_MDIO
GMAC1_TXD3
GMAC1_TXD2
GMAC1_TXD1
GMAC1_TXD0
GMAC1_TXEN
GMAC1_TXCLK

RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial

C6710 3pF C0G 50V C0402 DNP
Close to Pin20

VCC3V3_PHY — R6736 DNP 4.7K R0402 — VCCIO_PHY
R6737 1.8K R0402
GMAC1_RSTn_L — R6738 0R R0402
PHYRSTB is 3.3V IO
C6717 100nF X5R 10V C0402

PHY_RXD0/RXDLY — R6739 22R R0402 — GMAC1_RXD0
PHY_RXD1/TXDLY — R6740 22R R0402 — GMAC1_RXD1
PHY_RXD2/PLLOFF — R6741 22R R0402 — GMAC1_RXD2
PHY_RXD3/PHYAD0 — R6742 22R R0402 — GMAC1_RXD3
PHY_RXCLK/PHYAD1 — R6743 22R R0402 — GMAC1_RXCLK
PHY_RXDV/PHYAD2 — R6744 22R R0402 — GMAC1_RXDV_CRS
C6723 DNP C0402

Close to PHY

R6717 4.7K R0402 — PHY_LED0/CFG_EXT — R6718 DNP 4.7K R0402 — VCC3V3_PHY
R6719 DNP 4.7K R0402 — PHY_LED2/CFG_LDO1 — R6720 4.7K R0402
R6721 4.7K R0402 — PHY_LED1/CFG_LDO0

VCC_PHY0_IO Voltage Config

R6723 DNP 4.7K R0402 — PHY_RXD3/PHYAD0 — R6724 4.7K R0402 — VCCIO_PHY
R6725 4.7K R0402 — PHY_RXCLK/PHYAD1
R6726 4.7K R0402 — PHY_RXDV/PHYAD2

PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

R6727 DNP 4.7K R0402 — PHY_RXD0/RXDLY — R6728 4.7K R0402 — VCCIO_PHY

Pull-up for additional 2ns delay to RXC for data latching

R6729 4.7K R0402 — PHY_RXD1/TXDLY — R6730 DNP 4.7K R0402 — VCCIO_PHY

Pull-up for additional 2ns delay to TXC for data latching

R6732 DNP 4.7K R0402 — PHY_RXD2/PLLOFF — R6733 4.7K R0402 — VCCIO_PHY

Pull-up to disable PLL @ ALDPS mode(Low power mode)

PHY_REG_OUT — L6700 2.2uH IND_303015
C6714 4.7uF X5R 10V C0603
C6715 100nF X5R 10V C0402
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial

VDD10_PHY
C6716 100nF X5R 10V C0402
Close to PIN21

C6720 100nF X5R 10V C0402
C6721 100nF X5R 10V C0402
C6722 100nF X5R 10V C0402
Close to PIN3,8,38

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
External 1.8V(default)	1'b0	2'b10	

PHY_LED2/CFG_LDO1 — C6705 100pF C0G 50V C0402 DNP
PHY_LED1/CFG_LDO0 — C6706 100pF C0G 50V C0402 DNP
Reserve for EMI.

VCC_1V8 — R6731 DNP 0.1R1% R0603 — VCCIO_PHY
VCC_3V3 — R6734 DNP 0.1R1% R0603
C6707 4.7uF 10V X5R C0603
C6708 1uF 10V X5R C0402
C6709 100nF X5R 10V C0402
Close to PIN28

VCC_3V3 — R6735 0.1R1% R0603 — VCC3V3_PHY
C6711 4.7uF X5R 10V C0603
C6712 100nF X5R 10V C0402
C6713 100nF X5R 10V C0402
Close to PIN11,40

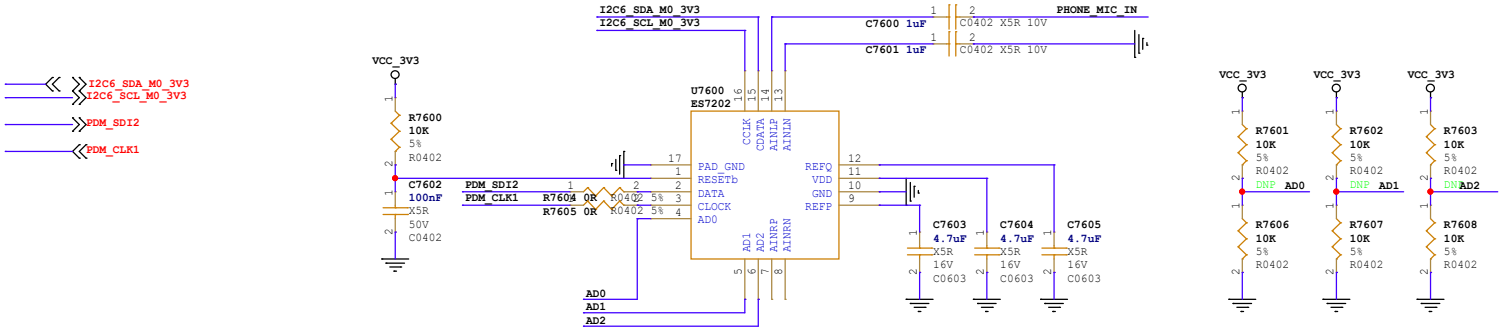
C6718 4.7uF X5R 10V C0603
C6719 100nF X5R 10V C0402
Close to PIN29

Rockchip Confidential

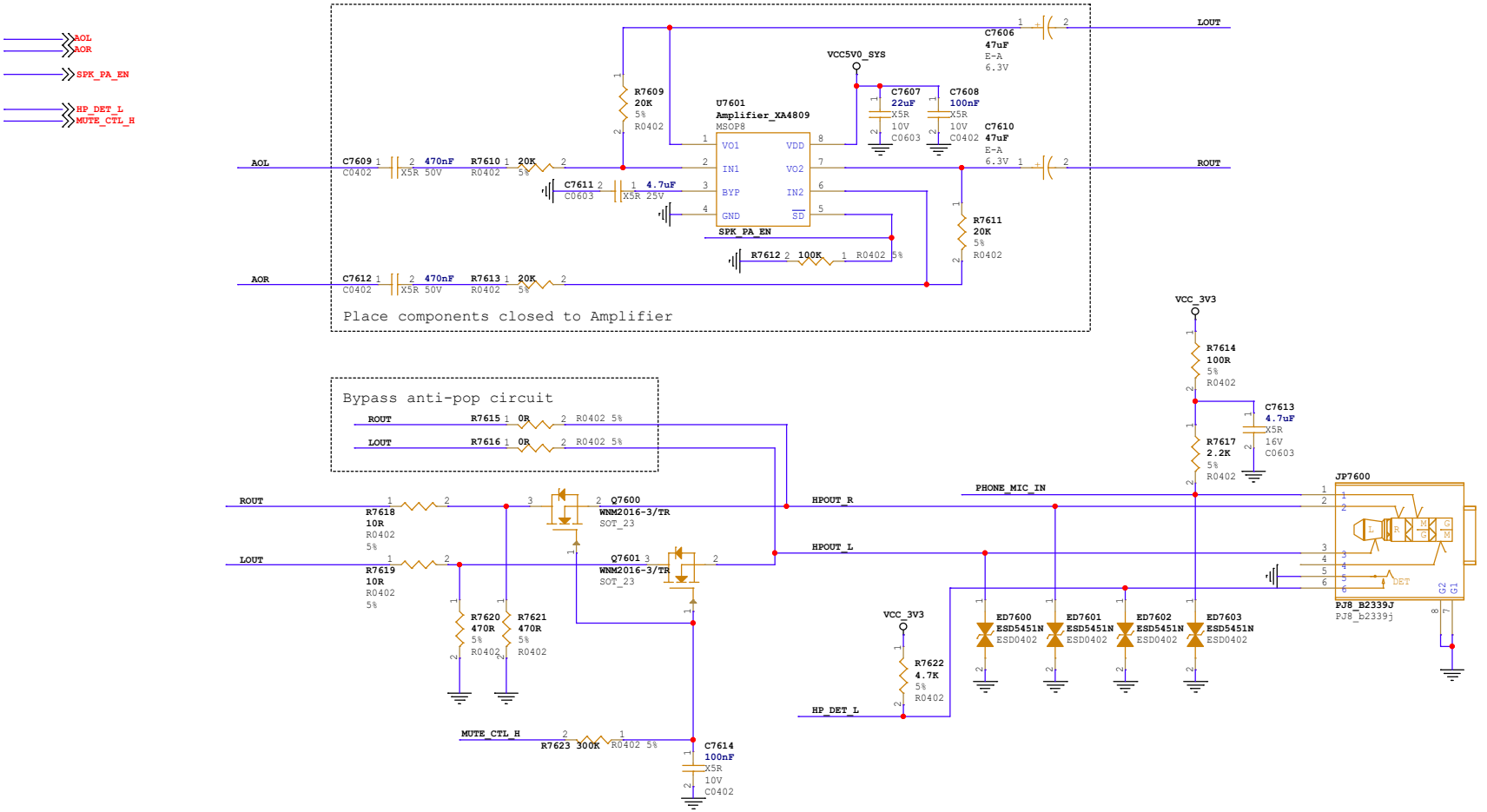
Rockchip Electronics Co., Ltd

Project:	RK3528_REF_SCH				
File:	67.Ethernet-GEPHY_RGMII				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	42 of 50

MICIN

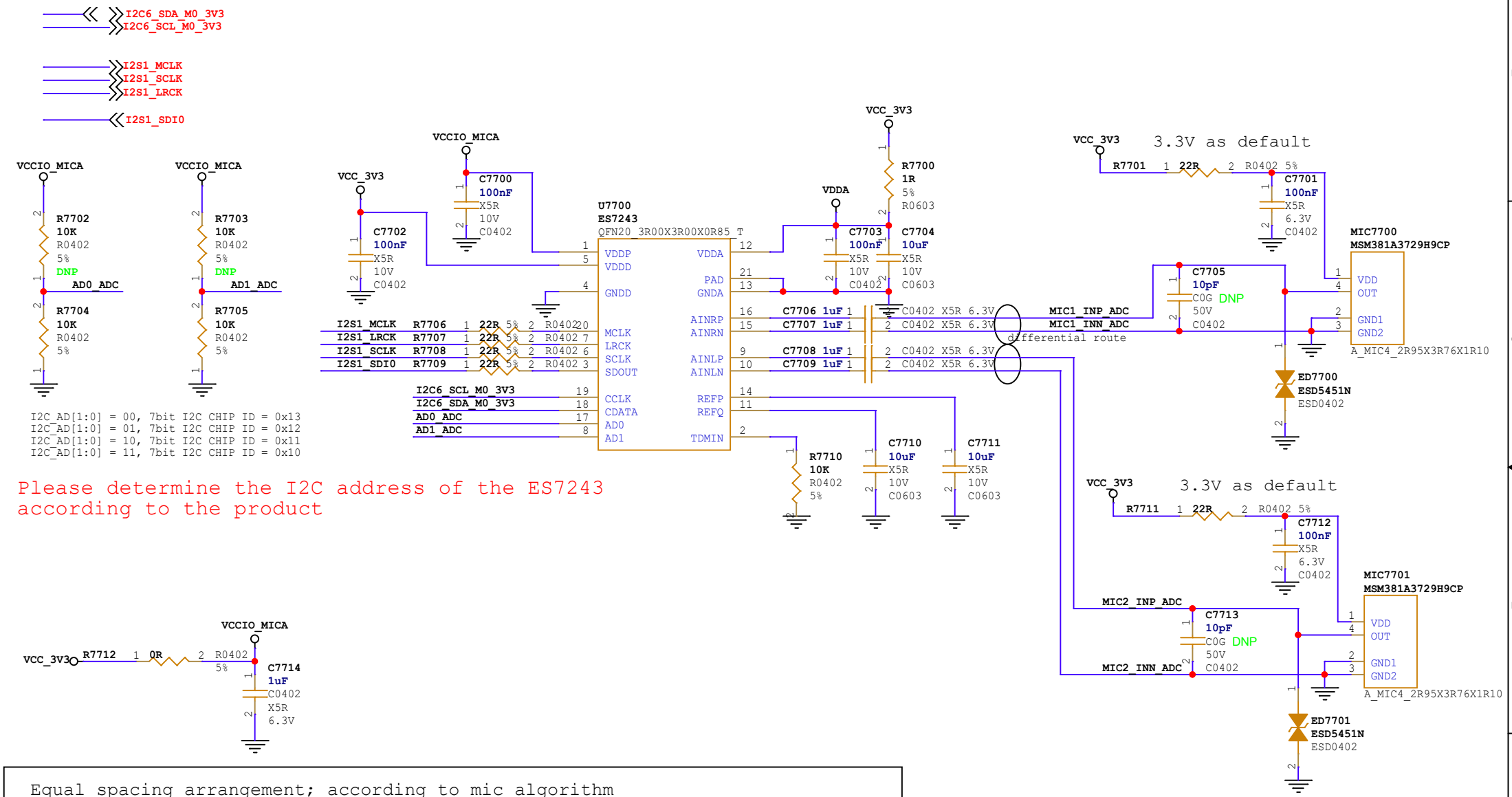


Headphone with Amplifier



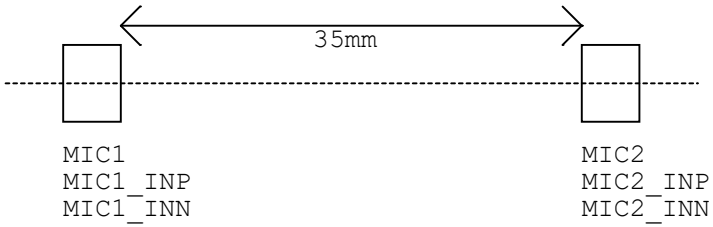
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3528_REF_SCH		
File:	76.Audio-Headphone/MICIN		
Date:	Saturday, May 27, 2023	Rev:	V1.0
Designed by:	HXS	Reviewed by: Default	Sheet: 43 of 50

Audio-MicArray(2xI2S-DMIC)



Please determine the I2C address of the ES7243 according to the product

Equal spacing arrangement; according to mic algorithm

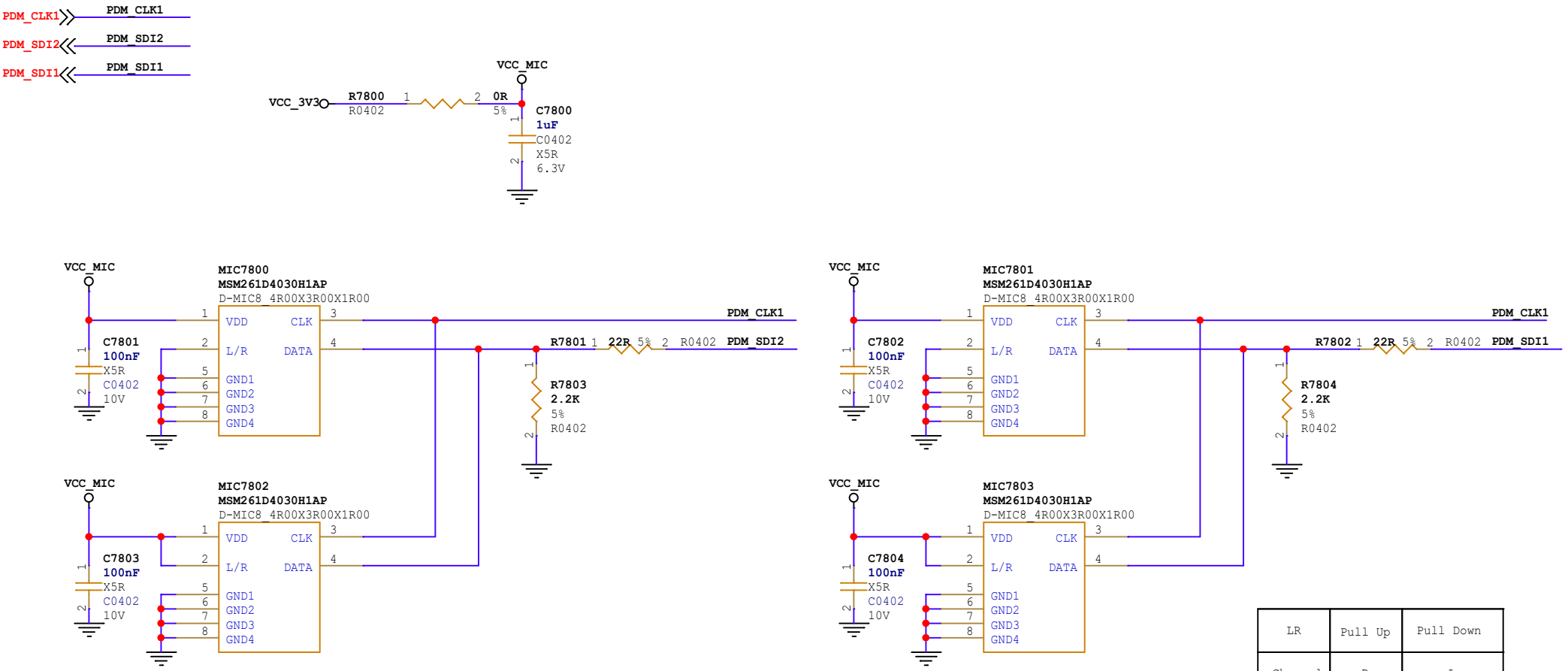


For 2MIC Array Applications

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	77.Audio-MicArray(2xI2S-DMIC)				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	44 of 50

Audio-MicArray(4xPDM-DMIC)

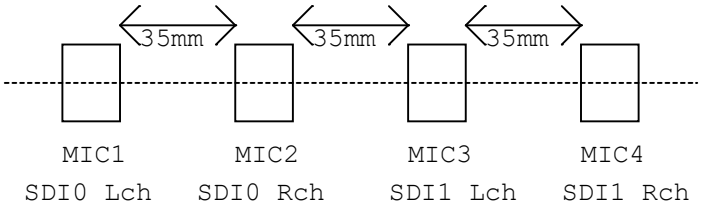


The SDI line should have a 2.2kohm PD resistor to discharge the line during the time that all microphones on the bus have tristated their outputs.

LR	Pull Up	Pull Down
Channel	R	L

Reference the datasheet

Equal spacing arrangement; according to mic algorithm

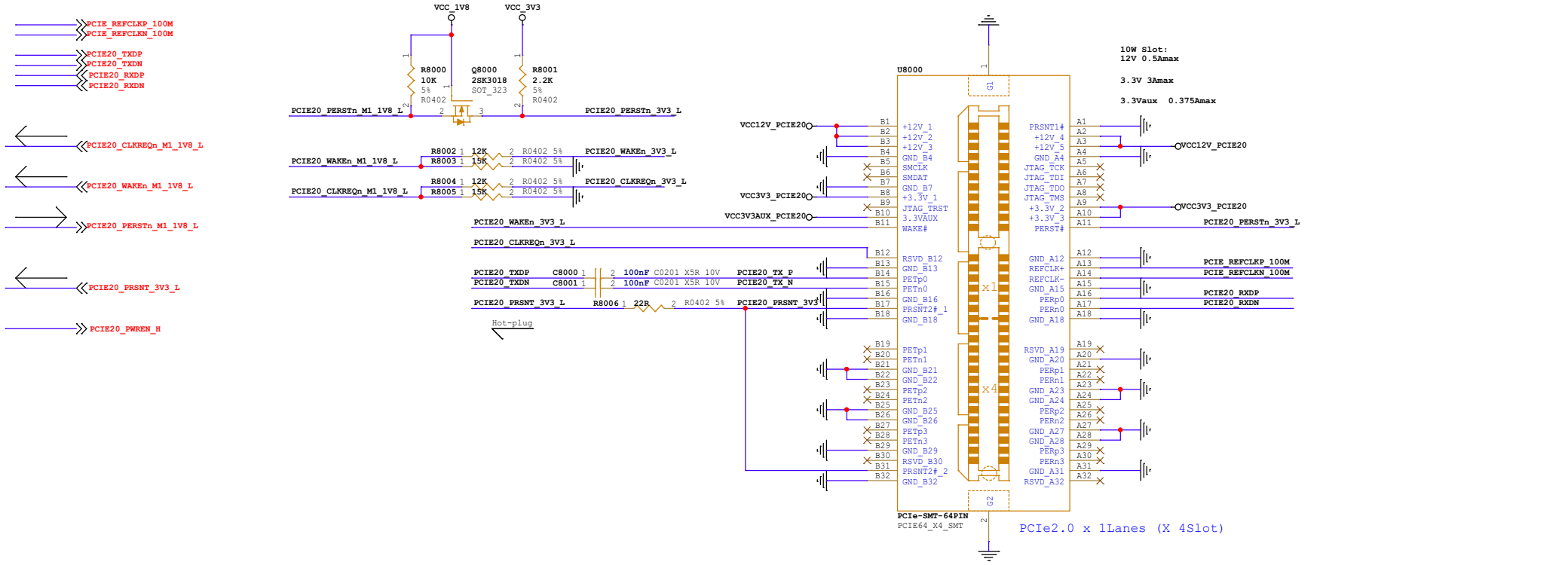


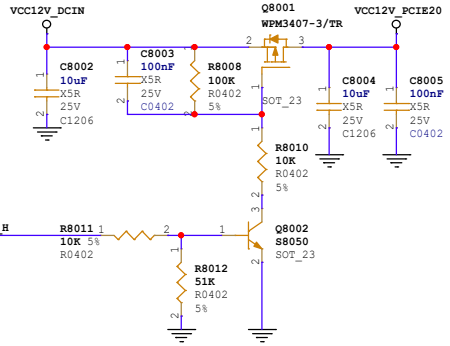
For 4MIC Array Applications

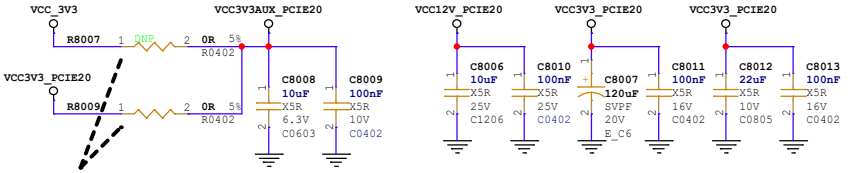
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	78.Audio-MicArray(4xPDM-DMIC)				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	45 of 50

PCIe2.0 x 1Lanes Slot

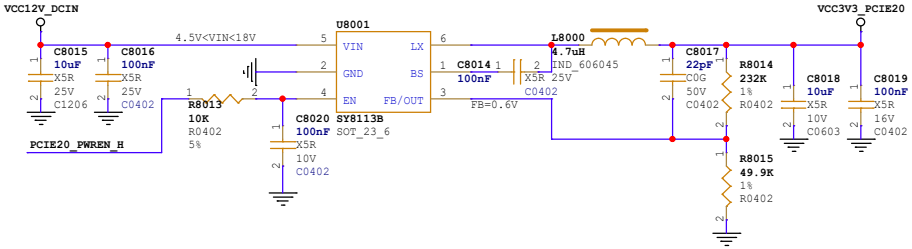






Note:

According to the actual choice of mounted
Cannot be mounted at the same time



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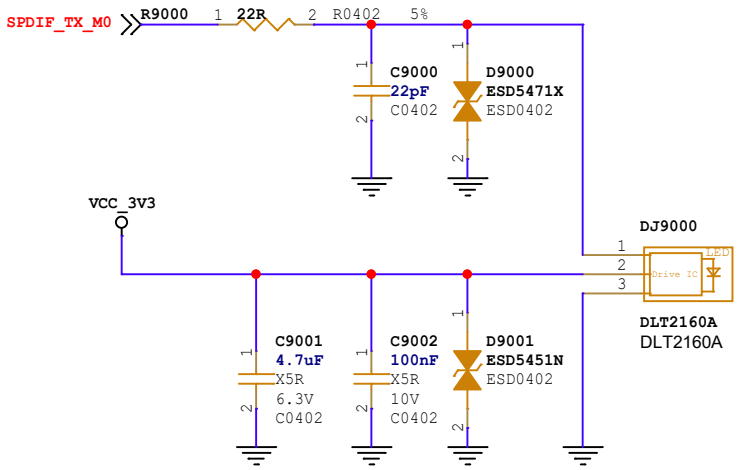
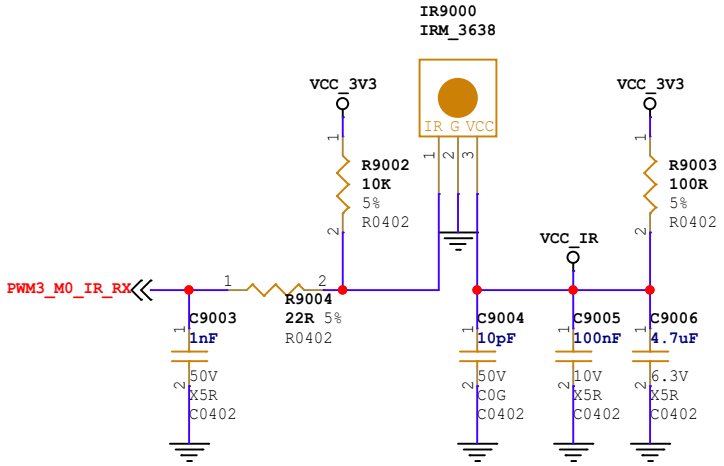
Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	80.PCIE-PCIE2.0_Slot(OPTION)				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	46 of 50

SPDIF



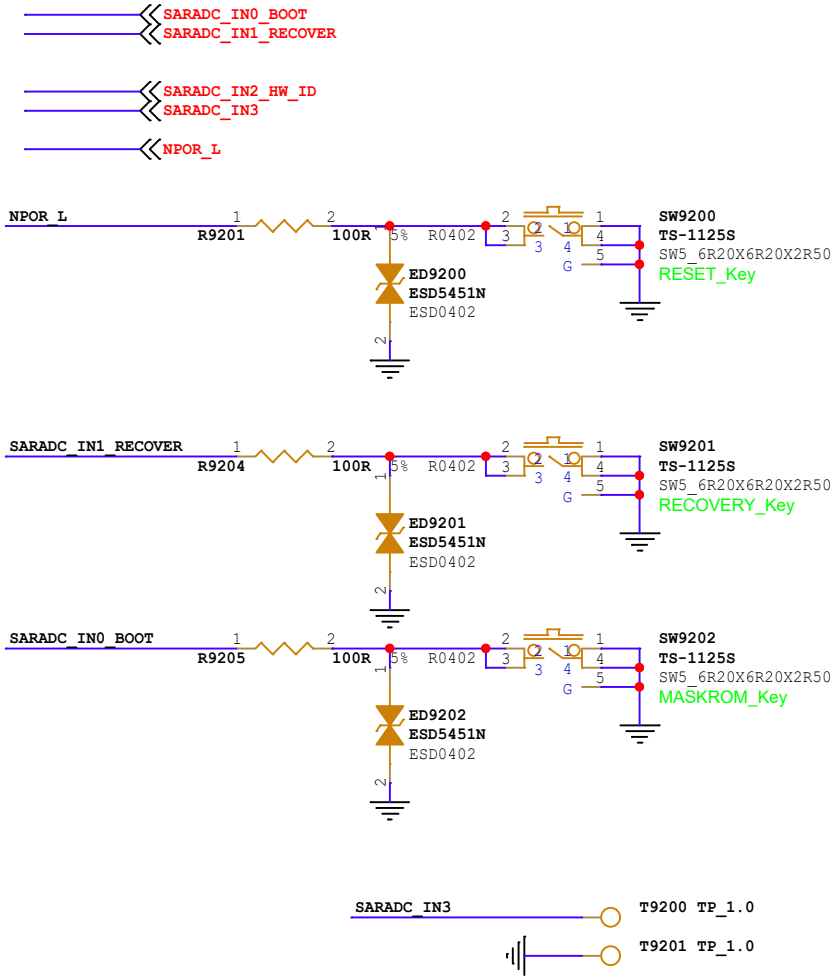
IR Receiver



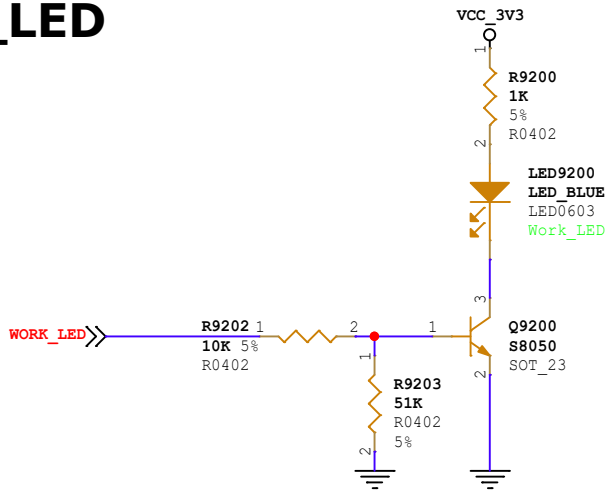
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	90.Spdif TX/IR_RX				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	47 of 50

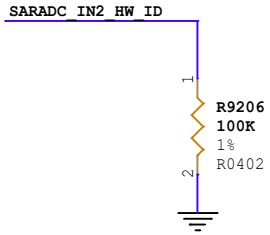
KEY



Work_LED



HW_ID



TABLE

V1.0

SARADC_IN2	Rup	Rdown	ADC
HW_ID0	DNP	100K	0
HW_ID1	100K	12K	114
HW_ID2	100K	27K	228
HW_ID3	100K	51K	342
HW_ID4	100K	82K	456
HW_ID5	100K	120K	570
HW_ID6	100K	200K	683
HW_ID7	100K	330K	796
HW_ID8	100K	820K	910
HW_ID9	100K	DNP	1023

Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	92.Key/HW ID/LED				
Date:	Saturday, May 06, 2023			Rev:	V1.0
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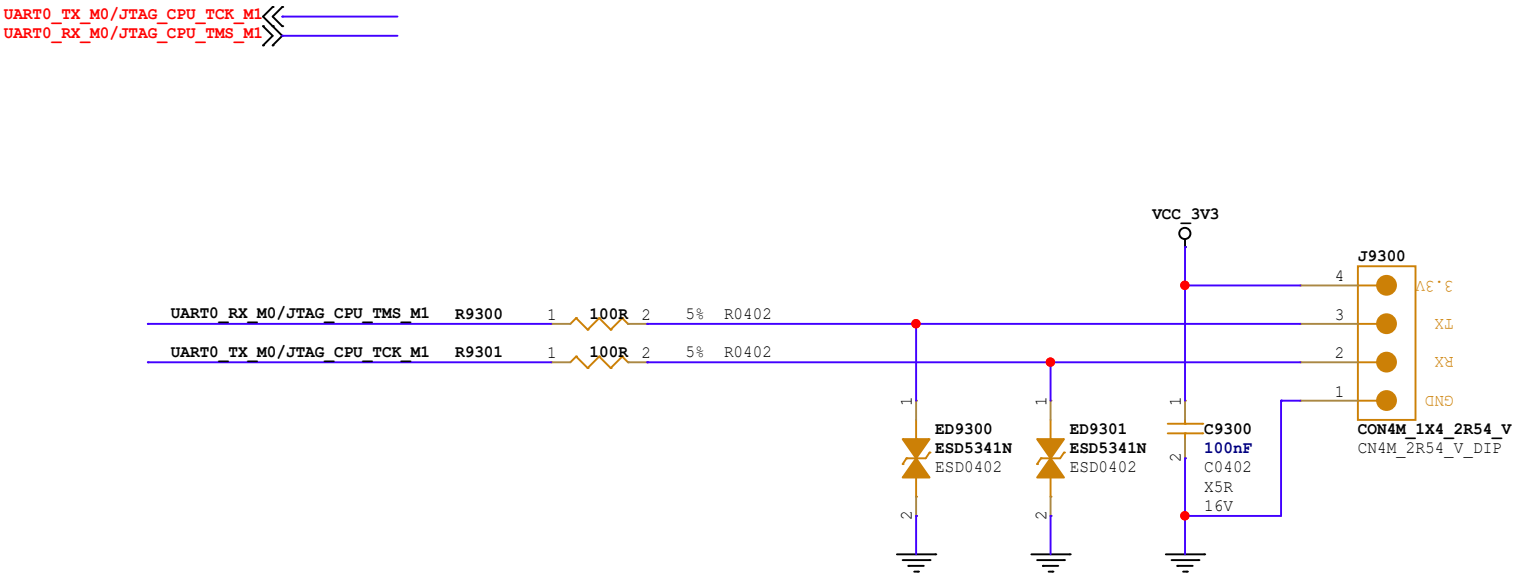
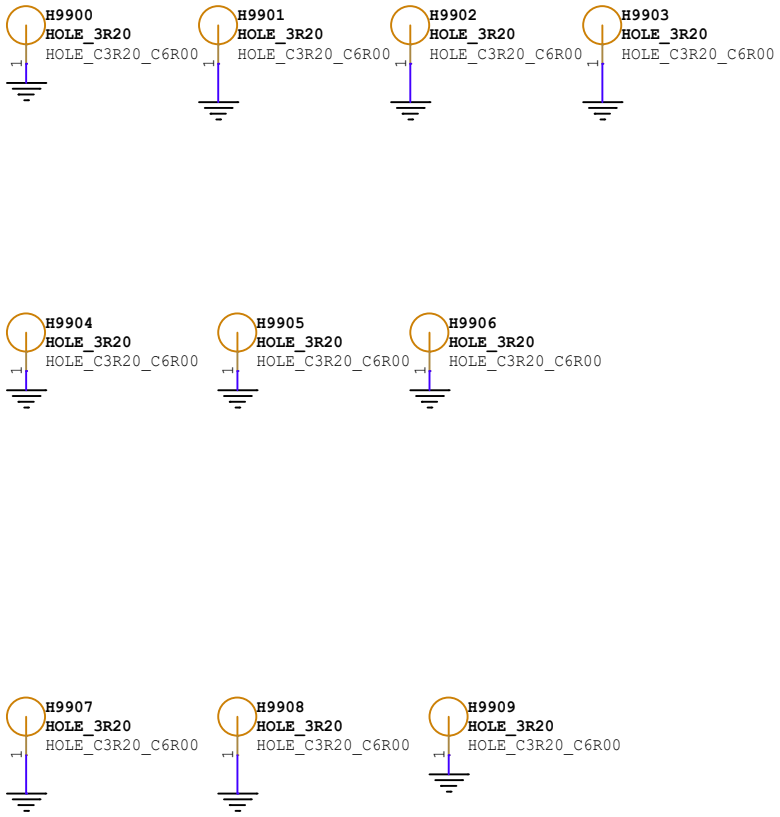
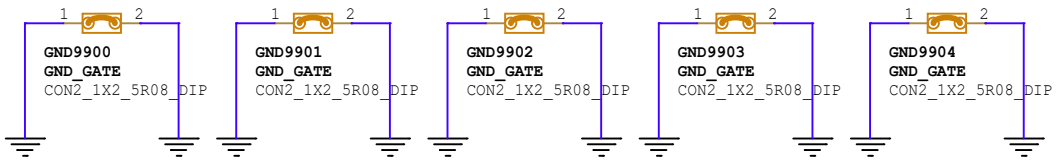
Debug UART0



Rockchip Electronics Co., Ltd					
Project:	RK3528_REF_SCH				
File:	93.Debug UART				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	49 of 50

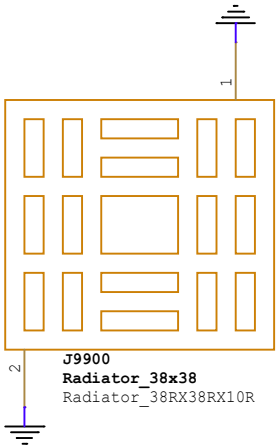


HOLE



Ground GATE(for test)

PCB Mark Point



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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3528_REF_SCH				
File:	99.Mark/Hole/Heatsink				
Date:	Saturday, May 06, 2023			Rev:	V1.0
Designed by:	HXS	Reviewed by:	Default	Sheet:	50 of 50