
STM32
CubeMX

1. Description

1.1. Project

Project Name	stock_price
Board Name	NUCLEO-H743ZI2
Generated with:	STM32CubeMX 6.6.1
Date	09/26/2022

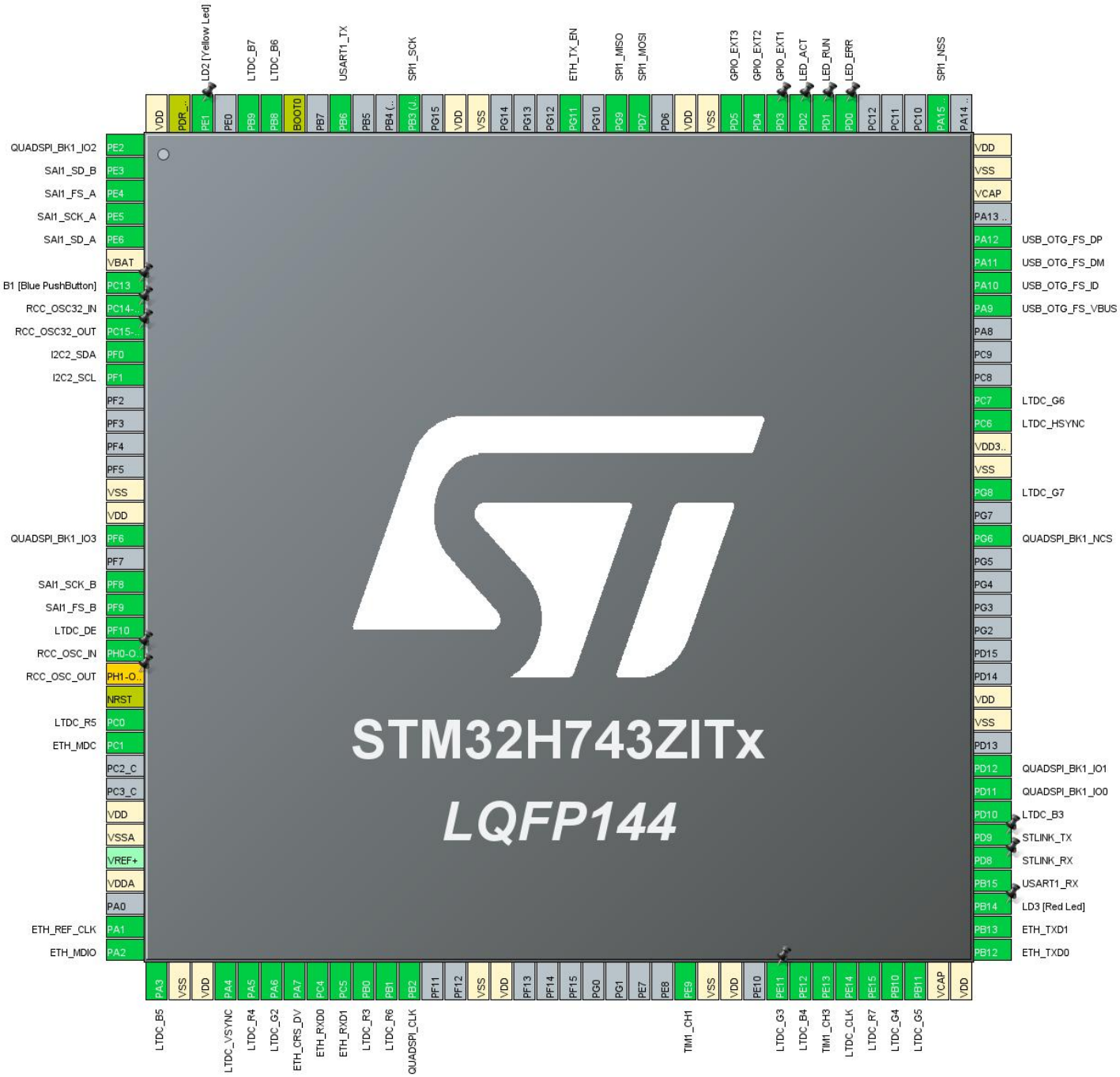
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	QUADSPI_BK1_IO2	
2	PE3	I/O	SAI1_SD_B	
3	PE4	I/O	SAI1_FS_A	
4	PE5	I/O	SAI1_SCK_A	
5	PE6	I/O	SAI1_SD_A	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	B1 [Blue PushButton]
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	QUADSPI_BK1_IO3	
20	PF8	I/O	SAI1_SCK_B	
21	PF9	I/O	SAI1_FS_B	
22	PF10	I/O	LTDC_DE	
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1) **	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	LTDC_R5	
27	PC1	I/O	ETH_MDC	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
37	PA3	I/O	LTDC_B5	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	LTDC_VSYNC	
41	PA5	I/O	LTDC_R4	
42	PA6	I/O	LTDC_G2	
43	PA7	I/O	ETH_CRS_DV	

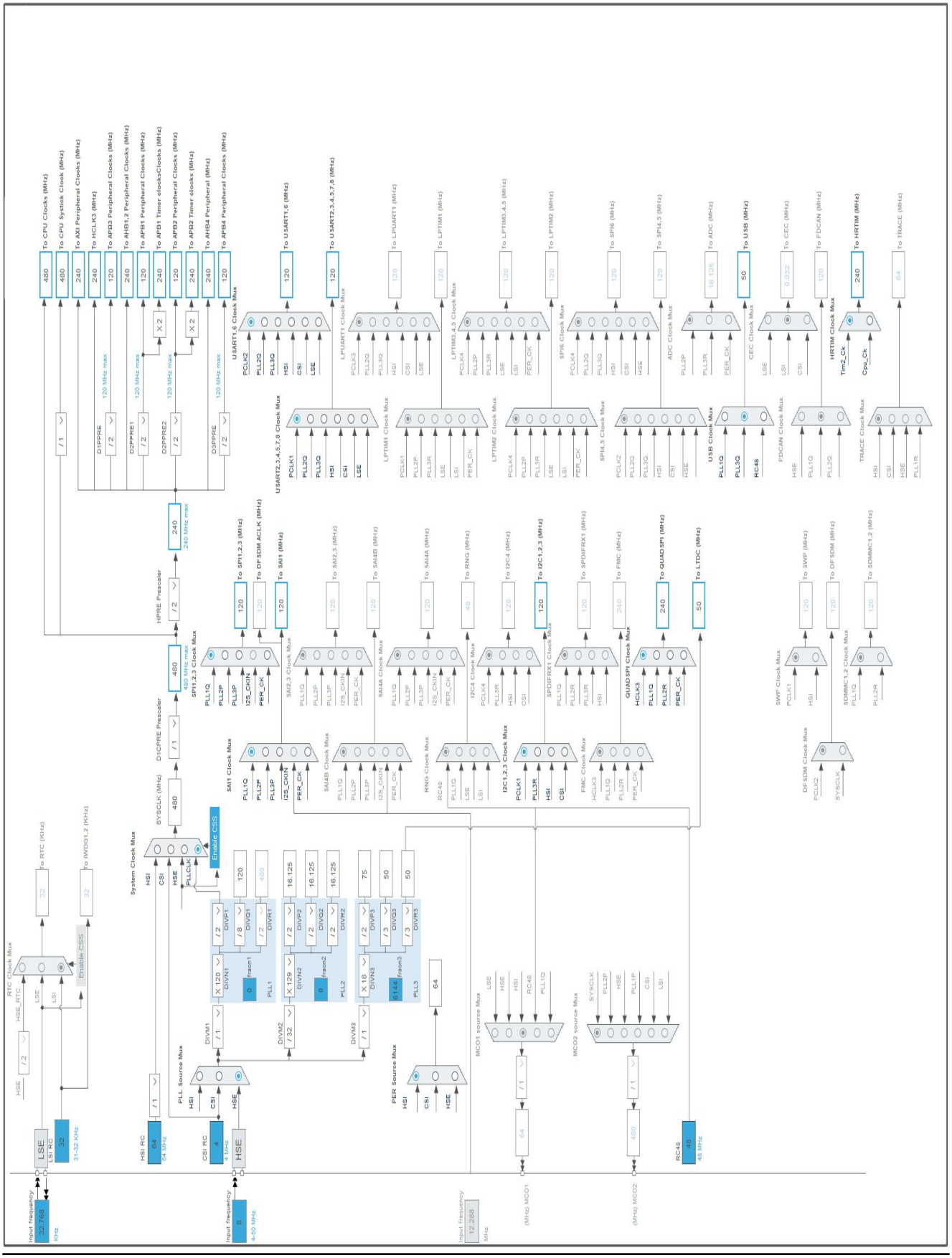
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
46	PB0	I/O	LTDC_R3	
47	PB1	I/O	LTDC_R6	
48	PB2	I/O	QUADSPI_CLK	
51	VSS	Power		
52	VDD	Power		
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	LTDC_G3	
65	PE12	I/O	LTDC_B4	
66	PE13	I/O	TIM1_CH3	
67	PE14	I/O	LTDC_CLK	
68	PE15	I/O	LTDC_R7	
69	PB10	I/O	LTDC_G4	
70	PB11	I/O	LTDC_G5	
71	VCAP	Power		
72	VDD	Power		
73	PB12	I/O	ETH_TXD0	
74	PB13	I/O	ETH_TXD1	
75	PB14 *	I/O	GPIO_Output	LD3 [Red Led]
76	PB15	I/O	USART1_RX	
77	PD8	I/O	USART3_TX	STLINK_RX
78	PD9	I/O	USART3_RX	STLINK_TX
79	PD10	I/O	LTDC_B3	
80	PD11	I/O	QUADSPI_BK1_IO0	
81	PD12	I/O	QUADSPI_BK1_IO1	
83	VSS	Power		
84	VDD	Power		
91	PG6	I/O	QUADSPI_BK1_NCS	
93	PG8	I/O	LTDC_G7	
94	VSS	Power		
95	VDD33_USB	Power		
96	PC6	I/O	LTDC_HSYNC	
97	PC7	I/O	LTDC_G6	
101	PA9	I/O	USB_OTG_FS_VBUS	
102	PA10	I/O	USB_OTG_FS_ID	
103	PA11	I/O	USB_OTG_FS_DM	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
104	PA12	I/O	USB_OTG_FS_DP	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
110	PA15 (JTDI)	I/O	SPI1_NSS	
114	PD0 *	I/O	GPIO_Output	LED_ERR
115	PD1 *	I/O	GPIO_Output	LED_RUN
116	PD2 *	I/O	GPIO_Output	LED_ACT
117	PD3 *	I/O	GPIO_Output	GPIO_EXT1
118	PD4 *	I/O	GPIO_Output	GPIO_EXT2
119	PD5 *	I/O	GPIO_Output	GPIO_EXT3
120	VSS	Power		
121	VDD	Power		
123	PD7	I/O	SPI1_MOSI	
124	PG9	I/O	SPI1_MISO	
126	PG11	I/O	ETH_TX_EN	
130	VSS	Power		
131	VDD	Power		
133	PB3 (JTDO/TRACESWO)	I/O	SPI1_SCK	
136	PB6	I/O	USART1_TX	
138	BOOT0	Boot		
139	PB8	I/O	LTDC_B6	
140	PB9	I/O	LTDC_B7	
142	PE1 *	I/O	GPIO_Output	LD2 [Yellow Led]
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stock_price
Project Folder	C:\Jeonghyun\coding\hangangview-circuit
Toolchain / IDE	EWARM V8.50
Firmware Package Name and Version	STM32Cube FW_H7 V1.10.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA2D_Init	DMA2D
4	MX_LTDC_Init	LTDC
5	MX_USART3_UART_Init	USART3
6	MX_JPEG_Init	JPEG
7	MX_LWIP_Init	LWIP
8	MX_HRTIM_Init	HRTIM
9	MX_I2C2_Init	I2C2
10	MX_SAI1_Init	SAI1
11	MX_SPI1_Init	SPI1

Rank	Function Name	Peripheral Instance Name
12	MX_TIM1_Init	TIM1
13	MX_USART1_UART_Init	USART1
14	MX_USB_OTG_FS_USB_Init	USB_OTG_FS
15	MX_QUADSPI_Init	QUADSPI

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

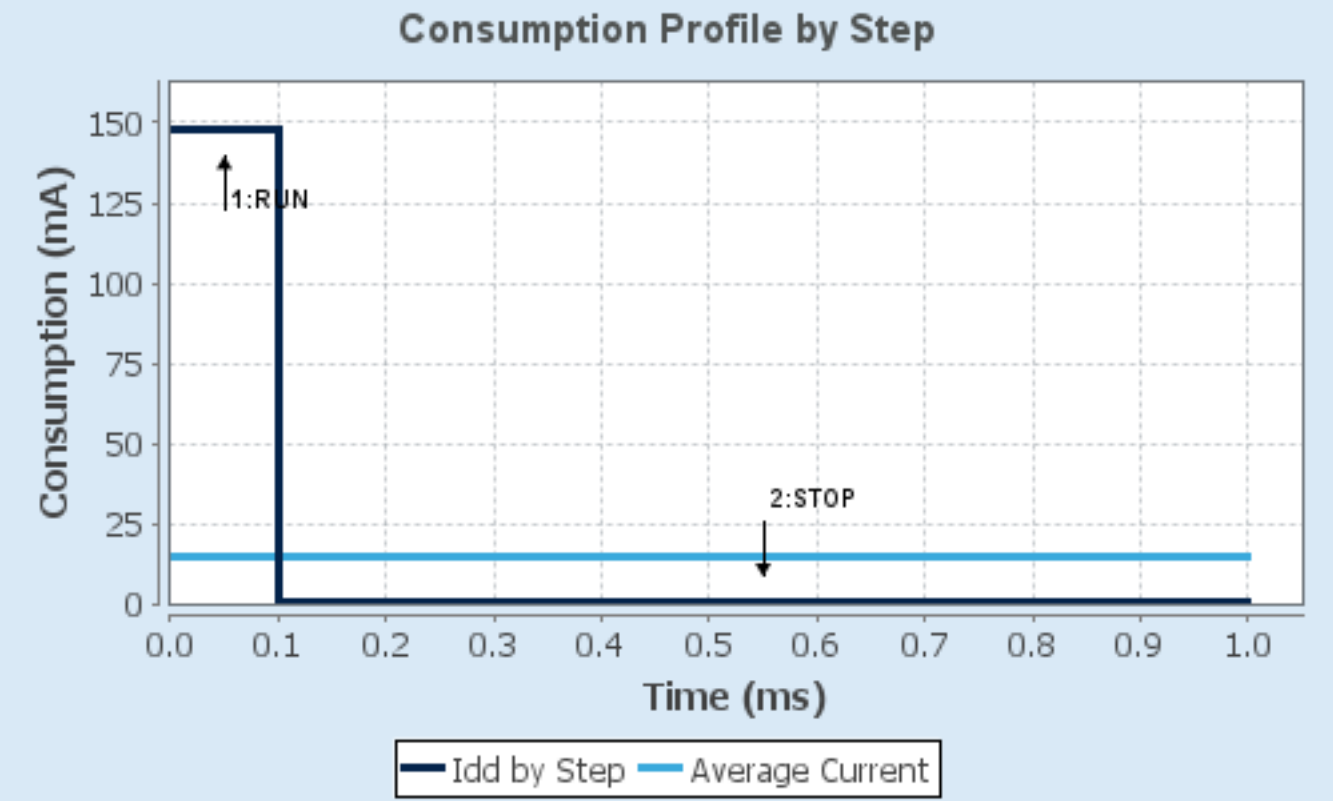
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.46	124.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. DMA2D

mode: Activated

7.1.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	**RGB565 ***
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	RGB565
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)
DMA2D Chroma Sub-Sampling Mode	No chroma sub-sampling 4:4:4

7.2. ETH

Mode: RMII

7.2.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30000200 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30000000 ***
Rx Buffers Address	**0x30000260 ***
Rx Buffers Length	1536

7.3. HRTIM

mode: Master Timer Enable

Timer A: No external Output

7.3.1. HRTIM Interrupt Configuration:

Sources:

1st Source of interrupt	No interrupt enabled
2nd Source of interrupt	No interrupt enabled
3rd Source of interrupt	No interrupt enabled
4th Source of interrupt	No interrupt enabled
5th Source of interrupt	No interrupt enabled
6th Source of interrupt	No interrupt enabled
7th Source of interrupt	No interrupt enabled
8th Source of interrupt	No interrupt enabled

7.3.2. Synchro Configuration:

Master Timer Synchronization:

Sync Options	HRTIM instance doesn't handle external synchronization signals (SYNCIN, SYNCOUT)

7.3.3. External Event Configuration:

External Event 1:

Event Configuration	Disable

External Event 2:

Event Configuration	Disable

External Event 3:

Event Configuration	Disable

External Event 4:

Event Configuration	Disable

External Event 5:

Event Configuration	Disable

External Event 6:

Event Configuration	Disable

External Event 7:

Event Configuration	Disable

External Event 8:

Event Configuration	Disable

External Event 9:

Event Configuration	Disable

External Event 10:

Event Configuration	Disable

7.3.4. Fault Lines Configuration:

Fault Line 1:

Line Configuration	No Configuration of Fault Line

Fault Line 2:

Line Configuration	No Configuration of Fault Line

Fault Line 3:

Line Configuration	No Configuration of Fault Line

Fault Line 4:

Line Configuration	No Configuration of Fault Line

Fault Line 5:

Line Configuration	No Configuration of Fault Line

7.3.5. ADC Triggers Configuration:

ADC Trigger 1:

ADC Trigger Configuration	Disable

ADC Trigger 2:

ADC Trigger Configuration	Disable

ADC Trigger 3:

ADC Trigger Configuration	Disable

ADC Trigger 4:

ADC Trigger Configuration	Disable

7.3.6. Burst Mode Configuration:

Burst Mode Enabling:

Burst Mode	Burst mode disabled

7.3.7. Master Timer:

General:

Timer Idx	Master Timer

Time Base Setting:

Prescaler Ratio	HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value =

	400MHz)
fHRCK Equivalent Frequency	2.4E8
Period	**0xFFFD ***
Resulting PWM Frequency	3662
Repetition Counter	**0x00 ***
Mode	The timer operates in continuous (free-running) mode

Timing Unit:

Half Mode Enable - The Compare Value of CP Unit 1 is set automatically to half the Timer Period -	Half mode is disabled
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	Preload disabled: the write access is directly done into the active register
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition disabled
Burst Mode	Timer counter clock is maintained and the timer operates normally
Interrupt Requests Sources Selection : Please enter the number of Active Interrupt Requests	0
Number of Master Timer Internal DMA Request Sources - you first have to enable the Master Timer DMA Request in the DMA Settings Tab	0

Compare Unit 1:

Compare Unit 1 Configuration	Disable

Compare Unit 2:

Compare Unit 2 Configuration	Disable

Compare Unit 3:

Compare Unit 3 Configuration	Disable

Compare Unit 4:

Compare Unit 4 Configuration	Disable

Burst DMA Controller:

Burst DMA Configuration	Disable

7.3.8. Timer A:

General:

Timer Idx	Timer A
Basic/Advanced Configuration	Advanced (using HAL_Waveform methods)

Time Base Setting:

Prescaler Ratio	HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value = 400MHz)
fHRCK Equivalent Frequency	2.4E8

Period	**0xFFFD ***
Resulting PWM Frequency	3662
Repetition Counter	**0x00 ***
Mode	The timer operates in continuous (free-running) mode

Timing Unit:

Half Mode Enable - The Compare Value of CP Unit 1 is set automatically to half the Timer Period -	Half mode is disabled
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	Preload disabled: the write access is directly done into the active register
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition disabled
Burst Mode	Timer counter clock is maintained and the timer operates normally
Push Pull	Push-Pull mode disabled
Number of Faults to enable	0
Fault Lock	Timer fault enabling bits are read/write
Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the number of Triggers to select	0
Reset Update	Update by Timer reset / roll-over disabled
Reset Trigger Sources Selection : Please enter the number of Triggers to select	0
Interrupt Requests Sources Selection : Please enter the number of Active Interrupt Requests	0
Number of Timer A Internal DMA Request Sources - you first have to enable the Timer A DMA Request in the DMA Settings Tab	0

Compare Unit 1:

Compare Unit 1 Configuration	Disable

Compare Unit 2:

Compare Unit 2 Configuration	Disable

Compare Unit 3:

Compare Unit 3 Configuration	Disable

Compare Unit 4:

Compare Unit 4 Configuration	Disable

Burst DMA Controller:

Burst DMA Configuration	Disable

Capture Unit 1:

Capture Unit 1 Configuration	Disable

Capture Unit 2:

Capture Unit 2 Configuration	Disable

External Event 1 Filtering:

Filtering Configuration	Disable

External Event 2 Filtering:

Filtering Configuration	Disable

External Event 3 Filtering:

Filtering Configuration	Disable

External Event 4 Filtering:

Filtering Configuration	Disable

External Event 5 Filtering:

Filtering Configuration	Disable

External Event 6 Filtering:

Filtering Configuration	Disable

External Event 7 Filtering:

Filtering Configuration	Disable

External Event 8 Filtering:

Filtering Configuration	Disable

External Event 9 Filtering:

Filtering Configuration	Disable

External Event 10 Filtering:

Filtering Configuration	Disable

7.4. I2C2

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled

Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. JPEG

mode: Activated

7.5.1. Parameter Settings:

Version:

JPEG version	jpeg1_v1_0

JPEG Software options:

ENCODE	**Disabled ***
DECODE	Enabled
RGB_FORMAT	**JPEG_RGB565 ***
JPEG_SWAP_RG	0

7.6. LTDC

Display Type: RGB565 (16 bits)

7.6.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485

Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

7.6.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

Number of Layers:

Number of Layers	2 layers

7.7. PWR

Power Voltage Detector In: Power Voltage Detector In (Internal analog voltage)

7.7.1. Parameter Settings:

Programmable_Voltage_Detector_Settings:

PVD detection Level	**PWR PVD LEVEL 6 (2.85 V) ***
PWR PVD Mode	basic mode is used

7.8. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.8.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.9. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.9.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)
Product revision	rev.Y

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL3 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL3 clock Output range	MEDIUM VCO range

7.10. SAI1

Mode: Master

mode: I2S/PCM Protocol

Mode: Master

mode: I2S/PCM Protocol

mode: External Synchro Out

7.10.1. Parameter Settings:

SAI A:

Synchronization Inputs	Asynchronous
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven

Protocol Parameters	
Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2
Clock Source	SAI PLL Clock
Master Clock No Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	**234.375 KHz ***
Error between Selected	**22.07 % ***
Fifo Threshold	Empty
Output Drive	Disabled

SAI B:

Synchronization Inputs	Asynchronous
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2
Clock Source	SAI PLL Clock
Master Clock No Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	**234.375 KHz ***
Error between Selected	**22.07 % ***
Fifo Threshold	Empty
Output Drive	Disabled

Advanced Parameters:

Synchronization External	Disabled

7.11. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits

First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**60.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.12. SYS

Timebase Source: SysTick

7.13. TIM1

Channel1: PWM Generation CH1

Channel3: PWM Generation CH3

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.14. USART1

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.15. USART3

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. USB_OTG_FS

Mode: OTG/Dual_Role_Device

Activate_VBUS: VBUS sensing

7.17. FREERTOS

Interface: CMSIS_V2

7.17.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16

USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

7.17.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.17.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.18. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.18.1. General Settings:

LwIP Version:	
LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2
IPv4 - DHCP Options:	
LWIP_DHCP (DHCP Module)	Enabled
RTOS Dependency:	
WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled
CMSIS_VERSION (CMSIS API Version used)	CMSIS v2
Platform Settings:	
PHY Driver	Choose/LAN8742
Protocols Options:	
LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.18.2. Key Options:

Infrastructure - OS Awarness Option:	
NO_SYS (OS Awarness)	OS Used
Infrastructure - Timers Options:	
LWIP_TIMERS (Use Support For sys_timeout)	Enabled
Infrastructure - Core Locking and MPU Options:	
SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled
Infrastructure - Heap and Memory Pools Options:	
MEM_SIZE (Heap Memory Size)	1600
LWIP_RAM_HEAP_POINTER (RAM Heap Pointer)	**0x30044000 ***
Infrastructure - Internal Memory Pool Sizes:	
MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16

MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	24
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0
LWIP_SOCKET_SELECT (Select for Socket)	Enabled
LWIP_SOCKET_POLL (Poll for Socket)	Enabled

7.18.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.18.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.18.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

7.18.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.18.7. SNTP/SMTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)	Disabled

7.18.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.18.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.18.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.18.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Enabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Enabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.18.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
LTDC	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC0	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA5	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD10	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG8	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF6	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
SAI1	PE3	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF8	SAI1_SCK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	SAI1_FS_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI1	PA15 (JTDI)	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG9	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3 (JTDO/TRACESWO)	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_RX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_TX
USB_OTG_FS	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Signals	(PH1)					
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red Led]
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_ERR
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RUN
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_ACT
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_EXT1
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_EXT2
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_EXT3
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Yellow Led]

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
USART1 global interrupt	unused		
USART3 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FPU global interrupt	unused		
SAI1 global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		
QUADSPI global interrupt	unused		
HRTIM master timer global interrupt	unused		
HRTIM timer A global interrupt	unused		
HRTIM fault global interrupt	unused		
JPEG global interrupt	unused		
HSEM1 global interrupt	unused		

8.5.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler

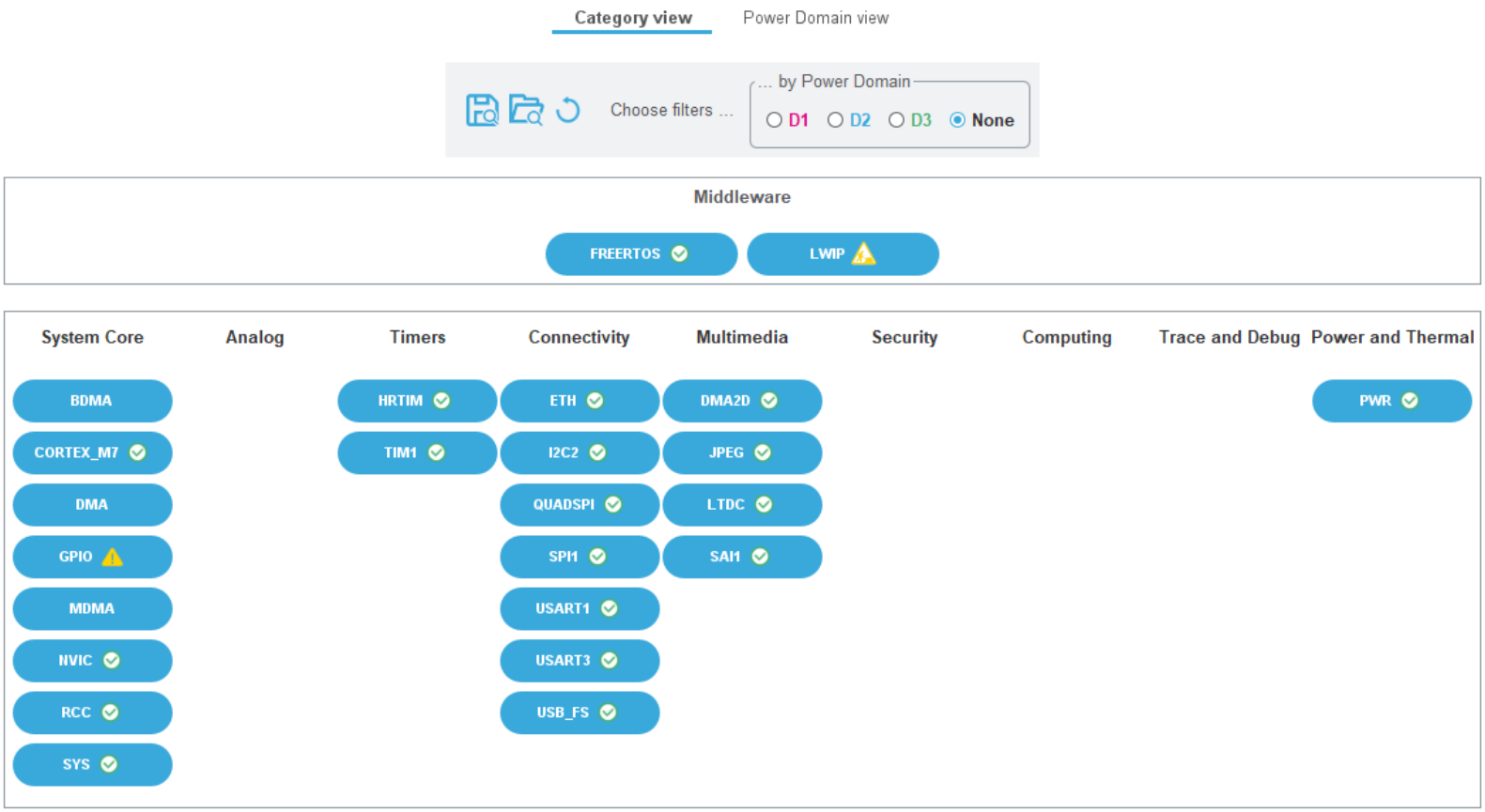
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	true	true

*** User modified value**

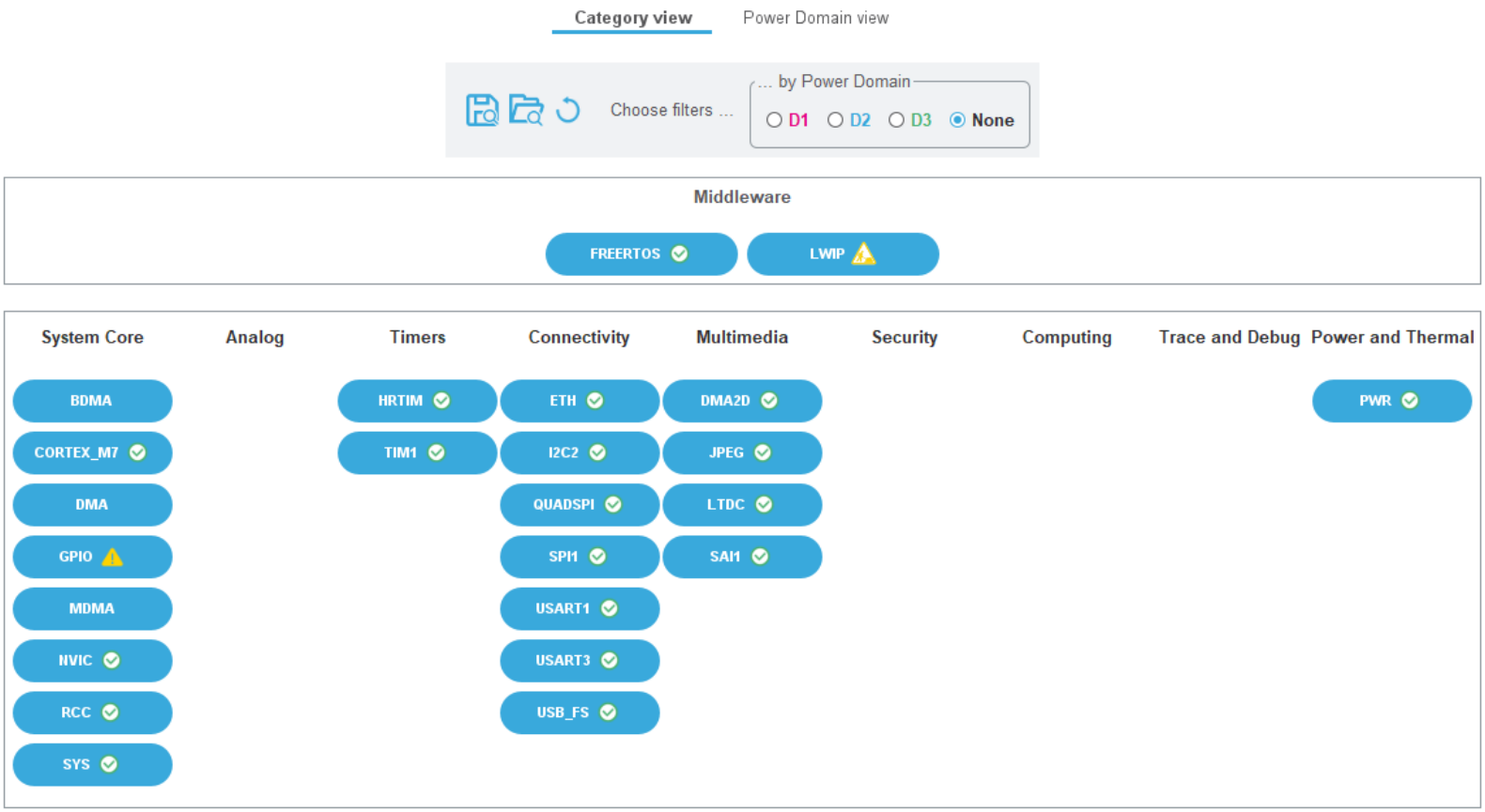
9. System Views

9.1. Category view

9.1.1. Current



9.1.2. Without filters



9.2. Power Domain view

10. Docs & Resources

Type	Link
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Training Material	https://www.st.com/resource/en/sales_guide/sg_sc2154.pdf
Training Material	https://www.st.com/resource/en/training_certification/faecp_stm32h7_dualcore_edr.pdf
Training Material	https://www.st.com/resource/en/training_certification/faecp_stm32h7_edr.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7vl.pdf
Flyers	https://www.st.com/resource/en/flyer/flnucleolrwan.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers	https://www.st.com/resource/en/flyer/flpowerstbd.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-

	and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2834-how-to-get-the-best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4230-stm32-microcontroller-random-number-generation-validation-using-the-nist-statistical-test-suite-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-

	applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4838-managing-memory-protection-unit-in-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4861-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
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