Version 0.2.b

DISCLAIMER

SMIC hereby provides the quality information but makes no claims, rompises or guarantees about the accuracy, completeness, or adequacy of the information herein. The information contained herein is provided on an "AS IS" basis without any warranty, and SMIC assumes no obligation to provide support of any kind or otherwise maintain the information. SMIC disclaims any representation that the information does not infringe any intellectual property rights or proprietary rights of any third parties. SMIC makes no other warranty, whether express, implied or statutory as to any matter whatsoever, including but not limited to the accuracy or sufficiency of any information or the merchantability and fitness for a particular purpose. Neither SMIC nor any of its representatives shall be liable for any cause of action incurred to connect to this service.

STATEMENT OF USE AND CONFIDENTIALITY

The following/attached material contains confidential and proprietary information of SMIC. This material is based upon information which SMIC considers reliable, but SMIC neither represents nor warrants that such information is accurate or complete, and it must not be relied upon as such. This information was prepared for informational purposes and is for the use by SMIC's customer only. SMIC reserves the right to make changes in the information at any time without notice. No part of this information may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any human or computer language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual, or otherwise, without the prior written consent of SMIC. Any unauthorized use or disclosure of this material is strictly prohibited and may be unlawful. By accepting this material, the receiving party shall be deemed to have acknowledged, accepted, and agreed to be bound by the foregoing limitations and restrictions.Thank you.

OVERVIEW

The 2-PORT Register File is designed for SMIC's 0.18um CMOS Logic process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.62V to 1.98V and a temperature range of -40°C to 125°C.

Chip enable (CENA,CENB), address (AA[i-1:0],AB[i-1:0]) and data in (DB[n-1:0]) signals are latched on the rising-edge of the clock. When CENA is low, the memory is in read-mode. Data is read from the memory location specified on the address bus AA[i-1:0] and appears on the data output bus QA[n-1:0].When CENB is low, the memory is in write-mode. The word on the data port DB[n-1:0] will be written into the location specified by the address AB[i-1:0] and the data will appear on the output port QA[n-1:0].When CENA is high, port A enters the standby mode. Data outputs remained stable.When CENB is high, port B enters the standby mode. Data stored in the memory is retained, but the new data writes is not allowed.

CONFIGURATION:

PARAMETER	VALUE
Mux	4
Words	64
Bits	24
Width	659.38um
Height	76.2um
Area	50244.756um^2

PIN DEFINITION:

PIN	DIRECTION	DEFINITION
AA[5:0]	Input	A Port Address Inputs
AB[5:0]	Input	B Port Address Inputs
DB[23:0]	Input	B Port Data Inputs
CENA	Input	A Port Enable
CENB	Input	B Port Enable
CLKA	Input	A Port Clock Input
CLKB	Input	B Port Clock Input
QA[23:0]	Output	Data Outputs

TIMING:

PARAMETER	DESCRIPTION	FF CORNER 1.98V, -40°C		FF CORNER 1.98V, 0°C		FF CORNER 1.98V, 125°C		SS CORNER 1.62V, -40°C		SS CORNER 1.62V, 125°C		TT CORNER 1.8V, 25°C	
(ns)		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Tcyc	Cycle Time	1.176		1.264		1.505		2.718		3.308		1.807	
Ta	[1]Access Time	0.562		0.605		0.720			2.059		2.506		1.369
Tah	Address Hold	0.333		0.363		0.433		0.612		0.744		0.534	
Tas	Address Setup	0.592		0.617		0.692		1.125		1.293		0.789	
Tch	Cen Hold	0.100		0.100		0.100		0.100		0.100		0.100	
Tcs	Cen Setup	0.460		0.469		0.495		0.603		0.658		0.526	
Tdh	Data Hold	0.114		0.112		0.118		0.185		0.199		0.171	
Tds	Data Setup	0.338		0.389		0.467		0.808		0.977		0.509	
Tclkh	Clock High	0.050		0.060		0.060		0.060		0.080		0.070	
Tclkl	Clock Low	0.200		0.220		0.240		0.210		0.260		0.290	
Tclkr	Clock Rise Skew	1.500		1.500		1.500		3.000		3.000		2.000	
Tcc	Clock Collision	1.176		1.264		1.505		2.718		3.308		1.807	

Timing simulation conditions:

1. Access time = best case for fast corner and worst case for slow/typical corners

POWER:

| PARAMETER	FF CORNER 1.98V, -40°C	FF CORNER 1.98V, 0°C	FF CORNER 1.98V, 125°C	SS CORNER 1.62V, -40°C	SS CORNER 1.62V, 125°C	TT CORNER 1.8V, 25°C
[2]AC Current (uA/MHz)	55.412	50.702	62.069	39.045	19.489	27.266
Read AC Current (uA/MHz)	43.887	41.517	53.833	23.327	17.332	28.231
Write AC Current (uA/MHz)	66.936	59.887	70.304	54.763	21.646	26.301
Standby Power (mW)	0.203066	0.251745	0.630097	0.000421	0.015992	0.047126
[3]Deselect Current (uA/MHz)	14.774	14.211	10.929	6.725	7.823	6.481

Power simulation conditions:

2. CEN is low, 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz

3. CEN is high, 50% of input pins toggle at 1Mhz

WRITE CYCLE TIMING:
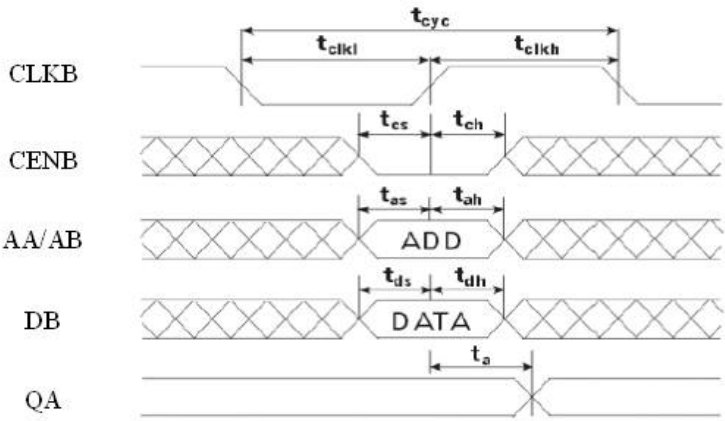
READ CYCLE TIMING:
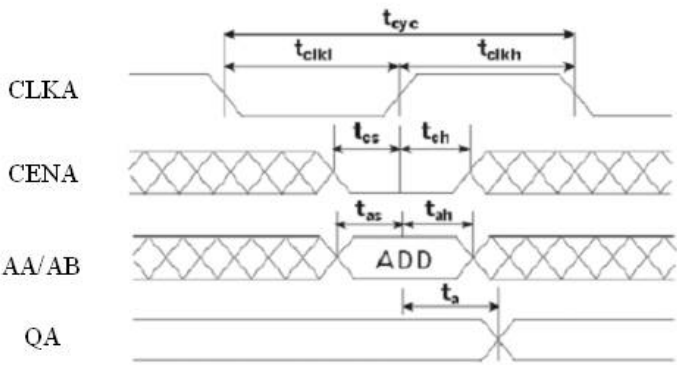
Datasheet Revision History

Date	Version	Changes
	null	