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1. Stage 1

Mentor precision and Aldec Riviera Pro for synthesis and simulation and used EDA Playground to code

a) ALU

i. EP Wave

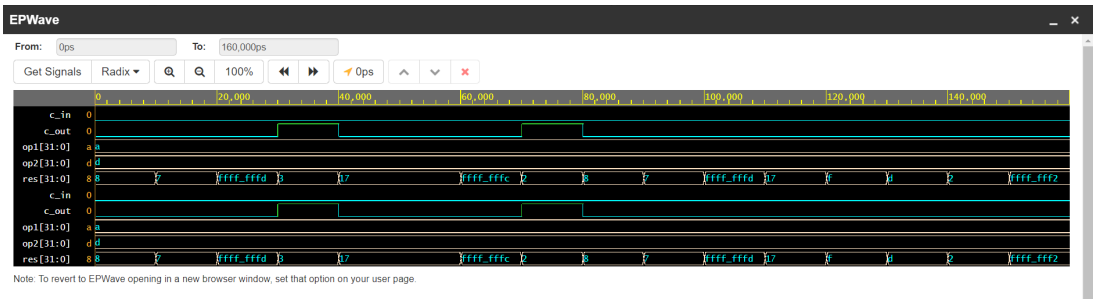

Figure 1: EP Wave output

ii. Basic working

At the crux, ALU is just a case statement. The file op_code.vhd has the type enumeration defined, and based on it and different opcode passed, the different operations are executed

iii. Log Output

All test cases pass, hence no error raised

```
[2022-02-09 01:09:18 EST] vlib work && vcom '-2008' op_code.vhd design.vhd testbench.vhd
    && vsim -c -do "vsim ALU_TB; vcd file dump.vcd; vcd add -r sim:/*; run -all; exit"
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
Aldec, Inc. VHDL Compiler, build 2020.04.130
VLM Initialized with path: "/home/runner/library.cfg".
DAGGEN WARNING DAGGEN_0523: "The source is compiled without the -dbg switch. Line
    breakpoints and assertion debug will not be available."
COMP96 File: op_code.vhd
COMP96 Compile Package "op_code"
COMP96 Compile Package Body "op_code"
COMP96 File: design.vhd
COMP96 Compile Entity "ALU"
COMP96 Compile Architecture "alu_arch" of Entity "ALU"
COMP96 File: testbench.vhd
COMP96 Compile Entity "ALU_TB"
COMP96 Compile Architecture "behavior" of Entity "ALU_TB"
COMP96 Compile success 0 Errors 0 Warnings Analysis time : 30.0 [ms]
```

```
# Aldec, Inc. Riviera-PRO version 2020.04.130.7729 built for Linux64 on June 10, 2020.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2020 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
# SLP: Finished : 0.0 [s]
# ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact Aldec for ordering information - sales@aldec.com.
# ELAB2: Elaboration final pass complete - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 5577 kB (elbread=427 elab2=5007 kernel=143 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2022-02-09 01:09:20 EST] Opening EPWave...
Done
```

iv. Basic NetList details

```
# Info: ******************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                      Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                           114     210      54.29%
# Info: Global Buffers                0       32        0.00%
# Info: LUTs                          107     63400     0.17%
# Info: CLB Slices                    26      15850     0.16%
# Info: Dffs or Latches               0       126800    0.00%
# Info: Block RAMs                    0       135       0.00%
# Info: DSP48E1s                      0       240       0.00%
# Info: ------------------------------------------------------------------
# Info: ******************************************************
# Info: Library: work  Cell: ALU   View: alu_arch
```

```
# Info: ****************************************************
# Info: Number of ports :                      114
# Info: Number of nets :                       365
# Info: Number of instances :                  285
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of LUTs :                       107
# Info: Number of LUTs with LUTNM/HLUTNM :       2
# Info: Number of MUX CARRYs :                  32
# Info: Number of accumulated instances :      285
```

b) Registers

i. EP Wave

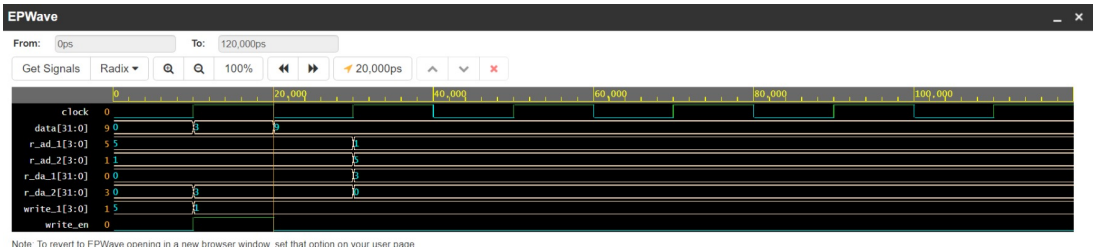

Figure 2: EP Wave output

ii. Basic working

r_ad_ 1 and 2 keep reading data into r_da_ 1 and 2 respectively, and whenever clock has a rising edge is write is enabled, we change the memory at wirte locn

iii. Log Output

```
[2022-02-09 01:31:38 EST] vlib work && vcom '-2008' op_code.vhd design.vhd testbench.vhd
    && vsim -c -do "vsim Reg_TB; vcd file dump.vcd; vcd add -r sim:/*; run -all; exit"
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
Aldec, Inc. VHDL Compiler, build 2020.04.130
VLM Initialized with path: "/home/runner/library.cfg".
DAGGEN WARNING DAGGEN_0523: "The source is compiled without the -dbg switch. Line
    breakpoints and assertion debug will not be available."
COMP96 File: op_code.vhd
COMP96 Compile Package "op_code"
COMP96 Compile Package Body "op_code"
COMP96 File: design.vhd
COMP96 Compile Entity "Reg"
COMP96 Compile Architecture "reg_arch" of Entity "Reg"
COMP96 File: testbench.vhd
COMP96 Compile Entity "Reg_TB"
COMP96 Compile Architecture "behavior" of Entity "Reg_TB"
```

```
COMP96 Compile success 0 Errors 0 Warnings Analysis time : 30.0 [ms]
# Aldec, Inc. Riviera-PRO version 2020.04.130.7729 built for Linux64 on June 10, 2020.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2020 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
# SLP: Finished : 0.0 [s]
# ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact
    Aldec for ordering information - sales@aldec.com.
# ELAB2: Elaboration final pass complete - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of
    simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 6586 kB (elbread=427 elab2=6016 kernel=143 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2022-02-09 01:31:39 EST] Opening EPWave...
Done
```

iv. Basic NetList details

```
# Info: ******************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                      Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                           110     210      52.38%
# Info: Global Buffers                1       32        3.12%
# Info: LUTs                          48      63400     0.08%
# Info: CLB Slices                    12      15850     0.08%
# Info: Dffs or Latches               0       126800    0.00%
# Info: Block RAMs                    0       135       0.00%
# Info: Distributed RAMs
# Info:   RAM32M                      10
# Info:   RAM64M                      2
```

```
# Info: DSP48E1s                        0       240      0.00%
# Info: ------------------------------------------------------------
# Info: ****************************************************
# Info: Library: work  Cell: Reg   View: reg_arch
# Info: ****************************************************
# Info: Number of ports :                          110
# Info: Number of nets :                           220
# Info: Number of instances :                      111
# Info: Number of references to this view :          0
# Info: Total accumulated area :
# Info: Number of LUTs :                            48
# Info: Number of accumulated instances :          123
# Info: ****************************
```

c) Data Mempory

i. EP Wave

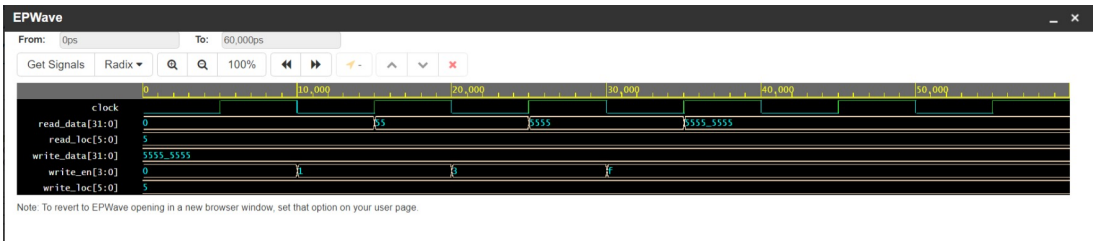

Figure 3: EP Wave output

ii. Basic working

wherever write is enabled, write that byte, else write 000000 in its place. For read,read from locn and keep outputing the signal

iii. Log Output

```
[2022-02-09 02:23:41 EST] vlib work && vcom '-2008' op_code.vhd design.vhd testbench.vhd
    && vsim -c -do "vsim DT_TB; vcd file dump.vcd; vcd add -r sim:/*; run -all; exit"
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
Aldec, Inc. VHDL Compiler, build 2020.04.130
VLM Initialized with path: "/home/runner/library.cfg".
DAGGEN WARNING DAGGEN_0523: "The source is compiled without the -dbg switch. Line
    breakpoints and assertion debug will not be available."
COMP96 File: op_code.vhd
COMP96 Compile Package "op_code"
COMP96 Compile Package Body "op_code"
COMP96 File: design.vhd
COMP96 Compile Entity "data_mem"
COMP96 Compile Architecture "arch" of Entity "data_mem"
```

```
COMP96 File: testbench.vhd
COMP96 Compile Entity "DT_TB"
COMP96 Compile Architecture "behavior" of Entity "DT_TB"
COMP96 Compile success 0 Errors 0 Warnings Analysis time : 20.0 [ms]
# Aldec, Inc. Riviera-PRO version 2020.04.130.7729 built for Linux64 on June 10, 2020.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2020 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
# SLP: Finished : 0.0 [s]
# ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact
    Aldec for ordering information - sales@aldec.com.
# ELAB2: Elaboration final pass complete - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of
    simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 5565 kB (elbread=427 elab2=4995 kernel=143 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2022-02-09 02:23:42 EST] Opening EPWave...
Done
```

iv. Basic NetList details

```


# Info: ******************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                    Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                         81      210     38.57%
# Info: Global Buffers              1       32       3.12%
# Info: LUTs                        64      63400    0.10%
# Info: CLB Slices                  16      15850    0.10%
```

```
# Info: Dffs or Latches                0      126800    0.00%
# Info: Block RAMs                     0      135       0.00%
# Info: Distributed RAMs
# Info:   RAM64X1D                     32
# Info: DSP48E1s                       0      240       0.00%
# Info: ------------------------------------------------------------
# Info: ********************************************************
# Info: Library: work  Cell: data_mem  View: arch
# Info: ********************************************************
# Info: Number of ports :                          81
# Info: Number of nets :                          162
# Info: Number of instances :                      82
# Info: Number of references to this view :         0
# Info: Total accumulated area :
# Info: Number of LUTs :                           64
# Info: Number of Primitive LUTs :                 64
# Info:   Number of LUTs as Distributed RAM :      64
# Info: Number of accumulated instances :         113
# Info: ****************************
```

d) Program Memory

i. EP Wave

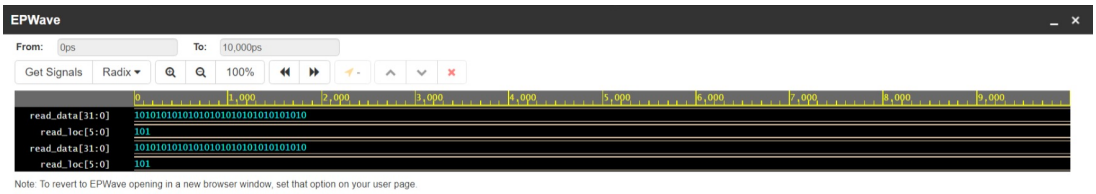

Figure 4: EP Wave output

ii. Basic working

Basically read from locn and keep outputing the signal

iii. Log Output

```
[2022-02-09 02:14:17 EST] vlib work && vcom '-2008' op_code.vhd design.vhd testbench.vhd
    && vsim -c -do "vsim PR_TB; vcd file dump.vcd; vcd add -r sim:/*; run -all; exit"
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
Aldec, Inc. VHDL Compiler, build 2020.04.130
VLM Initialized with path: "/home/runner/library.cfg".
DAGGEN WARNING DAGGEN_0523: "The source is compiled without the -dbg switch. Line
    breakpoints and assertion debug will not be available."
COMP96 File: op_code.vhd
COMP96 Compile Package "op_code"
```

```
COMP96 Compile Package Body "op_code"
COMP96 File: design.vhd
COMP96 Compile Entity "prog_mem"
COMP96 Compile Architecture "arch" of Entity "prog_mem"
COMP96 File: testbench.vhd
COMP96 Compile Entity "PR_TB"
COMP96 Compile Architecture "behavior" of Entity "PR_TB"
COMP96 Compile success 0 Errors 0 Warnings Analysis time : 20.0 [ms]
# Aldec, Inc. Riviera-PRO version 2020.04.130.7729 built for Linux64 on June 10, 2020.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2020 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
# SLP: Finished : 0.0 [s]
# ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact
    Aldec for ordering information - sales@aldec.com.
# ELAB2: Elaboration final pass complete - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of
    simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 5562 kB (elbread=427 elab2=4992 kernel=142 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2022-02-09 02:14:18 EST] Opening EPWave...
Done
```

iv. Basic NetList details

```
# Info: ******************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                      Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                           38      210     18.10%
# Info: Global Buffers                0       32       0.00%
```

```
# Info: LUTs                          0      63400    0.00%
# Info: CLB Slices                    0      15850    0.00%
# Info: Dffs or Latches               0      126800   0.00%
# Info: Block RAMs                    0      135      0.00%
# Info: DSP48E1s                      0      240      0.00%
# Info: ------------------------------------------------------------
# Info: ********************************************************
# Info: Library: work  Cell: prog_mem  View: arch
# Info: ********************************************************
# Info: Number of ports :                      38
# Info: Number of nets :                       34
# Info: Number of instances :                  34
# Info: Number of references to this view :     0
# Info: Total accumulated area : unknown
# Info: ****************************
```