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1. Stage 1

Mentor precision for synthesis and quartus for netlist and used EDA Playground to code

a) Processor

i. Processor

Figure 1: EP Wave output for program 1 and 2

Code for GCD Program used for testinG

```
0 => X"E3A00004",
1 => X"E3A01038",
2 => X"E1500001",
3 => X"0A000004",
4 => X"BA000001",
5 => X"E0400001",
6 => X"EAFFFFFA",
```

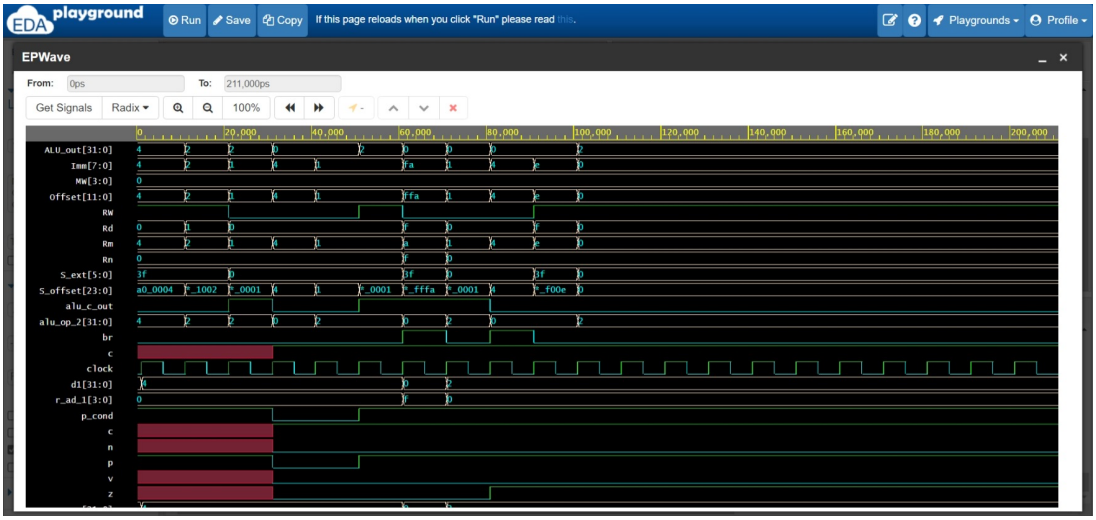

Figure 2: EP Wave output for custom gcd program

```
7 => X"E0411000",
8 => X"EAFFFFF8",
9 => X"E1A0F00E",
others => X"00000000"
```

b) Netlist

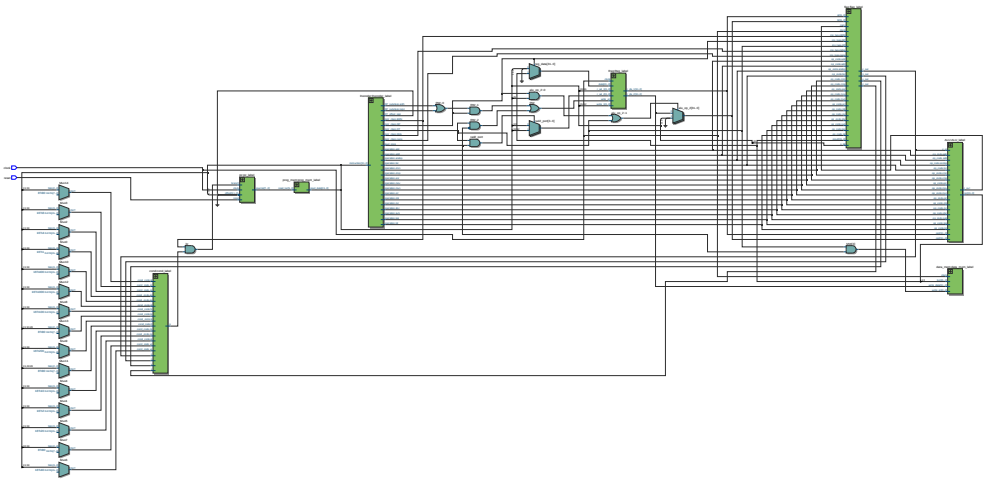

Figure 3: Net List

i. Basic working

Processor.vhd is the glue. It connects all the correct ports along with implementing the various signals for mux based on instruction types. All instructions happen in a single cycle as this staege is a single cycle cpu only. The cond.vhd implement the 15 various configurations of conditions. The flags.vhd implement various flags. Decode.vhd was provided by professor. PC is simple. It goes to +4 each cycle unless we get a branch instruction, in which case it goes pc + 4*offset + 8

ii. Log Output

```
[2022-02-19 09:27:18 EST] vlib work && vcom '-2019' '-o' ALU.vhd Cond.vhd data_mem.vhd Flags.vhd Instr.vhd MyTypes.vhd PC.vhd prog_mem.vhd Register.vhd design.vhd testbench.vhd && vsim -c -do "vsim TB; vcd file dump.vcd; vcd add -r sim:/*; run -all; exit"
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
Aldec, Inc. VHDL Compiler, build 2020.04.130
VLM Initialized with path: "/home/runner/library.cfg".
DAGGEN WARNING DAGGEN_0523: "The source is compiled without the -dbg switch. Line breakpoints and assertion debug will not be available."
COMP96 File: ALU.vhd
COMP96 Compile Entity "ALU"
COMP96 Compile Architecture "alu_arch" of Entity "ALU"
COMP96 File: Cond.vhd
COMP96 Compile Entity "cond"
COMP96 Compile Architecture "arch" of Entity "cond"
COMP96 File: data_mem.vhd
COMP96 Compile Entity "data_mem"
COMP96 Compile Architecture "arch" of Entity "data_mem"
COMP96 File: Flags.vhd
COMP96 Compile Entity "flag"
COMP96 Compile Architecture "arch" of Entity "flag"
COMP96 File: Instr.vhd
COMP96 Compile Entity "Decoder"
COMP96 Compile Architecture "Behavioral" of Entity "Decoder"
COMP96 File: MyTypes.vhd
COMP96 Compile Package "MyTypes"
COMP96 Compile Package Body "MyTypes"
COMP96 File: PC.vhd
COMP96 Compile Entity "pc"
COMP96 Compile Architecture "arch" of Entity "pc"
COMP96 File: prog_mem.vhd
COMP96 Compile Entity "prog_mem"
COMP96 Compile Architecture "arch" of Entity "prog_mem"
COMP96 File: Register.vhd
COMP96 Compile Entity "Reg"
COMP96 Compile Architecture "reg_arch" of Entity "Reg"
COMP96 File: design.vhd
COMP96 Compile Entity "processor"
COMP96 Compile Architecture "arch" of Entity "processor"
COMP96 File: testbench.vhd
COMP96 Compile Entity "TB"
COMP96 Compile Architecture "behavior" of Entity "TB"
COMP96 Incorrect order of units detected.
COMP96 Automatic reorder and incremental recompilation of required units in progress.
COMP96 File: ALU.vhd
COMP96 Compile Entity "ALU"
COMP96 Compile Architecture "alu_arch" of Entity "ALU"
COMP96 File: Cond.vhd
```

```
COMP96 Compile Entity "cond"
COMP96 Compile Architecture "arch" of Entity "cond"
COMP96 File: Instr.vhd
COMP96 Compile Entity "Decoder"
COMP96 Compile Architecture "Behavioral" of Entity "Decoder"
COMP96 File: Flags.vhd
COMP96 Compile Entity "flag"
COMP96 Compile Architecture "arch" of Entity "flag"
COMP96 File: design.vhd
COMP96 Compile Architecture "arch" of Entity "processor"
COMP96 Top-level unit(s) detected:
COMP96 Entity => TB
COMP96 Compile success 0 Errors 0 Warnings Analysis time : 0.1 [s]
# Aldec, Inc. Riviera-PRO version 2020.04.130.7729 built for Linux64 on June 10, 2020.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2020 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
# SLP: Finished : 0.0 [s]
# ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact
    Aldec for ordering information - sales@aldec.com.
# ELAB2: Elaboration final pass complete - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of
    simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 6628 kB (elbread=427 elab2=6057 kernel=144 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut, Process: line__213.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut, Process: line__230.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut, Process: line__231.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut, Process: line__232.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/Decoder_label, Process: line__28.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/Reg_label, Process: line__22.
```

```
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/Reg_label, Process: line__23.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/data_mem_label, Process: line__20.
# RUNTIME: Fatal Error: RUNTIME_0046 PC.vhd (24): Incompatible ranges; left: (7 downto 0),
    right: (31 downto 0).
# KERNEL: Time: 65 ns, Iteration: 1, Instance: /TB/uut/pc_label, Process: c.
# KERNEL: Stopped at time 65 ns + 1.
# VSIM: Error: Fatal error occurred during simulation.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2022-02-19 09:27:20 EST] Opening EPWave...
Done
```