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1. Stage 3

Mentor precision for synthesis and quartus for netlist and used EDA Playground to code

a) Multi Cycle Processor

i. EP Waves

Figure 1: EP Wave output for program 1

Figure 2: EP Wave output for program 2

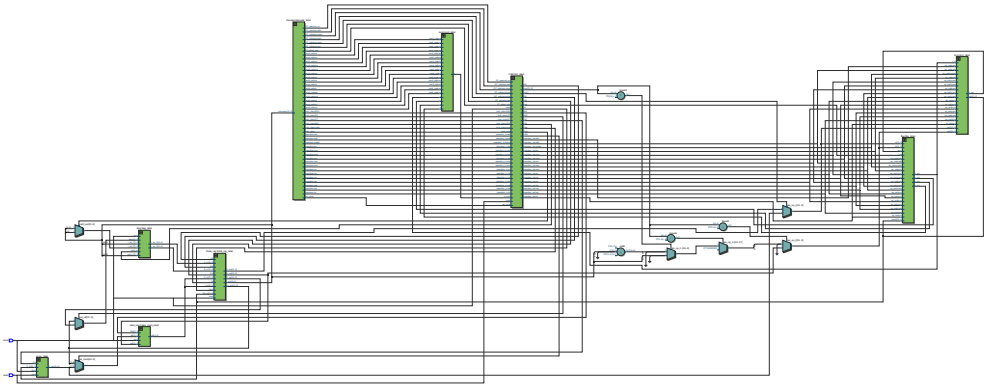

Figure 3: Net List

b) Netlist

i. Basic working

Now along with all the previous glue logic, we have an extra FSM module and IDAB module. IDAB module essentially is a module for I,D,A and B registers. The FSM implements the state machine. The template of this state machine was generated with the help of quartus. [1]. Essentially FSM module has a signal name reg_fstate, which holds the next state and fstate becomes reg_fstate when a rising edge occours. This FSM takes in input as clock, instructions decoded and output the corresponting signals for Muxes and write enable signals. Essentially we implement the FSM and processor design as shown in Lec10 slides.

ii. Log Output

```
[2022-02-24 09:51:56 EST] vlib work && vcom '-2019' '-o' ALU.vhd Cond.vhd data_mem.vhd
    Flags.vhd FSM.vhd IDAB_Reg.vhd Instr.vhd MyTypes.vhd PC.vhd Register.vhd design.vhd
```

[1] It has an option for automatically converting FSM diagram to vhdl code

```
    testbench.vhd && vsim -c -do "vsim TB; vcd file dump.vcd; vcd add -r sim:/*; run -all;
     exit"
VSIMSA: Configuration file changed: ‘/home/runner/library.cfg’
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
Aldec, Inc. VHDL Compiler, build 2020.04.130
VLM Initialized with path: "/home/runner/library.cfg".
DAGGEN WARNING DAGGEN_0523: "The source is compiled without the -dbg switch. Line
    breakpoints and assertion debug will not be available."
COMP96 File: ALU.vhd
COMP96 Compile Entity "ALU"
COMP96 Compile Architecture "alu_arch" of Entity "ALU"
COMP96 File: Cond.vhd
COMP96 Compile Entity "cond"
COMP96 Compile Architecture "arch" of Entity "cond"
COMP96 File: data_mem.vhd
COMP96 Compile Entity "data_mem"
COMP96 Compile Architecture "arch" of Entity "data_mem"
COMP96 File: Flags.vhd
COMP96 Compile Entity "flag"
COMP96 Compile Architecture "arch" of Entity "flag"
COMP96 File: FSM.vhd
COMP96 Compile Entity "FSM"
COMP96 Compile Architecture "behaviour" of Entity "FSM"
COMP96 File: IDAB_Reg.vhd
COMP96 Compile Entity "IDAB_reg"
COMP96 Compile Architecture "IDAB_reg_arch" of Entity "IDAB_reg"
COMP96 File: Instr.vhd
COMP96 Compile Entity "Decoder"
COMP96 Compile Architecture "Behavioral" of Entity "Decoder"
COMP96 File: MyTypes.vhd
COMP96 Compile Package "MyTypes"
COMP96 Compile Package Body "MyTypes"
COMP96 File: PC.vhd
COMP96 Compile Entity "pc"
COMP96 Compile Architecture "arch" of Entity "pc"
COMP96 File: Register.vhd
COMP96 Compile Entity "Reg"
COMP96 Compile Architecture "reg_arch" of Entity "Reg"
COMP96 File: design.vhd
COMP96 Compile Entity "processor"
COMP96 Compile Architecture "arch" of Entity "processor"
COMP96 File: testbench.vhd
COMP96 Compile Entity "TB"
COMP96 Compile Architecture "behavior" of Entity "TB"
COMP96 Incorrect order of units detected.
COMP96 Automatic reorder and incremental recompilation of required units in progress.
COMP96 File: ALU.vhd
COMP96 Compile Entity "ALU"
COMP96 Compile Architecture "alu_arch" of Entity "ALU"
COMP96 File: Cond.vhd
```

```
COMP96 Compile Entity "cond"
COMP96 Compile Architecture "arch" of Entity "cond"
COMP96 File: FSM.vhd
COMP96 Compile Entity "FSM"
COMP96 Compile Architecture "behaviour" of Entity "FSM"
COMP96 File: Instr.vhd
COMP96 Compile Entity "Decoder"
COMP96 Compile Architecture "Behavioral" of Entity "Decoder"
COMP96 File: Flags.vhd
COMP96 Compile Entity "flag"
COMP96 Compile Architecture "arch" of Entity "flag"
COMP96 File: design.vhd
COMP96 Compile Architecture "arch" of Entity "processor"
COMP96 Top-level unit(s) detected:
COMP96 Entity => TB
COMP96 Compile success 0 Errors 0 Warnings Analysis time : 0.2 [s]
# Aldec, Inc. Riviera-PRO version 2020.04.130.7729 built for Linux64 on June 10, 2020.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2020 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
# SLP: Finished : 0.0 [s]
# ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact
    Aldec for ordering information - sales@aldec.com.
# ELAB2: Elaboration final pass complete - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of
    simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 8072 kB (elbread=427 elab2=7500 kernel=144 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/Decoder_label, Process: line__34.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/Decoder_label, Process: line__48.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/data_mem_label, Process: line__29.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/Reg_label, Process: line__25.
# KERNEL: WARNING: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
```

```
99  # KERNEL: Time: 0 ps, Iteration: 0, Instance: /TB/uut/Reg_label, Process: line__26.
100 # KERNEL: Simulation has finished. There are no more test vectors to simulate.
101 # VSIM: Simulation has finished.
102 Finding VCD file...
103 ./dump.vcd
104 [2022-02-24 09:51:58 EST] Opening EPWave...
105 Done
```