
STM32
CubeMX

1. Description

1.1. Project

Project Name	oscilloscope
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 6.0.0
Date	06/04/2024

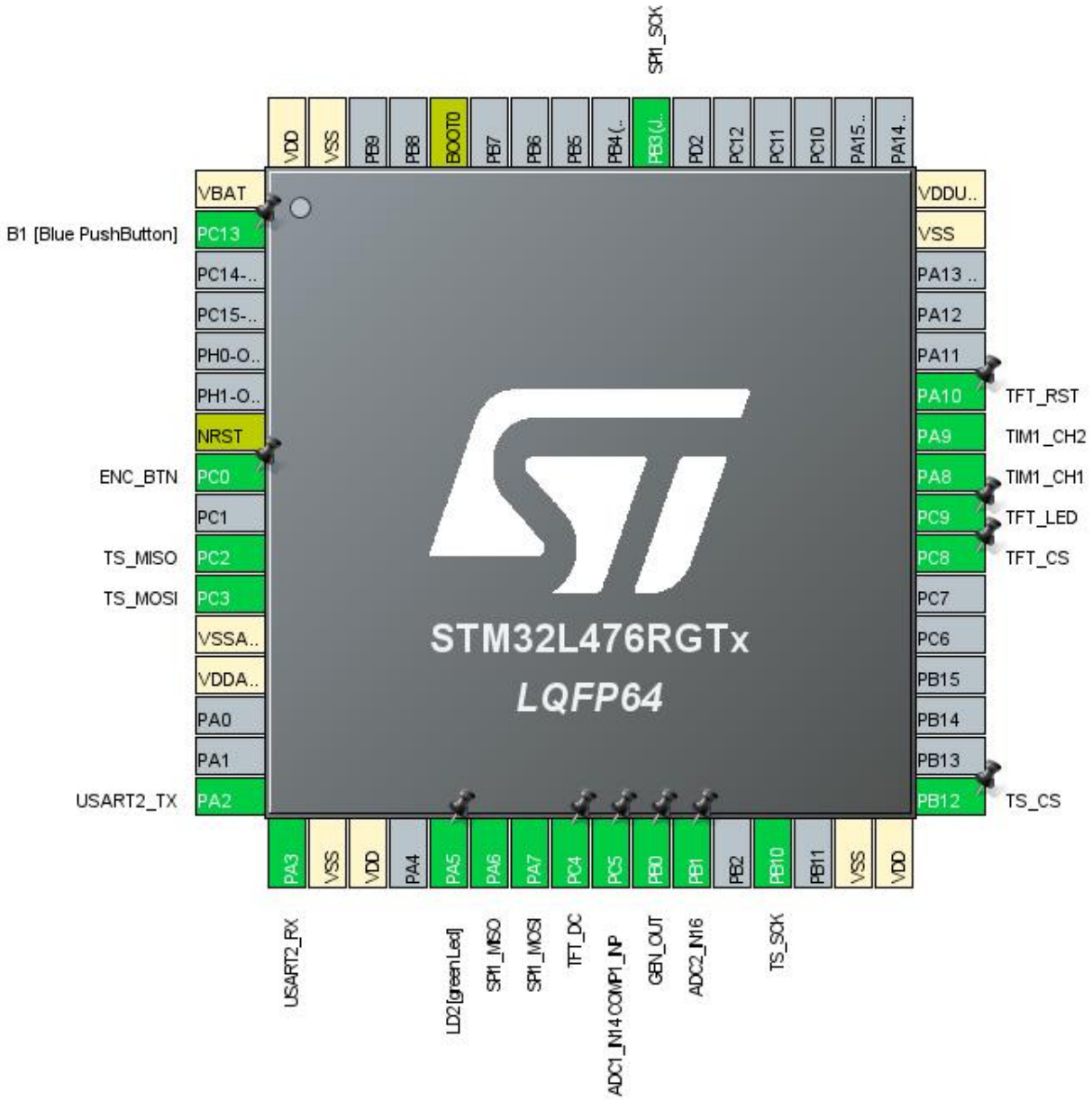
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

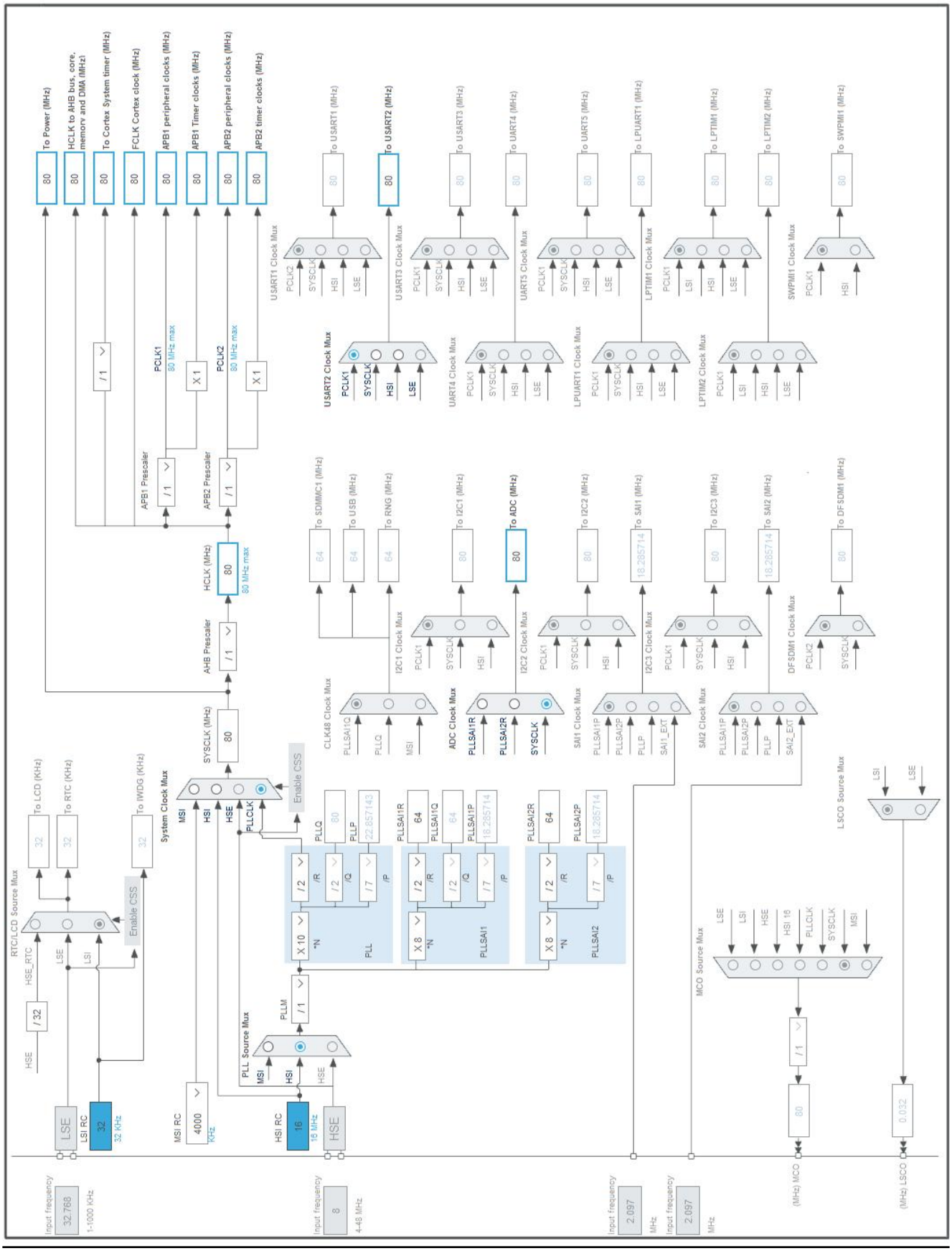


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	ENC_BTN
10	PC2	I/O	SPI2_MISO	TS_MISO
11	PC3	I/O	SPI2_MOSI	TS_MOSI
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LD2 [green Led]
22	PA6	I/O	SPI1_MISO	
23	PA7	I/O	SPI1_MOSI	
24	PC4 *	I/O	GPIO_Output	TFT_DC
25	PC5	I/O	ADC1_IN14, COMP1_INP	
26	PB0	I/O	TIM3_CH3	GEN_OUT
27	PB1	I/O	ADC2_IN16	
29	PB10	I/O	SPI2_SCK	TS_SCK
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	TS_CS
39	PC8 *	I/O	GPIO_Output	TFT_CS
40	PC9	I/O	TIM3_CH4	TFT_LED
41	PA8	I/O	TIM1_CH1	
42	PA9	I/O	TIM1_CH2	
43	PA10 *	I/O	GPIO_Output	TFT_RST
47	VSS	Power		
48	VDDUSB	Power		
55	PB3 (JTDO-TRACESWO)	I/O	SPI1_SCK	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	oscilloscope
Project Folder	E:\PWR\Semestr6\Sterowniki_robotow\KD-23MTS\code
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.16.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_SPI1_Init	SPI1
5	MX_SPI2_Init	SPI2
6	MX_TIM3_Init	TIM3
7	MX_ADC1_Init	ADC1
8	MX_TIM1_Init	TIM1
9	MX_USART2_UART_Init	USART2
10	MX_DAC1_Init	DAC1
11	MX_COMP1_Init	COMP1

Rank	Function Name	IP Instance Name
12	MX_ADC2_Init	ADC2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	DS10198_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

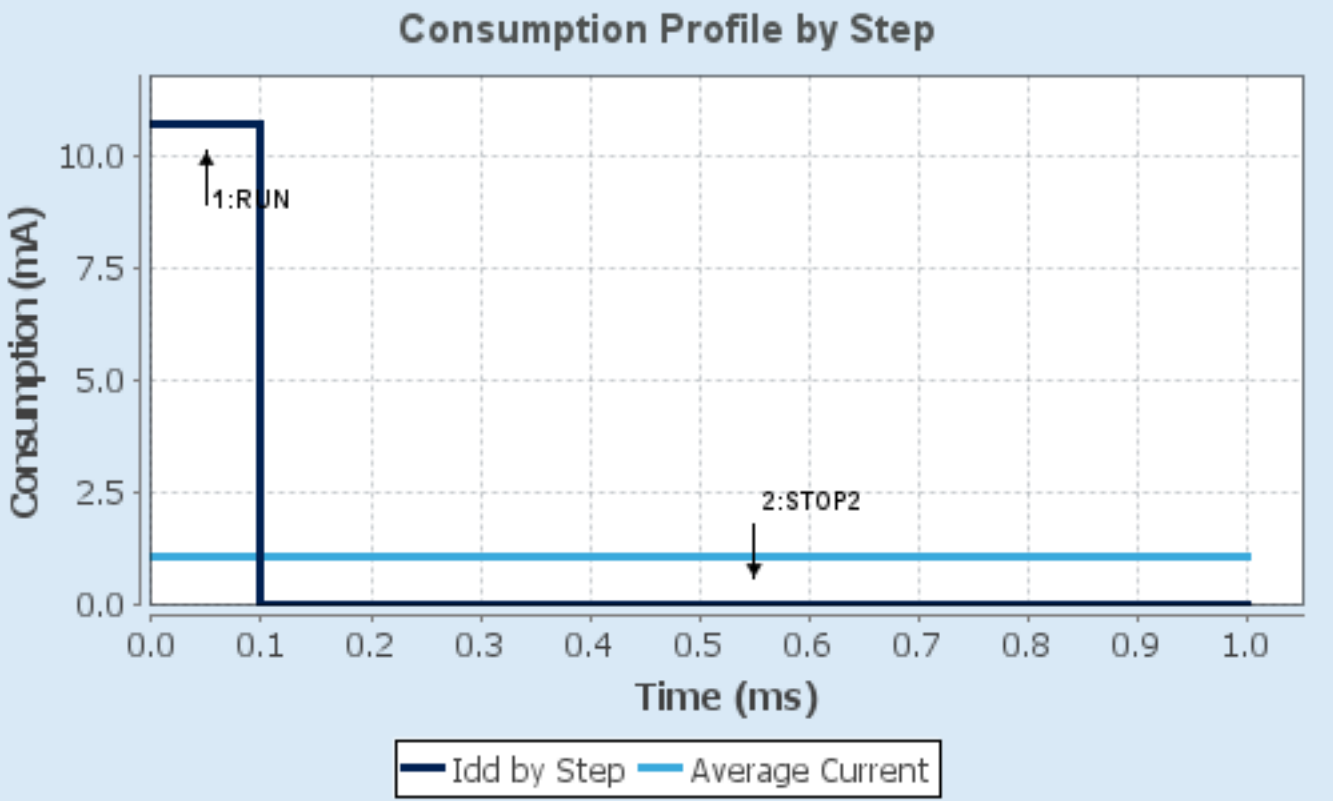
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.56	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

IN14: IN14 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 14
Sampling Time	**6.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

mode: IN16 Single-ended

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 16
Sampling Time	**6.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. COMP1

mode: Input [+]

Input [-]: DAC OUT1

7.3.1. Parameter Settings:

Basic Parameters:

Speed / Power Mode	High Speed
Trigger Mode	**Rising Edge Interrupt ***
Hysteresis Level	**Low ***

Output Configuration:

Blanking Source	None
Output Pol	COMP output on GPIO isn't inverted

7.4. DAC1

OUT1 mode: Connected to on chip-peripherals only

7.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Disable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.5. GPIO

7.6. RCC

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0

MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.7. SPI1

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**40.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.8. SPI2

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**10.0 MBits/s ***
Clock Polarity (CPOL)	Low

Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.9. SYS

Timebase Source: SysTick

7.10. TIM1

Combined Channels: Encoder Mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.11. TIM3

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**79 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.12. USART2

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC5	ADC1_IN14	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
ADC2	PB1	ADC2_IN16	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
COMP1	PC5	COMP1_INP	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
SPI1	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB3 (JTDO-TRACESWO)	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TS_MISO
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TS_MOSI
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TS_SCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	**Pull-up ***	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	**Pull-up ***	Low	
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	GEN_OUT
	PC9	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	TFT_LED
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC0	GPIO_Input	Input mode	**Pull-up ***	n/a	ENC_BTN
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green Led]
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	TFT_DC
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High**	TS_CS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	TFT_CS
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	TFT_RST

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_TX	DMA1_Channel3	Memory To Peripheral	Low
ADC1	DMA1_Channel1	Peripheral To Memory	Low
ADC2	DMA1_Channel2	Peripheral To Memory	Low

SPI1_TX: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
COMP1 and COMP2 interrupts through EXTI lines 21 and 22	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
SPI2 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false

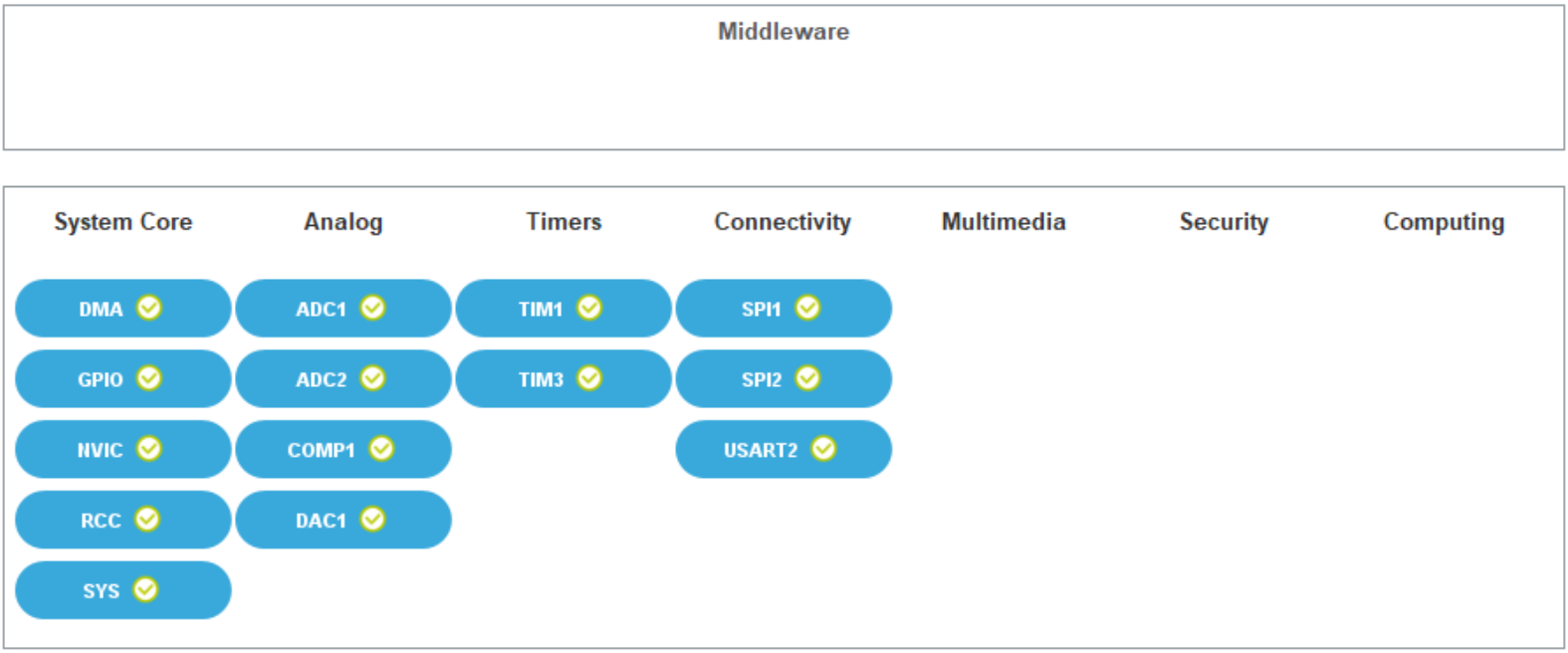
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Prefetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
DMA1 channel1 global interrupt	true	true	true
DMA1 channel2 global interrupt	true	true	true
DMA1 channel3 global interrupt	true	true	true
SPI1 global interrupt	true	true	true
COMP1 and COMP2 interrupts through EXTI lines 21 and 22	true	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00108832.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00083560.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00111498.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156964.pdf
Application note	http://www.st.com/resource/en/application_note/DM00150423.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209748.pdf

Application note	http://www.st.com/resource/en/application_note/DM00125306.pdf
Application note	http://www.st.com/resource/en/application_note/DM00141025.pdf
Application note	http://www.st.com/resource/en/application_note/DM00144612.pdf
Application note	http://www.st.com/resource/en/application_note/DM00148033.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209768.pdf
Application note	http://www.st.com/resource/en/application_note/DM00216518.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00269143.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00269146.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209772.pdf
Application note	http://www.st.com/resource/en/application_note/DM00476869.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660597.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf