Interfacing op amps to high-speed DACs, Part 1: Current-sinking DACs

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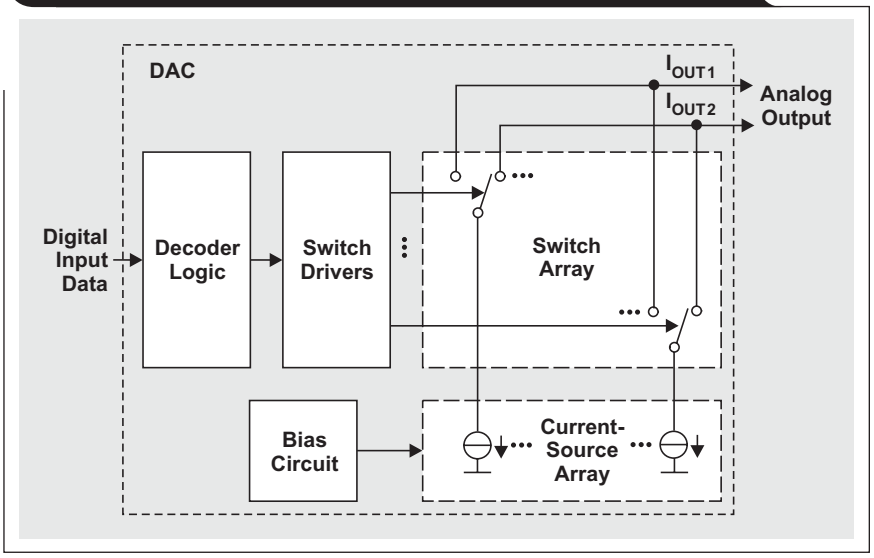
Introduction

Digital-to-analog converters (DACs) come in many bit resolutions and sampling speeds. Outputs from lower-speed DACs are often single-ended and have either a voltage or a current output. Most high-speed DACs are designed with complementary outputs that either source or sink current. This article, Part 1 of a three-part series, discusses the interface between a current-sinking DAC and an op amp. Part 2, which will appear in a future issue of the *Analog Applications Journal*, will discuss the interface between a current-sourcing DAC and an op amp. Part 3, also in a future issue of the *Analog Applications Journal*, will provide a simplified approach to the interface analogy presented in Part 2.

Figure 1. Simplified block diagram of current-steering DAC



High-speed DACs are used in end-equipment applications like communications, test equipment, medical applications, industrial applications, and many more where signal generation is required. Each of these applications has its own specific requirements for signal characteristics and performance. This article focuses on end equipment that requires DC coupling, like signal generators with frequency bandwidths of up to 100 MHz and a single-ended output. In these cases, high-speed op amps can provide a good solution for converting the complementary-current output from a high-speed DAC to a voltage that can drive the signal output.

Overview of complementary-current-steering DAC

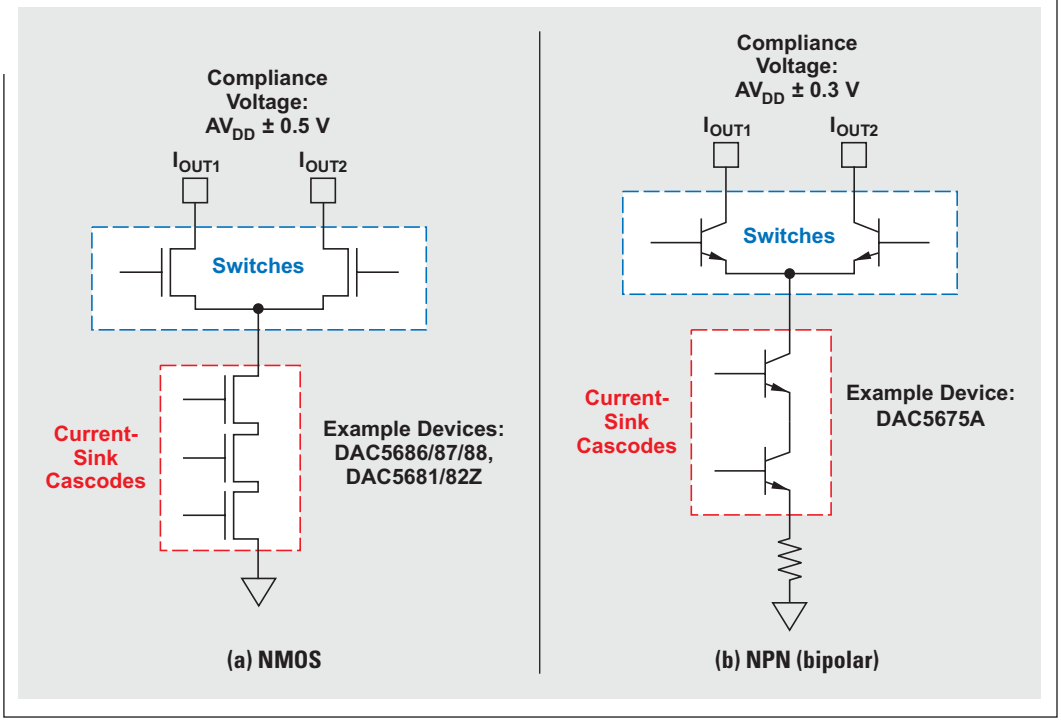
A simplified block diagram of a complementary-current-steering DAC is shown in Figure 1. The digital input is decoded for the switch drivers that switch, or steer, the appropriate current source(s) in the current-source array to the outputs, I_{OUT1} and I_{OUT2}. I_{OUT1} and I_{OUT2} are complementary, which means that if current flows out of one it is subtracted from the other, and vice versa, keeping the total current constant. For example, if full scale is 20 mA, the minimum code input or zero-scale input may provide 0 mA at I_{OUT1} and 20 mA at I_{OUT2}. At midscale, each output provides 10 mA; and at maximum or full scale, I_{OUT1} = 20 mA and I_{OUT2} = 0 mA. This example is illustrated in Table 1. It is important to note that the midscale input, with each output at 10 mA, will be used to set the output common-mode condition for the design.

The current-source array is constructed with either n-type or p-type transistors. The word "source" is used generically to refer to the transistor circuit structure, which may either source or sink current. This article considers the interface between a current-sinking DAC and an op amp in the case where the source array is constructed with n-type transistors.

Table 1. Example of I_{OUT1} and I_{OUT2} currents for 20-mA full scale

INPUT	I_{OUT1} (mA)	I_{OUT2} (mA)
Maximum Scale	20	0
Midscale	10	10
Zero Scale	0	20

Figure 2. Simplified NMOS and NPN current sinks

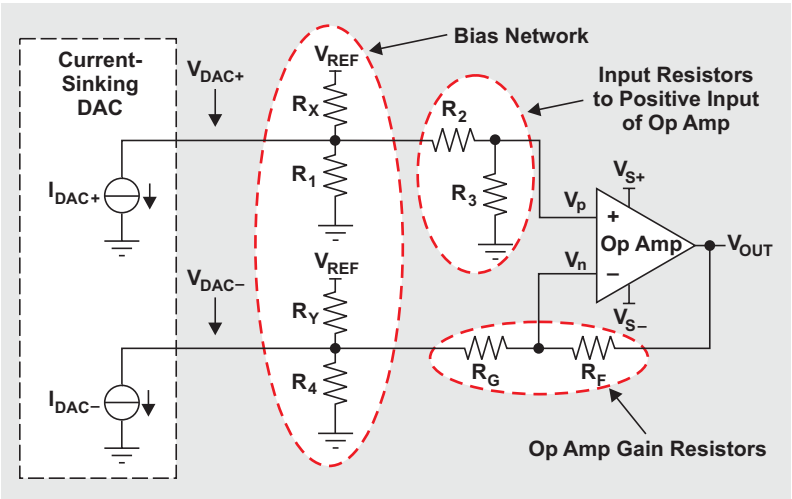


Architecture and compliance voltage of current-sinking DACs

Figure 2 shows simplified examples of NMOS and NPN current sinks and lists a few devices that use them. The compliance voltage shown for each group of devices is the voltage range at the DAC outputs within which a device will perform as specified. Lower voltages tend to shut down the outputs, and higher voltages have the potential to cause breakdown. Both of these should be avoided to provide the best performance and long-term reliability.

Generally the output is terminated via some impedance to a positive power supply. This impedance supplies a current path needed for the sink array, and the voltage drop across the same impedance can be used as a voltage output. The impedance can be constructed in various ways; it can be a simple resistor divider, a transformer-coupled impedance, or a combination of passive components and an active circuit. This article focuses on the latter option, with an op amp as the active circuit.

Figure 3. Proposed circuit for an op amp interface



Op amp interface

The proposed op amp interface is shown in Figure 3. This circuit will provide biasing of the DAC outputs, convert the DAC currents to voltages, and provide a single-ended output voltage via the op amp. The op amp is the active amplifier element for the circuit and uses R_2, R_3, R_G, and R_F to make a difference amplifier.

- I_{DAC+} and I_{DAC-} are the current outputs from the DAC.
- R_2 and R_3 are input resistors to the positive input of the op amp.
- R_G and R_F are the main gain-setting resistors for the op amp.
- R_X, R_1, R_Y, and R_4 provide bias and impedance termination for the DAC outputs.

- V_{DAC+} and V_{DAC-} are the voltages at the outputs of the DAC.
- V_p and V_n are the input terminals of the op amp.
- V_{S+} and V_{S-} are the power supplies to the op amp.

Proper component selection will provide the impedance required to maintain voltage compliance with maximum amplitude and balance for the best performance.

Typically, harmonic distortion in an op amp is dominated (at least at lower frequencies) by the second-order harmonics. Balanced inputs to the difference-amplifier circuit will help suppress second-order harmonics and provide for the best performance, but little impact is expected on third-order harmonics if the inputs are not balanced.

For analysis, it is easiest to break the circuit into positive and negative halves and examine each separately. It will also be assumed that the op amp is ideal.

Analysis of positive side

The positive half of the circuit is shown in Figure 4. To start the analysis, Kirchhoff's current law can be used to write a node equation at V_{DAC+}:

$$I_{DAC+} + \frac{V_{DAC+} - V_{REF}}{R_X} + \frac{V_{DAC+}}{R_1} + \frac{V_{DAC+}}{R_2 + R_3} = 0 \qquad (1)$$

The input impedance can be expressed as

$$Z_{DAC+} = R_X \parallel R_1 \parallel (R_2 + R_3). \qquad (2)$$

Equations 1 and 2 are simultaneous equations with many variables, and designers must choose or identify values based on other design criteria in order to solve them. The following assumptions are made for this article:

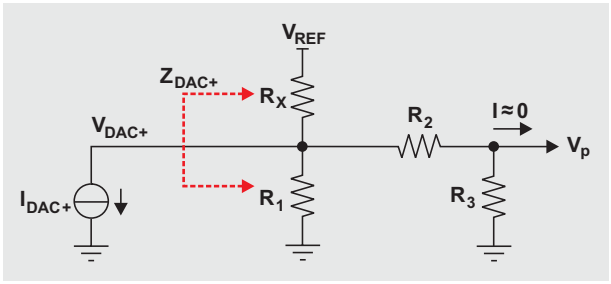
1. The DAC output current, I_{DAC+}, and the voltage swing, V_{DAC+}, are defined by the designer, which sets a target value for Z_{DAC+}.
2. An existing circuit voltage or other known voltage is used for V_{REF}.
3. In a difference amplifier, R_3/R_2 needs to equal R_F/R_G to balance the gain of the amplifier.*
4. The equations will be solved for the condition where the DAC current on the positive side is zero: I_{DAC+} = 0 mA. This in turn sets the DAC voltage on the positive side to its maximum value, $V_{DAC+} = V_{DAC+}(max)$.

With these constraints, the designer can apply algebra and simultaneous-equation techniques to Equations 1 and 2 to solve for $1/R_1$:

$$\frac{1}{R_1} = \frac{1}{Z_{DAC+}\left(1 + \frac{1}{\frac{V_{REF}}{V_{DAC+(max)}} - 1}\right)} - \frac{1}{R_2 + R_3} \qquad (3)$$

*Note that in a voltage-feedback op amp, it is desirable to make the impedance at V_p equal to that at V_n in order to cancel voltage offset caused by the input bias current. In a current-feedback op amp, the input bias currents are not correlated; so it is acceptable not to balance these impedances, but it may be desirable to minimize them.

Figure 4. Positive side of analysis circuit



The known value for R_1 can be substituted into Equation 2, which can then be rearranged to find $1/R_X$:

$$\frac{1}{R_X} = \frac{1}{Z_{DAC+}} - \frac{1}{R_1} - \frac{1}{R_2 + R_3} \qquad (4)$$

Analysis of negative side

The negative half of the circuit is shown in Figure 5. Analysis of the negative side is complicated, because V_n is driven not only by the negative side of the DAC but also by the positive side via the op amp's action. To start the analysis, Kirchhoff's current law can be used to write a node equation at V_{DAC-}:

$$I_{DAC-} + \frac{V_{DAC-} - V_{REF}}{R_Y} + \frac{V_{DAC-}}{R_4} + \frac{V_{DAC-} - V_n}{R_G + R_3} = 0 \qquad (5)$$

The input impedance can be expressed as

$$Z_{DAC-} = \frac{V_{DAC-}}{I_{DAC-}}. \qquad (6)$$

With substitution and rearrangement, the designer can use

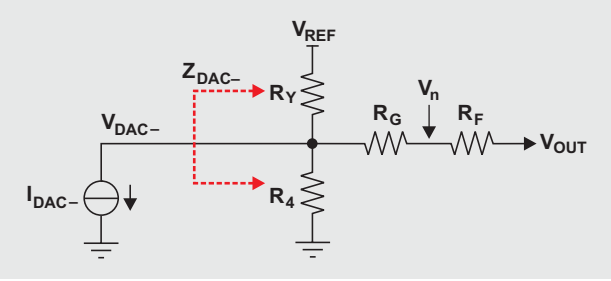
$$V_p = V_{DAC+} \times \frac{R_3}{R_2 + R_3}$$

and $V_n = \alpha V_p$ to rewrite Equation 6 as

$$\frac{1}{Z_{DAC-}} = \frac{1}{Z_{DAC+} \times \alpha\left(\frac{R_3}{R_2 + R_3}\right)} \times \left(\frac{1}{R_Y} + \frac{1}{R_4} + \frac{1}{R_G}\right). \qquad (7)$$

$$1 - \frac{}{R_G}$$

Figure 5. Negative side of analysis circuit



Using the same substitutions and general design constraints used on the positive side to drive values for Z_{DAC-}, V_{REF}, and R_G, simultaneous-equation techniques can be applied to Equations 5 and 7 to solve for $1/R_4$ (Equation 8). Note that the equations are solved for the condition where the DAC current on the negative side is zero: $I_{DAC-} = 0$ mA. This sets the DAC voltage on the negative side to its maximum value, $V_{DAC-} = V_{DAC-(max)}$, and sets the DAC voltage on the positive side to its minimum value, $V_{DAC+} = V_{DAC+(min)}$.

$$\frac{1}{R_4} = \frac{\dfrac{1-\dfrac{Z_{DAC+}\times\alpha\left(\dfrac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} + \left[\dfrac{V_{DAC+(min)}\times\alpha\left(\dfrac{R_3}{R_2+R_3}\right) - V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}} - 1\right]\left(\dfrac{1}{R_G}\right)}{\dfrac{V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}+1} \quad \textbf{(8)}$$

The value of $1/R_4$ can then be used to find $1/R_Y$:

$$\frac{1}{R_Y} = \frac{1-\dfrac{Z_{DAC+}\times\alpha\left(\dfrac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} - \left(\frac{1}{R_4}+\frac{1}{R_G}\right) \quad \textbf{(9)}$$

Note that α, the multiplication factor from V_p to V_n, in essence expresses the difference between the input pins. In a voltage-feedback amplifier, α is set by the loop gain of the amplifier. In a current-feedback amplifier, α is the gain of the input buffer between the inputs. All that aside, α is typically close enough to 1 that it can simply be removed from the calculation.

Calculating output voltage

Superposition can be used to write equations for the separate sources referred to V_{OUT}. Since the DAC only sinks current, which is by convention negative current flow, the output-voltage swing is the opposite of what might be expected. In other words, when the DAC is sinking current on the positive side, the output of the op amp tends to swing negative, and when the DAC is sinking current on the negative side, the output of the op amp tends to swing positive. This means that in the following equations, I_{DAC+} and I_{DAC-} are always negative or zero.

The output-referred DC bias from the positive side is

$$V_{OUT\_V_{p(DC)}} = \left(1+\frac{R_F}{R_G+R_Y \parallel R_4}\right)\times\left[V_{REF}\times\frac{R_1R_3}{R_1(R_2+R_3)+R_X(R_1+R_2+R_3)}\right].$$

The output-referred DAC signal from the positive side is

$$V_{OUT\_V_{p(DAC)}} = \left(1+\frac{R_F}{R_G+R_Y \parallel R_4}\right)\times\left[I_{DAC+}\times\frac{R_XR_1R_3}{R_XR_1+(R_1+R_X)(R_2+R_3)}\right].$$

The output-referred DC bias from the negative side is

$$V_{OUT\_V_{n(DC)}} = -\left(V_{REF}\times\frac{R_4}{R_Y+R_4}\times\frac{R_F}{R_G+R_Y \parallel R_4}\right).$$

The output-referred DAC signal from the negative side is

$$V_{OUT\_V_{n(DAC)}} = -\left(I_{DAC-}\times\frac{R_YR_4R_F}{R_YR_4+R_GR_4+R_YR_G}\right).$$

Adding these four equations provides an expression for V_{OUT}:

$$V_{OUT} = V_{OUT\_V_{p(DC)}} + V_{OUT\_V_{p(DAC)}} + V_{OUT\_V_{n(DC)}} + V_{OUT\_V_{n(DAC)}} \quad \textbf{(10)}$$

If it is assumed that $I_{DAC} = I_{DAC+} - I_{DAC-}$, $Z = Z_{DAC+} = Z_{DAC-}$, and $R_F/R_G = R_3/R_2$, the DC component of the DAC outputs will cancel and the AC-signal's gain equation from the DAC output current to the voltage output of the op amp can be simplified and written as

$$\frac{V_{OUT}}{I_{DAC}} = 2Z\times\frac{R_F}{R_G}. \quad \textbf{(11)}$$

Design example and simulation

For an example of how to proceed with the design, assume that one of the NMOS DACs noted earlier, with a compliance voltage of 3.3 ±0.5 V, is being used. Also assume that the full-scale output is set to 20 mA. To get a 5-V_{PP}, DC-coupled single-ended output signal, the circuit shown in Figure 3 can be used. Since a ±5-V power supply is being used for the op amp, it is convenient to make V_{REF} = 5 V. Given that $I_{DAC±}$ = 20 mA and $V_{DAC±}$ = 1 V_{PP}, the target impedance, $Z_{DAC±}$, can be calculated to equal 50 Ω.

With the starting design constraints given earlier, the THS3095 current-feedback op amp is selected as the amplifier, where $R_3 = R_F$ = 750 Ω. The gain from $V_{DAC±}$ to the output is given by the resistor ratios $R_F/R_G = R_3/R_2$, so R_G can be calculated as

$$R_G = R_2 = R_F \times \frac{V_{DAC±}}{V_{OUT}} = 750\ \Omega \times \frac{2(1\ V)}{5\ V} = 300\ \Omega.$$

The nearest standard 1% value, 301 Ω, should be used.

Equations 3, 4, 8, and 9 can be used to find, respectively, R_1, R_X, R_4, and R_Y:

$$R_1 = \frac{1}{\frac{1}{Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(max)}}-1}\right)} - \frac{1}{R_2+R_3}} = \frac{1}{\frac{1}{50\ \Omega\left(1+\frac{1}{\frac{5\ V}{3.8\ V}-1}\right)} - \frac{1}{301\ \Omega+750\ \Omega}} = 259.8\ \Omega$$

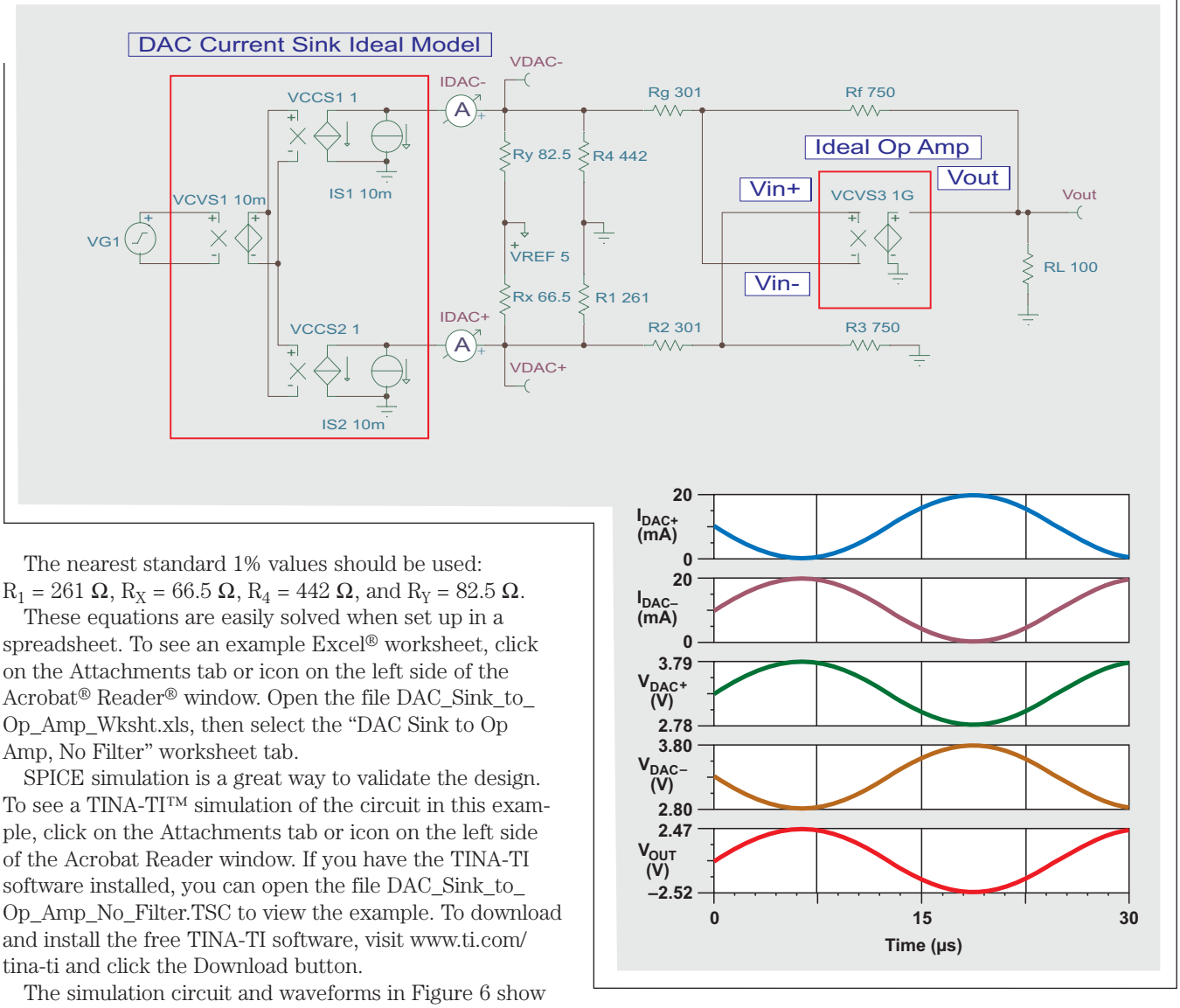
$$R_X = \frac{1}{\frac{1}{Z_{DAC+}} - \frac{1}{R_1} - \frac{1}{R_2+R_3}} = \frac{1}{\frac{1}{50\ \Omega} - \frac{1}{259.8\ \Omega} - \frac{1}{301\ \Omega+750\ \Omega}} = 65.8\ \Omega$$

$$R_4 = \frac{\frac{V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}+1}{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} + \left[\frac{V_{DAC+(min)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}-1\right]\left(\frac{1}{R_G}\right)}$$

$$= \frac{\frac{3.8\ V}{5\ V-3.8\ V}+1}{\frac{1-\frac{50\ \Omega\times1\times\frac{750\ \Omega}{301\ \Omega+750\ \Omega}}{301\ \Omega}}{50\ \Omega} + \left(\frac{2.8\ V\times1\times\frac{750\ \Omega}{301\ \Omega+750\ \Omega}-3.8\ V}{5\ V-3.8\ V}-1\right)\left(\frac{1}{301\ \Omega}\right)} = 447.2\ \Omega$$

$$R_Y = \frac{1}{\frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{Z_{DAC-}} - \left(\frac{1}{R_4}+\frac{1}{R_G}\right)} = \frac{1}{\frac{1-\frac{50\ \Omega\times1\times\frac{750\ \Omega}{301\ \Omega+750\ \Omega}}{301\ \Omega}}{50\ \Omega} - \left(\frac{1}{447.2\ \Omega}+\frac{1}{301\ \Omega}\right)} = 82.9\ \Omega$$

Figure 6. Simulation of current-sinking DAC interfaced to op amp



The nearest standard 1% values should be used: R_1 = 261 Ω, R_X = 66.5 Ω, R_4 = 442 Ω, and R_Y = 82.5 Ω.

These equations are easily solved when set up in a spreadsheet. To see an example Excel® worksheet, click on the Attachments tab or icon on the left side of the Acrobat® Reader® window. Open the file DAC_Sink_to_Op_Amp_Wksht.xls, then select the "DAC Sink to Op Amp, No Filter" worksheet tab.

SPICE simulation is a great way to validate the design. To see a TINA-TI™ simulation of the circuit in this example, click on the Attachments tab or icon on the left side of the Acrobat Reader window. If you have the TINA-TI software installed, you can open the file DAC_Sink_to_Op_Amp_No_Filter.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

The simulation circuit and waveforms in Figure 6 show that the circuit simulates as expected. I_{DAC+} and I_{DAC-} are the DAC currents, V_{DAC+} and V_{DAC-} are the voltages developed at the DAC outputs, and V_{OUT} is the output of the amplifier. The current-sinking DAC and op amp are ideal elements constructed with SPICE macros and are intended to show that the equations derived earlier for R_1, R_X, R_4, and R_Y are valid for ideal elements. Actual performance will vary depending on selected devices.

DAC image-filter considerations

The DAC output signal will have the desired baseband signal as well as the sampling images that occur at multiples of the sampling frequency. Filtering is usually used to reduce the amplitude of the sampling images because they degrade performance. Filtering directly at the DAC output before the op amp will preserve the best performance. This is especially important with multitone signals where second-order intermodulation products from the sampling images appear at the baseband.

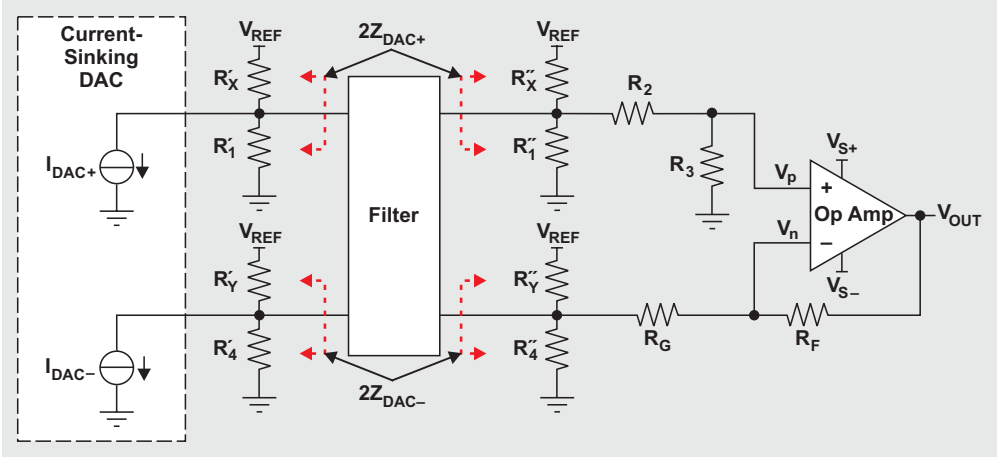
Filter design is not the topic of this article, so it will not be covered in much detail; but for proper operation the filter component values are calculated based on the input and output impedances seen by the filter. While finding the exact value of the impedance is not so troublesome, it is usually much easier to find standard component values to implement the filter when the input and output impedances to the filter are equal. With this in mind, let's now consider how to achieve the same goals as before while keeping the impedance seen by the filter balanced.

Figure 7 shows the proposed circuit implementation. R_1, R_X, R_4, and R_Y have been replaced with prime and double-prime components on either side of the filter, where

$R_1 = R'_1 \parallel R''_1$,
$R_X = R'_X \parallel R''_X$,
$R_4 = R'_4 \parallel R''_4$, and
$R_Y = R'_Y \parallel R''_Y$.

With the additional constraint that the impedance seen on each terminal of the filter is $2 \times Z_{DAC\pm}$, the following equations can be derived after quite a lot of algebra:

Figure 7. Inserting DAC image filter



$$\frac{1}{R'_1} = \frac{1}{2Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(max)}}-1}\right)} \quad \textbf{(12)}$$

$$\frac{1}{R''_1} = \frac{1}{2Z_{DAC+}\left(1+\frac{1}{\frac{V_{REF}}{V_{DAC+(max)}}-1}\right)} - \frac{1}{R_2+R_3} \quad \textbf{(13)}$$

$$\frac{1}{R'_X} = \frac{1}{2Z_{DAC+}} - \frac{1}{R'_1} \quad \textbf{(14)}$$

$$\frac{1}{R''_X} = \frac{1}{2Z_{DAC+}} - \frac{1}{R''_1} - \frac{1}{R_2+R_3} \quad \textbf{(15)}$$

$$\frac{1}{R'_4} = \frac{\left[1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{\frac{R_G}{2Z_{DAC-}}}\right]}{\frac{V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}+1} \quad \textbf{(16)}$$

$$\frac{1}{R''_4} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{\frac{R_G}{2Z_{DAC-}}} + \left[\frac{V_{DAC+(min)}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)-V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}-1\right]\left(\frac{1}{R_G}\right)}{\frac{V_{DAC-(max)}}{V_{REF}-V_{DAC-(max)}}+1} \quad \textbf{(17)}$$

$$\frac{1}{R'_Y} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{2Z_{DAC-}} - \frac{1}{R'_4} \quad \textbf{(18)}$$

$$\frac{1}{R''_Y} = \frac{1-\frac{Z_{DAC+}\times\alpha\left(\frac{R_3}{R_2+R_3}\right)}{R_G}}{2Z_{DAC-}} - \left(\frac{1}{R''_4}+\frac{1}{R_G}\right) \quad \textbf{(19)}$$

These equations are easily solved when set up in a spreadsheet. To see an example Excel worksheet, click on the Attachments tab or icon on the left side of the Acrobat Reader window. Open the file DAC_Sink_to_Op_Amp_Wksht.xls, then select the "DAC Sink to Op Amp, With Filter" worksheet tab.

SPICE simulation is a great way to validate the design. To see a TINA-TI simulation comparing results with a filter used in the circuit, click on the Attachments tab or icon on the left side of the Acrobat Reader window. If you have the TINA-TI software installed, you can open the file DAC_Sink_to_Op_Amp_With_Filter.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button. To show

the effects of balancing the filter impedance, a 100-MHz differential filter designed for 100-Ω input and output impedance is inserted into the interface of the DAC and op amp. In the top circuit, the filter is inserted between the bias resistors and amplifier gain resistors with no regard for balancing the impedance; the output is labeled "V_{OUT} No Match1." In the bottom circuit, the filter is inserted between the DAC and the bias resistors with no regard for balancing the impedance; the output is labeled "V_{OUT} No Match2." In the center circuit, the bias network is designed for 100-Ω balanced impedance; the output is labeled "V_{OUT} Matched." The transient simulation waveforms look the same as those shown in Figure 6 for each of these circuits, but simulation of an AC transfer function (see Figure 8) shows that the unmatched implementations result in significant ripple in the frequency response while the matched design performs as desired.

During design of the Texas Instruments TSW3070 evaluation board, a circuit was derived as shown in Figure 9 that appears to be well-balanced and that provides for proper impedance matching to the

Figure 8. Simulation of AC transfer function with matched vs. unmatched filter implementations

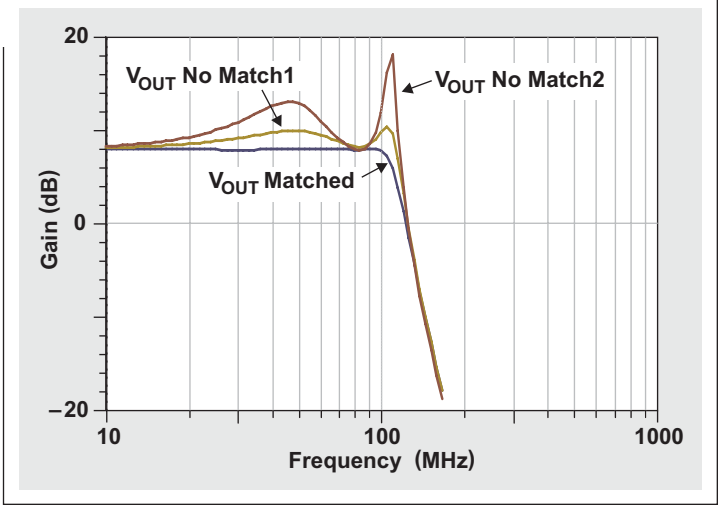
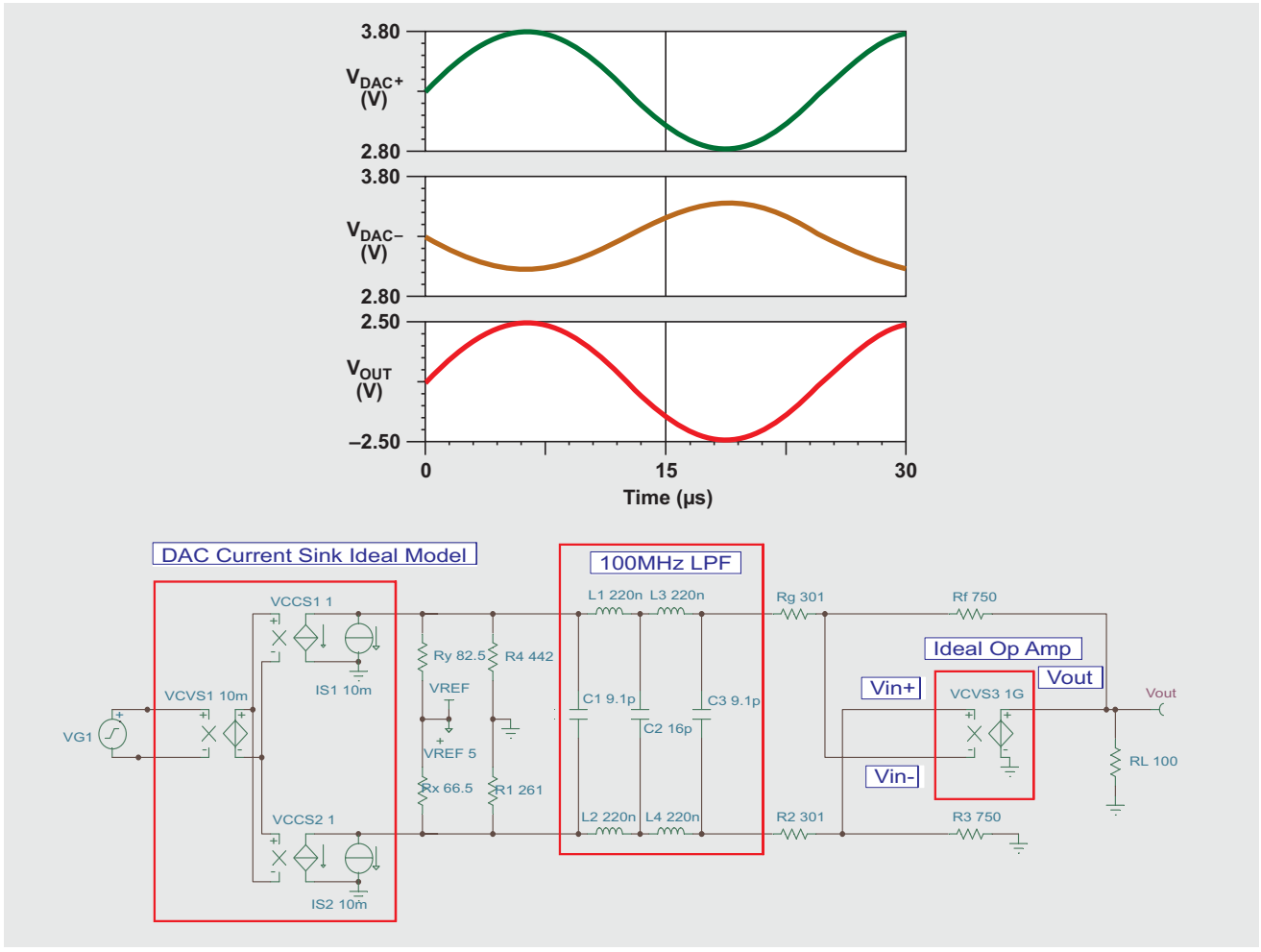


Figure 9. Original TSW3070 circuit simulation (not balanced)



100-MHz low-pass filter (LPF). However, the circuit's simulation waveforms show that the impedances seen by the outputs of the DAC are not balanced and that the voltage at V_{DAC+} is not the mirror image of that at V_{DAC-}. Per the last example given, this circuit was modified to balance the impedances for the DAC and the LPF. Performance of the second and third harmonics was tested before and after the modification, and the results (shown in Figure 10) show as much as a 10-dB improvement in the second harmonics (depending on the frequency) with basically no change in the third harmonics.

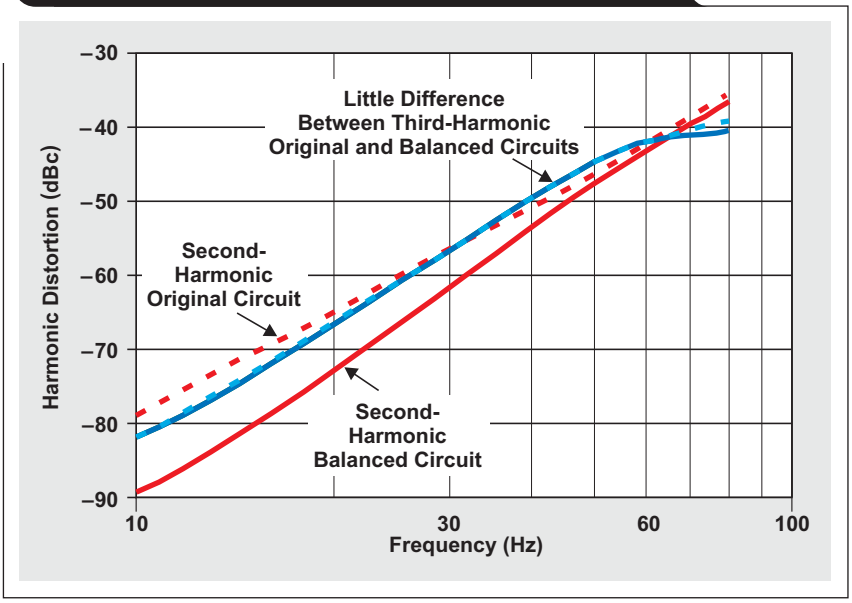
Conclusion

This article has shown a circuit implementation using a single-stage op amp to convert complementary-current outputs from a current-sinking DAC to a single-ended voltage. Equations were derived and a methodology presented for proper selection of component values to set the DAC's output-voltage compliance while maintaining balanced input signals to the op amp for best overall performance. Filter-design considerations were also included to explain proper insertion when filtering before the amplifier is desired.

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with DAC5675A, DAC5681, DAC5682Z, DAC5686, DAC5687, DAC5688, or THS3095
www.ti.com/tina-ti
www.ti.com/tsw3070

Figure 10. Harmonic distortion with balanced versus unbalanced impedance



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