

**YORK UNIVERSITY**

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

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# **SKY130 CMOS Readout Array Design for Scalable Nanopore-Based DNA Sequencing**

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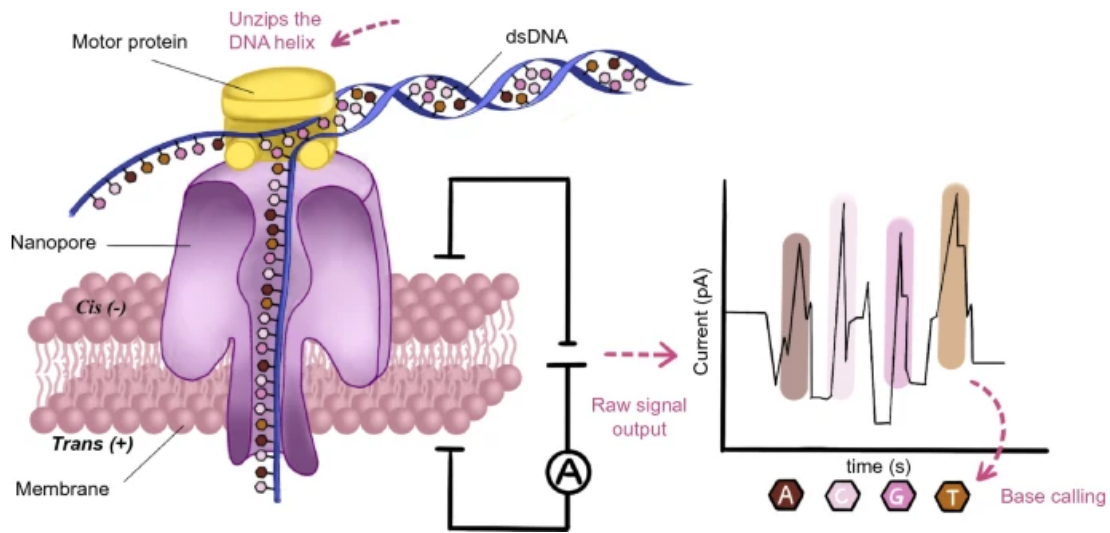
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## Motivation

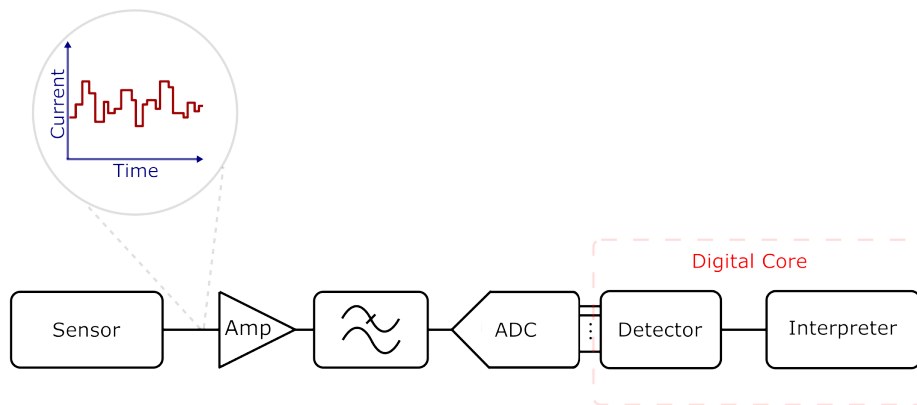
Nanopore sequencing involves the use of nanopores, which can be biological or solid-state, to determine the order of nucleotides in DNA by electrically measuring the movement of the DNA through the nanopore. Nanopores are tiny apertures at the nanometer scale, directing molecules to precise spatial locations. Electrically, nanopores function as voltage-clamp sensors, with a constant voltage applied across them to establish an ionic current. As illustrated in Fig. 1, DNA is threaded through the nanopore during sequencing, causing modulation of the ionic current in a complex relationship to the sequence of base molecules (A, C, G, T) in the DNA strand.



**Figure 1:** Illustration of the nanopore-based sequencing process [1].

In the field of modern biotechnology, nanopore DNA sequencing stands out as a remarkable and scalable method for nucleotide identification, leveraging current fluctuations as DNA molecules traverse through minuscule nanopores. The emergence of biological nanopore sensors underscores the urgent need for Digital Read-out Integrated Circuits (DROIC) capable of rapidly and accurately preparing these ultra-sensitive nanopore signals for digital analysis. The nanopore readout system requires highly sensitive amplifiers, which presents a challenge in integrating the readout circuitry. The noise generated by the analog-to-digital converters (ADCs) can couple into these sensitive amplifiers through various paths such as the substrate, power supply, or voltage references. To address this issue, a Discrete Time (DT) amplifier with digital correlated double sampling (CDS) has been introduced to mitigate flicker and  $kT/C$  noise [2]. However, the noise introduced by the digital readout circuitry remains uncorrelated, making it unable to be eliminated by CDS techniques. To minimize noise originating from the readout

circuitry, it is crucial to conduct the readout outside of the sampling phase; otherwise, it may distort the measured signal. Moreover, there is a growing demand for array-based structures to enable simultaneous DNA measurements [3]. Although the design and realization of high-performance read-out components for biosensors remain a critical objective, their arrangement into a high-throughput parallel-channel array is arguably even more important in today's rapidly evolving bio-technological landscape. Fig. 2 indicates a simplified block diagram illustrating one channel of the DROIC. Motivated by these challenges, we have engineered an ultra-low noise, low-power DROIC architecture in SKY130 technology equipped with on-chip Analog-to-Digital Converters (ADCs), strategically embedded within each column of the array. This innovative design not only facilitates scalability to accommodate hundreds or even thousands of channels but also ensures parallel operation to efficiently digitize input analog signals. Notably, the compact footprint of the individual channels sets our approach apart from existing nanopore DNA sequencing technologies. Furthermore, post-digitization, the serialized digital data from all ADCs undergoes meticulous processing to decode DNA bases from the binary stream, enabling precise determination of the DNA molecule's sequence (A, C, G, and T). Furthermore, we have implemented simultaneous integration and sampling through a specific methodology detailed in the patent [4]. This approach allows for both processes to occur concurrently, enhancing the efficiency and performance of the readout system.

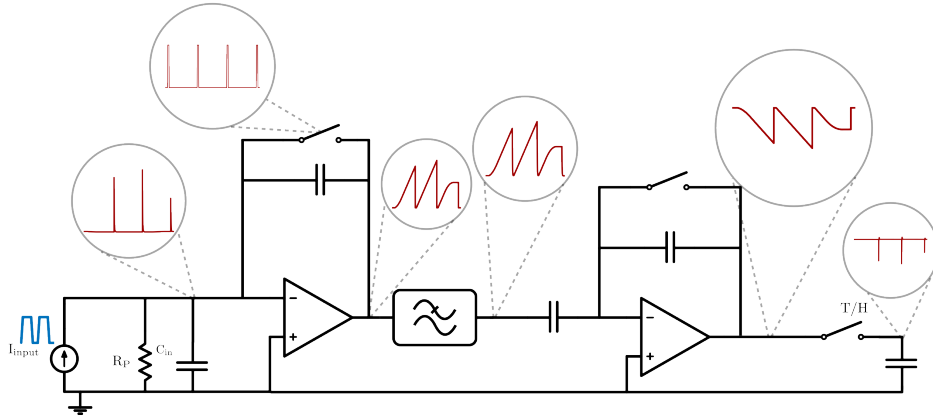


**Figure 2:** A simplified block diagram of DROIC.

## Description

In the Analog Front End (AFE), the discrete-time Transimpedance Amplifier (DT-TIA) functions as a current-to-voltage converter. Following the DT-TIA, a Low-Pass Filter (LPF) is utilized to enhance the noise performance of the signal processing chain. It achieves this by attenuating

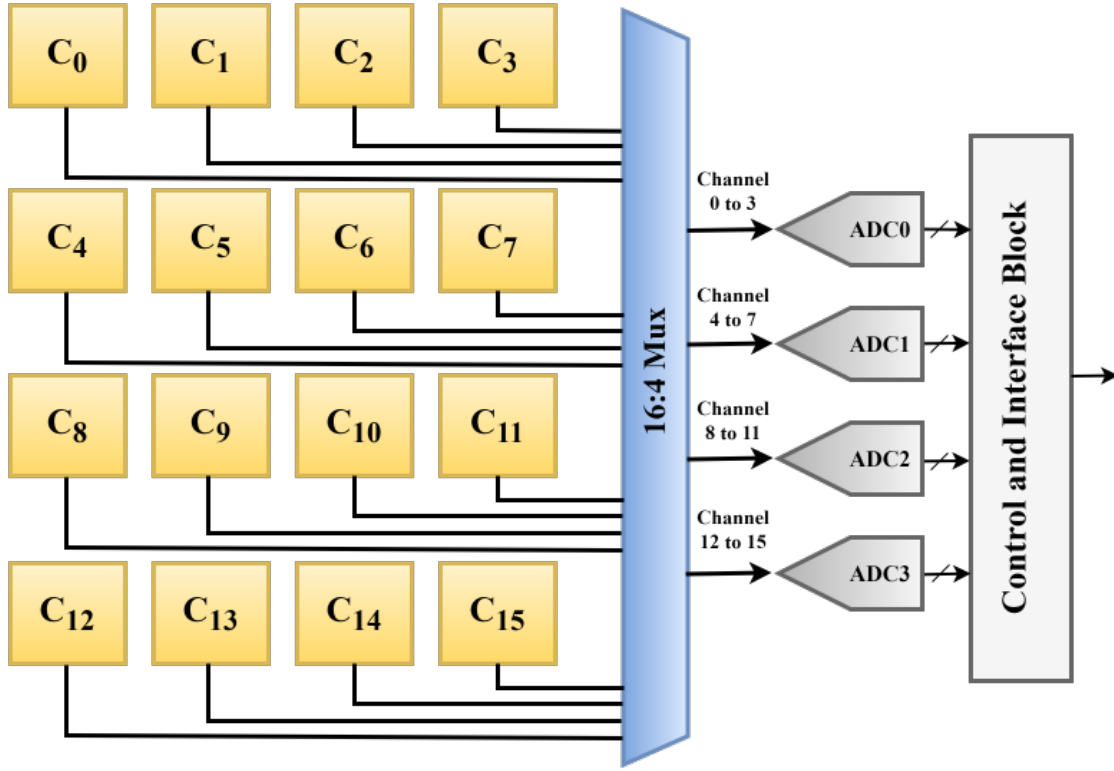
high-frequency noise contributions to the output signal and, from a sampled-system perspective, fulfills the anti-aliasing function. Lastly, the active Correlated-Double Sampler (CDS) block is integrated to mitigate flicker noise, charge injection, and  $kT/C$  noise Fig. 3.



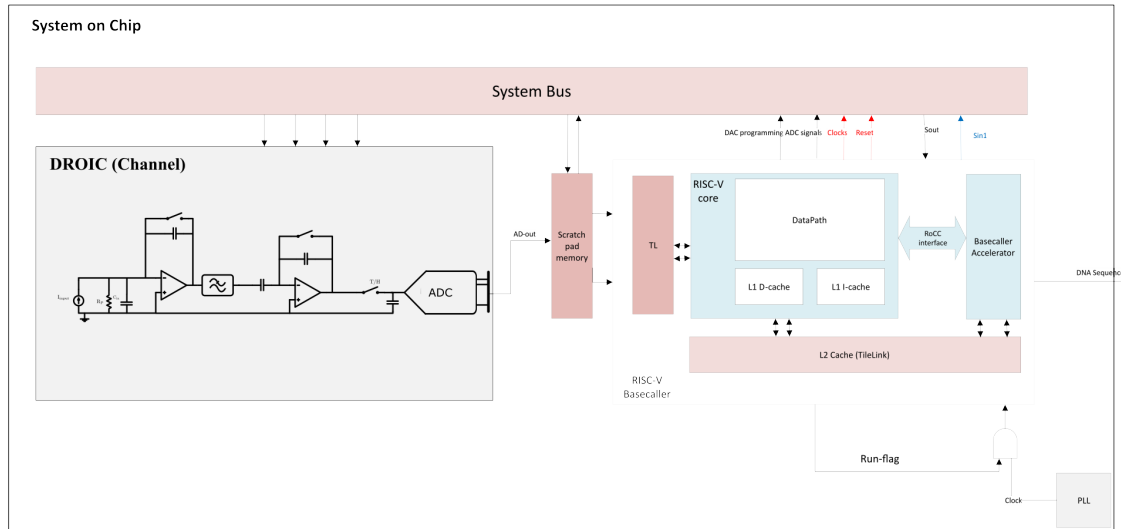
**Figure 3:** The DT analog front-end (AFE).

The project presents a System on Chip (SoC) comprising a high-speed, low-power mixed-signal readout array. The proposed Digital Read-Out Integrated Circuit (DROIC) system features a channel array capable of simultaneous amplifying, filtering, and digitizing pico-ampere range current signals with high accuracy and speed. Illustrated in Fig. 4 is the block diagram showcasing the analog and digital components for nanopore-based DNA sequencing. A key innovation of this design lies in implementing a novel readout method in each channel, resulting in reduced power consumption compared to previous works.

In the context of readout systems for biosensors, enhancing channel density refers to increasing the number of measurement channels within a given area or space. By implementing column ADCs (Analog-to-Digital Converters), multiple amplifiers can share a single ADC, effectively multiplexing the input signals. This approach optimizes the utilization of space on the integrated circuit while allowing for efficient signal processing and data acquisition from multiple channels simultaneously. Following the analog signal processing, the digital output from the Analog-to-Digital Converters (ADCs) undergoes conversion into digital samples, which are then serialized and transmitted to memory. This serialized data is subsequently retrieved by the RISC-V processor, depicted in Figure 3, where it undergoes basecalling algorithm execution, shown in Fig. 5.



**Figure 4:** Block diagram of readout array architecture.



**Figure 5:** An overview of the proposed system on chip (with only one measurement channel) for DNA sequencing, including Digital Read-Out circuitry, a temporal memory and the RISC-V basecaller.

## Design Goals

Digital Readout integrated circuits (DROICs) act as the intermediary between sensors and the computing systems responsible for interpreting their data. Their primary function is to amplify, filter, and digitize sensor signals. In contemporary and evolving DNA and biomolecular

measurement setups, DROICs are increasingly tasked with accommodating extensive sensor arrays. The project aims to develop and implement ultra-low noise and low-power analog front-end circuitry customized for the amplification and filtering of nanopore signals in the SKYWater 130-nm Technology. This will involve the integration of on-chip analog-to-digital converters (ADCs) to digitize the amplified signals with high accuracy and speed. Additionally, the project will focus on developing a parallel processing scheme to enable efficient data transmission and analysis. The performance of the 4 by 4 readout array will be comprehensively assessed, with a specific focus on noise, power consumption, speed, and scalability using the gm/id method. Ultimately, the goal is to contribute to the advancement of genomic research and biotechnology by addressing existing challenges in readout system design and realizing efficient, high-throughput DNA sequencing platforms with widespread applications across various domains.

## Bibliography

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