European Research Infrastructure supporting Smart Grid Systems Technology Development, Validation and Roll Out

Work Package 08

JRA2 - Co-Simulation based Assessment Methods

Report on

Selected Test Case Descriptions

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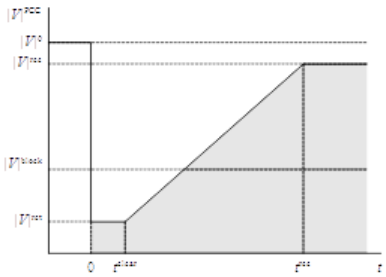
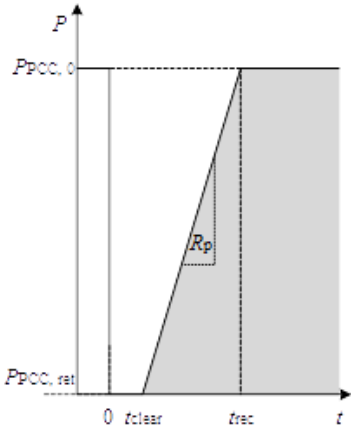
1 Test Case Specification for TC1

1.1 Test Case

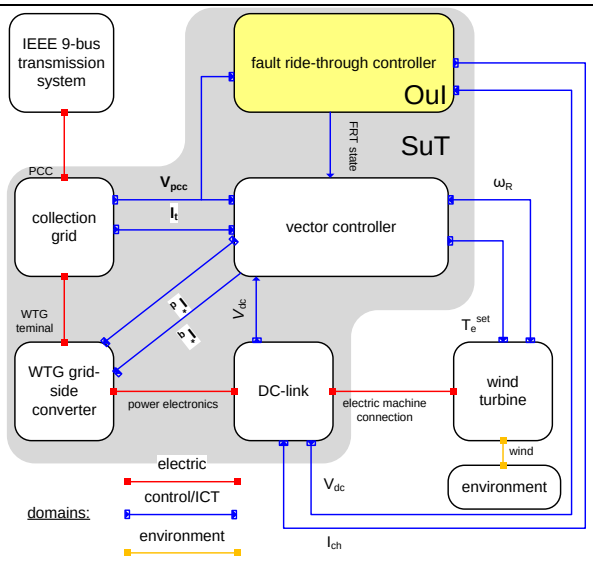
Name of the Test Case	JRA2-TC1
Narrative	This test case aims to study and evaluate cyclic dependencies between continuous simulators. The interaction between electricity network and converter interfaced devices is of main interest in this test case as converters generally exhibit non-linear behaviour during faults. The experiments in the test case verify the low-voltage ride through capability of an onshore wind power plant (WPP) that is interconnected to a small transmission system. The WPP comprises type 4 wind turbines, which have a fully rated converter interface. The wind power plant must comply to the grid code specification of a low-voltage ride through time against voltage profile. This profile stipulates at the coupling location the minimum profile at which the WPP must stay connected.
Function(s) under Investigation	The fault ride through capability of the converter, fast reactive power support, active power recovery by the WTGs.
Object under Investigation	The fault ride through capability of the converter, fast reactive power support, active power recovery by the WTGs
Domain under Investigation	• Electrical • Control/ICT • Environment
Purpose of Investigation	Verification of the converter dynamics and the converters' capability to comply to the FRT curves after a 3-phase short circuit upstream in the (sub-)transmission system, causing a voltage dip at the coupling point of the WPP.
System under Test	The wind park (collection system plus WTG) is treated by the system operator as one single entity, the wind power plant. The FRT curve is enforced at the coupling point, whereas the grid interface of the converter, its controls, protection, and electromechanical conversion components ensure the compliance to this curve. Hence, the SuT comprises: • the coupling point • the collection grid • the step-up transformers • the converters • the WTG converters • the WTG FRT controller • the WTG protection schemes • the WTG DC links • the WTG electrical machine
Functions under Test	• FRT functionality of the converter • fast reactive power support • physical response of external system interacting with OuI • post fault active power recovery functionality • normal operating controls of the WTGs • current limit of the converters • direct voltage control of the DC link of the wind turbine
Test criteria	• converter must stay connected during and after the fault

		• direct voltage operating region is not violated • WTGs remain synchronised to the grid • Transient and frequency stability must be maintained
	target metrics (test factors)	FRT curve: • WPP must stay connected • WPP may temporarily disconnect from transmission system  Active power recovery curve: • WTG has to comply to minimum ramping active power rate 
	variability attributes	• short circuit duration (primary versus backup protection)
	quality attributes (thresholds)	FRT curve tests: • short duration (200ms), deep dip • criteria are fulfilled in case FRT controls keep direct voltage and WTG speed within design boundaries, and phase locked loop (PLL) maintains synchronisation.

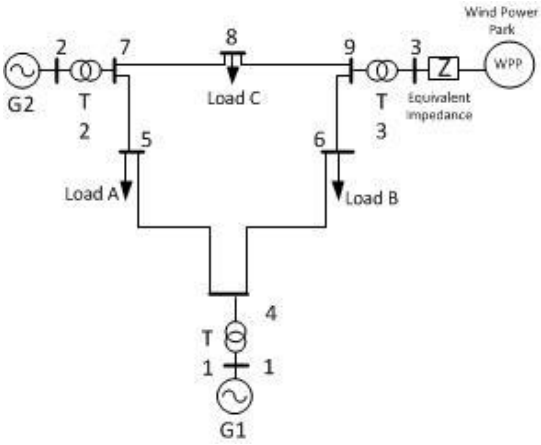
1.2 Qualification Strategy

1.2.1 Test Specification JRA2-TC1.TS1

Reference to Test Case	JRA2-TC1
Title of Test	Monolithic simulation of JRA2-TC1
Test Rationale	Perform and evaluate a monolithic simulation of JRA2-TC1.
Specific Test System (graphical)	Test-specific SuT:



Test system setup:



In the grid configuration above, generator G3 is replaced by an aggregated WPP via an equivalent impedance.

Please consider the grid configuration in the test case descriptions as a reference. The variables between the components are the domain specific interface variables. The connections in the control domain have a directional component. The type, descriptions, and units of the interfacing variables inside the test system are described below:

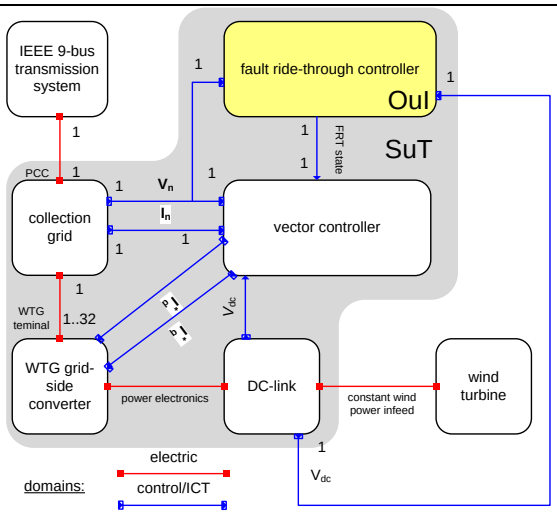
- V_{pcc}: 3x1 array with nodal voltages [V]
- I_t: 3x1 array with equivalent branch currents [A]
- I_d: 3x1 array with converter currents [A]
- I_q: 3x1 array with converter currents [A]
- V_{dc}: voltage between + and – pole [V]
- I_{lim}: limiting scheme (0=no limiting, 1=d-axis priority, 2=q-axis priority,3=proportional limiting) [-]
- K_{aRCI}: additional reactive current injection gain [p.u.]
- R_p: active power recovery ramp rate [p.u./s]
- R_{on}: ramp rate on/off [-]
- p_{rot}: chopper on/off [-]

Target measures	• FRT curve compliance • WPP remain synchronized to transmission grid • Correct initialization of converter controller and FRT controller

	• Direct Voltage operating region is not violated
Input and output parameters	Controllable input parameters: • fault duration • fault location • FRT control mode (on/off) Uncontrollable parameters: • voltage at coupling point implicitly set by the fault characteristics • wind turbine rotor speed Measured parameters: • DC voltage, • phase angle of PLL
Test Design	• determine operating point • set short circuit location to x • initiate short circuit at t=1 • clear fault at t=y • assess test criteria
Initial system state	WPP replaces G3 from IEEE 9 bus system inheriting it's operating point (P,Q at coupling point)
Evolution of system state and test signals	Test events: See test design. Target metrics: All deterministic cases (so all test criteria for all parameter variations) must be successful. Internal boundary conditions: The IGBT current limit of the converter is 110% of the rated current, the minimum active power recovery rate is 5 p.u./s, i.e., in 200 ms the wind turbines must be able to recover to the pre-fault power output. The wind turbine speed and the corresponding pitch controller are not modelled. Their boundaries and time constants are hence not taken into consideration for FRT operation.
Other parameters	N/A
Temporal resolution	• time constants inside SuT in between 50 µs and 5 s • continuous simulation, time step size depends on software experiment • components exhibit physical behaviour, the FRT controller is a discrete controller (state machine)
Source of uncertainty	N/A
Suspension criteria / Stopping criteria	• violation of WTG synchronism with grid • transient and frequency stability is violated

1.2.2 Test Specification JRA2-TC1.TS2

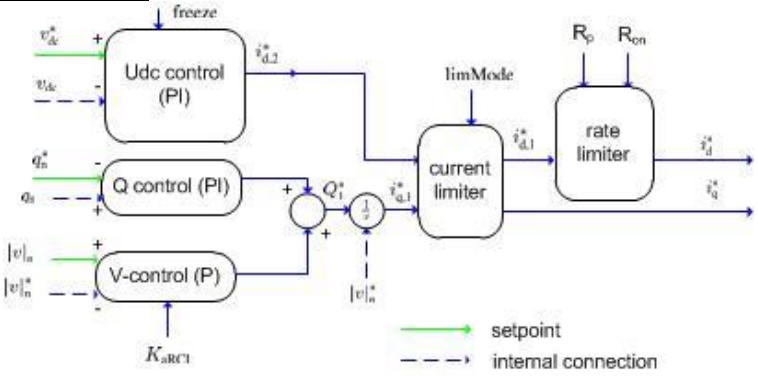
Reference to Test Case	JRA2-TC1
Title of Test	Co-simulation of JRA2-TC1
Test Rationale	Perform and evaluate a co-simulation with the power system, the FRT controller and the converter controller implemented in separate models.
Specific Test System (graphical)	Test specific SuT:



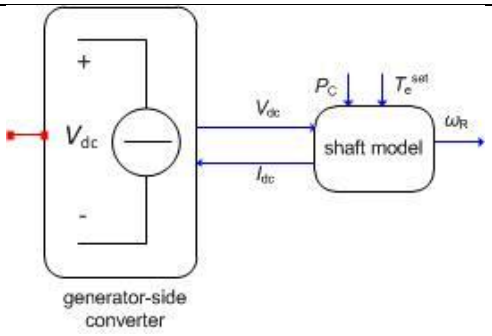
The variables between the components are the domain specific interface variables. The connections in the control domain have a directional component. The type, descriptions, and units of the interfacing variables inside the test system are described below:

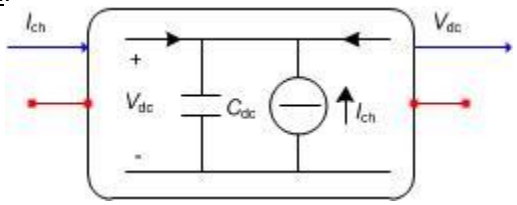
- V_{pcc}: 3x1 array with nodal voltages [V]
- I_t: 3x1 array with equivalent branch currents [A]
- I_d: 3x1 array with converter currents [A]
- I_q: 3x1 array with converter currents [A]
- V_{dc}: voltage between + and – pole [V]
- I_{lim}: limiting scheme (0=no limiting, 1=d-axis priority, 2=q-axis priority, 3=proportional limiting) [-]
- K_{aRCI}: additional reactive current injection gain [p.u.]
- R_p: active power recovery ramp rate [p.u./s]
- R_{on}: ramp rate on/off [-]
- p_{rot}: chopper on/off [-]

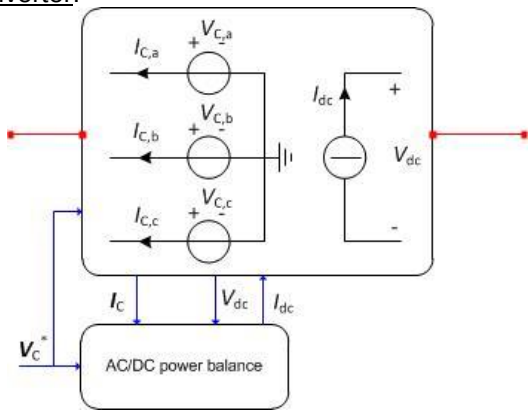
Vector Controller:

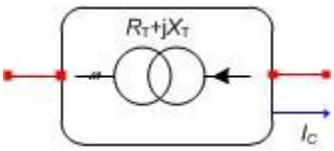


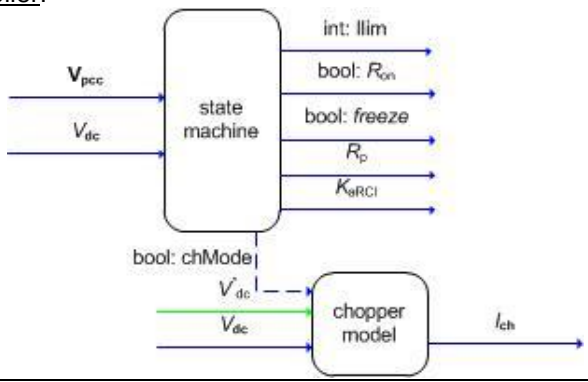
Wind Turbine Model:

<table>
<tr><td></td><td>


DC Link Model:


Grid Side Converter:


Collection Grid:


FRT Controller:


</td></tr>
<tr><td>Target measures</td><td>

FRT curve compliance
WPP remain synchronized to transmission grid
correct initialization of converter controller and FRT controller
direct voltage operating region is not violated

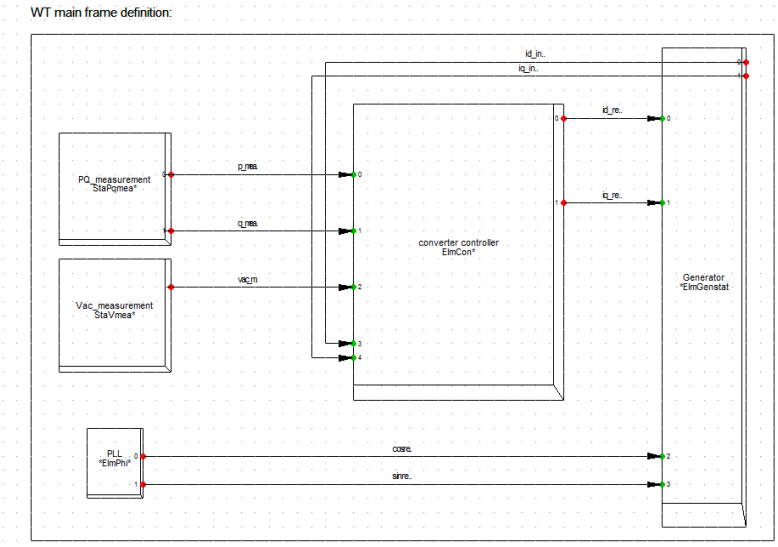
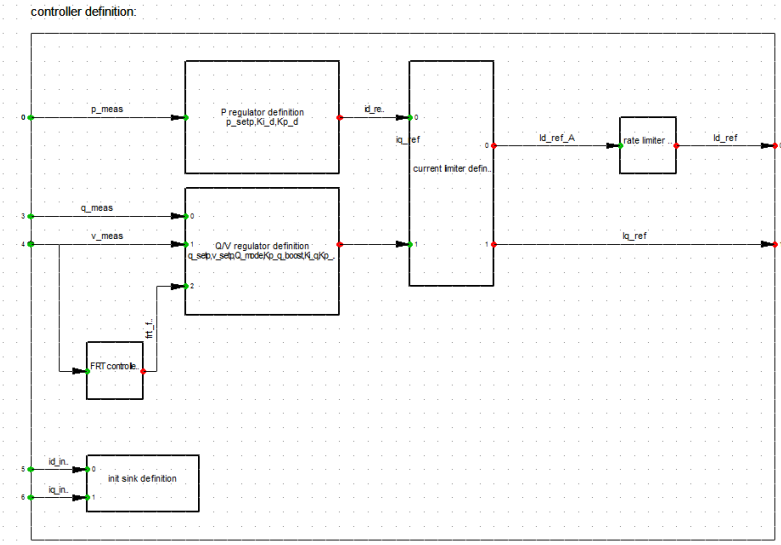
</td></tr>
<tr><td>Input and output parameters</td><td>Controllable input parameters:</td></tr>
</table>

	• fault duration • fault location • FRT control mode (on/off) Uncontrollable parameters: • voltage at coupling point implicitly set by the fault characteristics • wind turbine rotor speed Measured parameters: • DC voltage • Id and Iq currents
Test Design	• determine operating point • set short circuit location to x • initiate short circuit at t=1 • clear fault at t=y • assess test criteria
Initial system state	WPP replaces G3 from IEEE 9-bus system inheriting it's operating point (P,Q at coupling point)
Evolution of system state and test signals	Test events: See test design. Target metrics: All deterministic cases (so all test criteria for all parameter variations) must be successful. Internal boundary conditions: • IGBT current limit of the converter is 110% of the rated current • minimum active power recovery rate is 5 p.u./s, i.e., in 200 ms the wind turbines must be able to recover to the pre-fault power output. The wind turbine speed and the corresponding pitch controller are not modelled. Their boundaries and time constants are hence not taken into consideration for FRT operation.
Other parameters	N/A
Temporal resolution	• time constants inside SuT in between 50 µs and 5 s • continuous simulation, time step size depends on software experiment • components exhibit physical behaviour, the FRT controller is a discrete controller (state machine)
Source of uncertainty	N/A
Suspension criteria / Stopping criteria	• Violation of WTG synchronism with grid • If transient and frequency stability is violated

1.3 Mapping Strategy

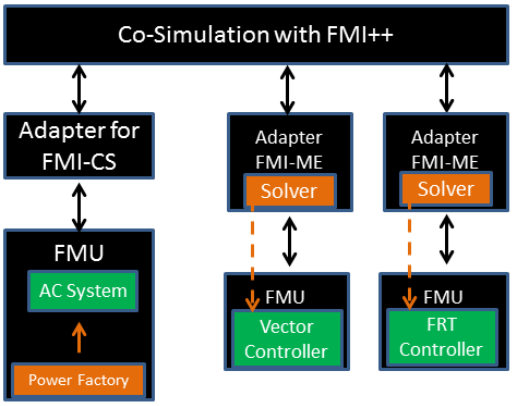
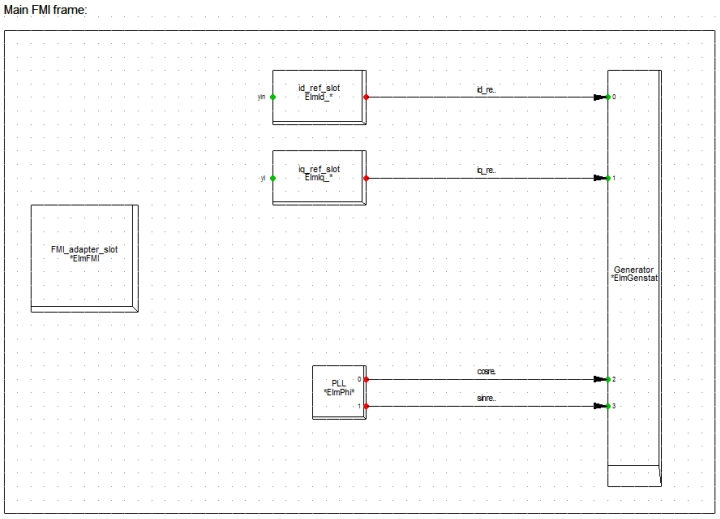
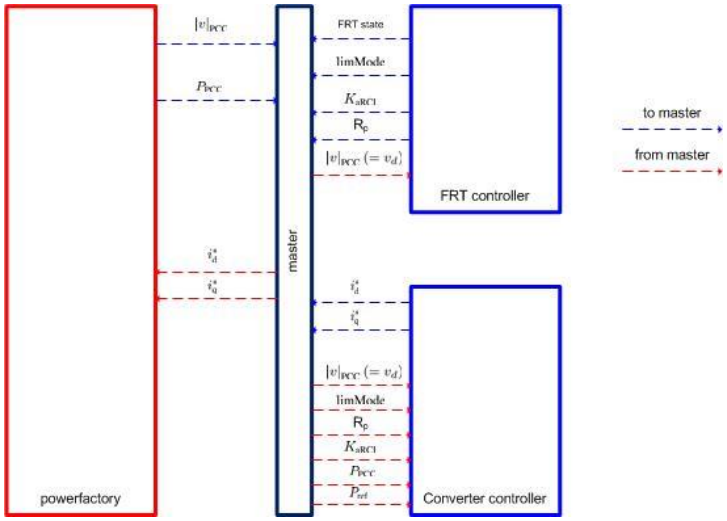
1.3.1 Experiment Specification JRA1-TC1.TS1.monolithic

Reference to Test Specification	JRA2-TC1.TS1
Title of Experiment	Monolithic Simulation Using PowerFactory
Experiment Realisation	A monolithic simulation approach is applied for simulating the entire test case in DIgSILENT Power Factory. The models are developed and simulated in PowerFactory.

Experiment Setup (concrete lab equipment)	Vector Controller:  Wind Turbine Frame: 
Experimental Design and Justification	• 3-phase short circuit location: bus 4 • variation of fault duration: 200ms
Precision of equipment	N/A
Uncertainty measurement	N/A
Storage of data	Simulations results are stored in PowerFactory for further analysis.

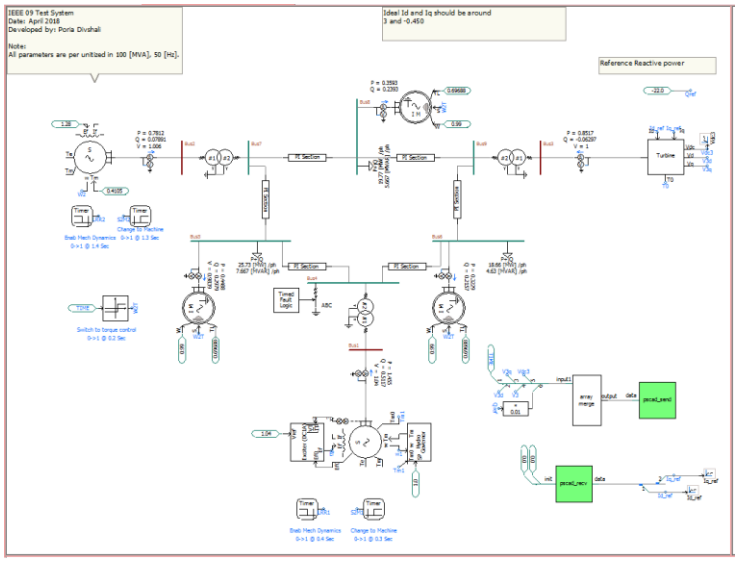
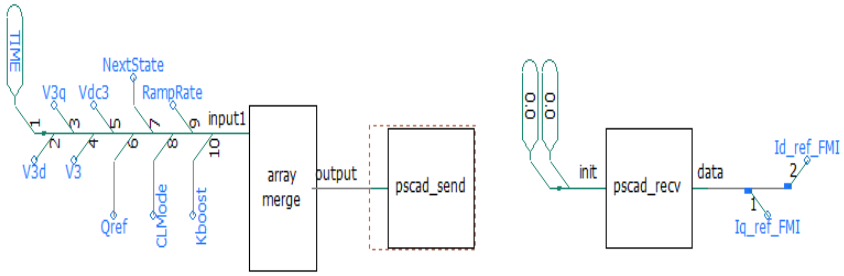
1.3.2 Experiment Specification JRA1-TC1.TS2.powerfactory-simulink

Reference to Test Specification	JRA2-TC1.TS2
Title of Experiment	Co-Simulation of PowerFactory and Simulink using the FMI++ Python Interface

Experiment Realisation	The FMI++ Python Interface is used to perform a co-simulation between Simulink and PowerFactory. The controller converter and FRT controller are modelled in Simulink. The IEEE 9-bus system, the collection grid, and the grid interface of the aggregated wind turbine are modelled in the RMS partition of PowerFactory, with control signals coming from the other FMUs
Experiment Setup (concrete lab equipment)	Co-simulation setup:  PowerFactory wind turbine frame (with I_d and I_q control):  PowerFactory co-simulation IO interface: 

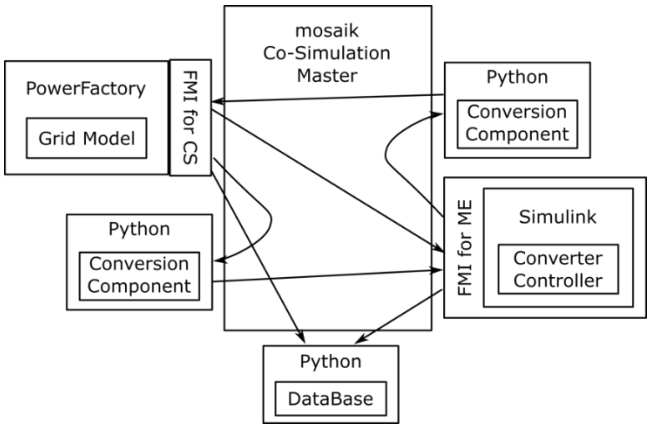
Experimental Design and Justification	• 3-phase short circuit location: bus 4 • variation of fault duration: 200ms
Precision of equipment	N/A
Uncertainty measurement	N/A
Storage of data	For further evaluation, recorded data points are stored in a CSV file on the simulation host.

1.3.3 Experiment Specification JRA1-TC1.TS2.pscad-simulink

Reference to Test Specification	JRA2-TC1.TS2
Title of Experiment	Co-simulation of PSCAD and Simulink using the FMI++ Python Interface
Experiment Realisation	The WTG controllers, including the FRT and converter controller, are modelled in Simulink and are exported as FMUs for ME. The transmission system, i.e., the dynamic IEEE 9-bus system, along with the WPP are modelled in PSCAD. The synchronous generator G3 is replaced by a WTG, which is modelled in PSCAD by a converter. The entire PSCAD simulation is exported as an FMU for CS, using the psacad_send and pscad_recv blocks, developed for the co-simulation interface of PSCAD. All FMUs are connected via the FMI++ Python Interface.
Experiment Setup (concrete lab equipment)	Co-simulation setup: • analogous to JRA2-TC1.TS2.powerfactory-simulink PSCAD system model:  PSCAD co-simulation IO interface: 
Experimental Design and Justification	• 3-phase short circuit location: bus 4variation of fault duration: 200ms

Precision of equipment	N/A
Uncertainty measurement	N/A
Storage of data	For further evaluation, recorded data points are stored in a CSV file on the simulation host.

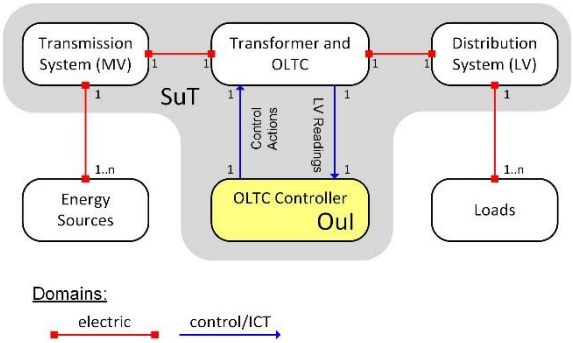
1.3.4 Experiment Specification JRA1-TC1.TS2.mosaik

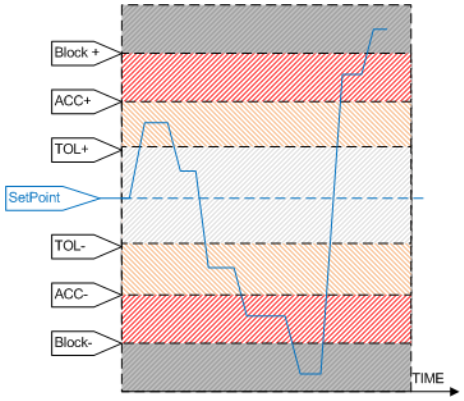
Reference to Test Specification	JRA2-TC1.TS2
Title of Experiment	Co-Simulation of PowerFactory and Simulink using mosaik
Experiment Realisation	Analogous to JRA1-TC1.TS2.powerfactory-simulink, only that mosaik is used to couple the FMUs.
Experiment Setup (concrete lab equipment)	Co-simulation setup:  Otherwise analogous to JRA1-TC1.TS2.powerfactory-simulink.
Experimental Design and Justification	Analogous to JRA1-TC1.TS2.powerfactory-simulink.
Precision of equipment	N/A
Uncertainty measurement	N/A
Storage of data	The outputs from the individual simulation components are stored as time series data (HDF5 data format).

2 Test Case Specification for TC2

2.1 Test Case

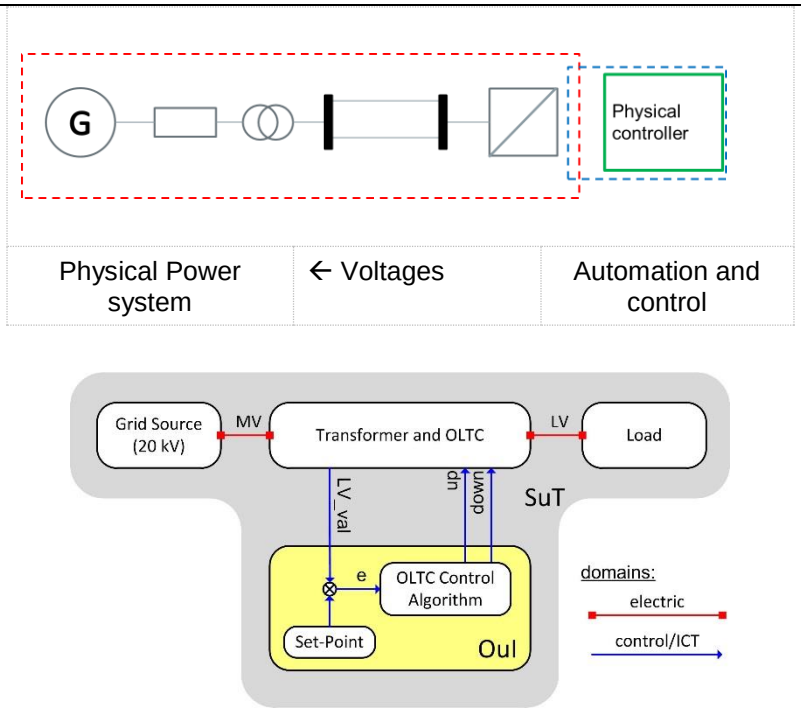
Name of the Test Case	JRA2-TC2
Narrative	OLTC transformer setups including the required control logic need thoughtful validation and testing beyond monolithic simulations. The purpose of this test case is to have the first step towards the implementation of a control block using FMU for ME functionality. In addition, an interface between a simulated part of the power system and a physical device can be carried out, using an embedded controller board such as an Arduino, in which data exchange is performed in both directions. Closed-loop voltage regulation can be implemented using not only a simulated controller but also using a physical controller embedded in an Arduino card.
Function(s) under Investigation	The focus of this investigation is the voltage control function for the OLTC transformer.

Object under Investigation	• OLTC controller
Domain under Investigation	• Electrical & electronic domains • Control / ICT domain
Purpose of Investigation	The described tests aim at verifying the functionality of various OLTC controller realizations. Each realization covers a different design and development stage of the controller under test. Especially, the capability of the OLTC controller realizations to successfully maintain the terminal voltage at the low voltage side of the transformer within the specified boundaries is evaluated. Certain controller realizations, such as the encapsulation into an FMU or a realization by an embedded device, may impose major challenges and may influence the behaviour of the controller. In order to characterize each realization and to verify whether the control logic is still functional, the experiments described below will be performed.
System under Test	The OLTC, its electrical vicinity, and its corresponding control algorithm comprise the SuT. The relevant sub-systems are: • grid supply • voltage sensor • transformer • OLTC control block • actuators that operate the OLTC • load • communication links between the controls and the transformer The following system diagram illustrates the interaction of the major system components. 
Functions under Test	• OLTC control functionality • voltage regulation within the admissible limits • control functionality implemented in an embedded hardware device (Arduino card) • control functionality exported into an FMU for ME
Test criteria	• OLTC control block must be able to exchange data with other blocks within the specified time-step using its software/physical versions of implementation • voltage operation region not violated
target metrics (test factors)	Voltage regulation regions (LV):

		
	variability attributes	• low-voltage set-point • load variations • medium-voltage variations
	quality attributes (thresholds)	A voltage variation test outcome is considered to be positive if and only if: • the admissible voltage range of [TOL-, TOL+] is re-established and maintained within the first 10 s after the induced disturbance, and • the system operates without system disconnections (shutdowns).

2.2 Qualification Strategy

2.2.1 Test Specification JRA2-TC2.TS1

Reference to Test Case	JRA2-TC2
Title of Test	Voltage Control Function Assessment
Test Rationale	This test aims at verifying the behavior of various OLTC controller implementations in the context of the SuT. It specifically targets the interaction of the OuI with surrounding system components and the resulting control actions.
Specific Test System (graphical)	

The types, descriptions, and units of the interface variables are as follows:

Name	Unit	Description
MV	[V]	Nodal voltages
LV	[V]	Nodal voltages
LV_val	[V]	Voltage measurement
set-point	[V]	Voltage set-point
e	[V]	Voltage error
up	[-]	Next transformer level (coil)
down	[-]	Previous transformer level (coil)

Target measures

- controller low voltage

Input and output parameters

Controllable input parameters:

- voltage set-point
- load value
- delays

Uncontrollable input parameters:

- transformer taps
- main source voltage value
- frequency.

Measured parameters:

- load voltage value
- controller states with respect to “target metrics” (see table below)

Concept	Value	unit	Notes
SetP	420	V	Set point
Tap Step	2.5%*	V	Tap Step
BLQ+	50%*	V	Block Control
ACC+	5%*	V	Step down (Delay)
TOL+	+1%*	V	Step Down
TOL-	- 1%*	V	Step Up
ACC+	-5%*	V	Step Up (Delay)
BLQ-	-50%*	V	Block Control

* depends on the rates of the deployed transformer

Test Design

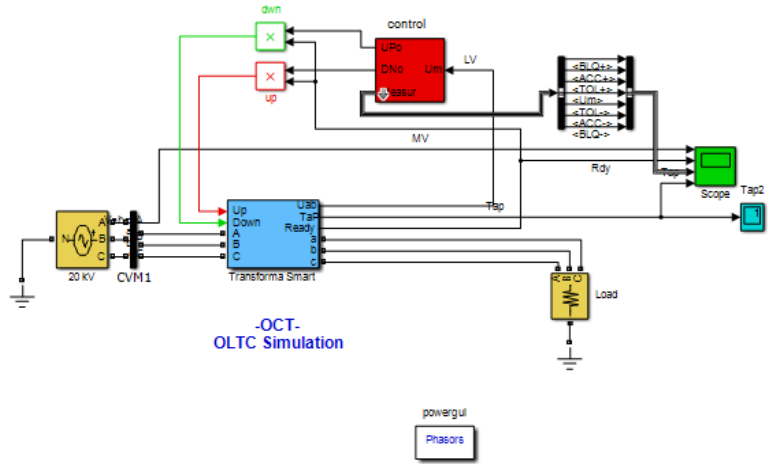
The test aims at validating and verifying the voltage control functionality of the controller in various experiments. The controller must be able to maintain a low voltage value within a certain voltage region. In order to assess the functionality, first, a predefined set of border cases will be applied. In each test iteration one input variation from the predefined set is chosen. The test criteria defined above will then be applied to evaluate each test run. The predefined set of inputs features an improved comparability of the experiments. If a test iteration shows difficulties, such as failed test criteria, additional test iterations with manually adjusted inputs will be scheduled. Such additional test iterations are used to gain further insights. Since the controllable inputs of each test run are mostly defined beforehand, a systematic/factorial test is performed. In particular, the following steps will be executed in each experiment:

	1. determine the operating set-point 2. wait until the output is stabilized 3. vary the MV input voltage and/or the set-point according to the current border case 4. assess test criteria 5. repeat 2-4 until all predefined border cases are tested The following border cases are defined: • maximally decrease MV input voltage, use constant voltage set-point • maximally increase MV input voltage, use constant voltage set-point • decrease voltage set-point from maximal to minimal value, do not artificially vary MV input voltage • increase voltage set-point from minimal to maximal value, do not artificially vary MV input voltage
Initial system state	Initial power flow conditions: • Load voltage value (output) = voltage set-point
Evolution of system state and test signals	The test is successful in the case of the load voltage is always regulated within the interval [TOL-, TOL+] in both cases soft/hard OLTC control regardless of load voltage variation.
Other parameters	N/A
Temporal resolution	The simulation of virtual components uses fixed time steps of 0.1 ms. Any periodic communication with external equipment such as the embedded controller may be done with a lower time resolution of up to 200 ms.
Source of uncertainty	LV and MV measurement error, parametric deviations (manly within the transformer), timing deviations
Suspension criteria / Stopping criteria	All test patterns are successfully applied.

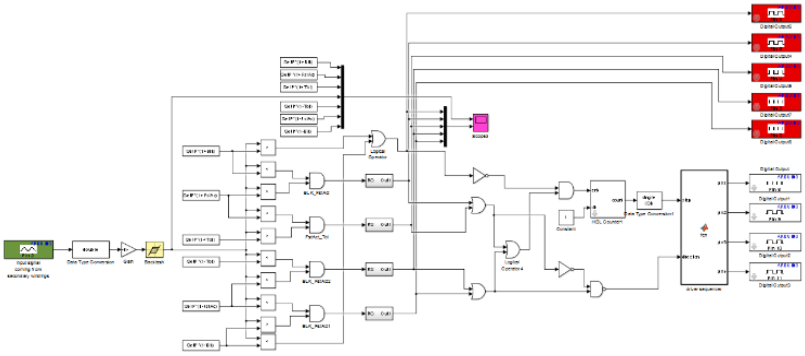
2.3 Mapping Strategy

2.3.1 Experiment Specification JRA2-TC2.TS1.1

Reference to Test Specification	JRA2-TC2.TS1
Title of Experiment	Software OLTC Controller
Experiment Realisation	In the initial experiment, the SuT is simulated by a monolithic model, which covers all components of the test setup. The monolithic model and the simulation results are used to test the functionality of the controller and to create a reference for further experiments. The initial model has been built in Simulink using blocks contained in the Physical Systems Simulation toolbox (branded Simscape). The tools were chosen in order to simulate the whole system and to be able to optimize the simulation via a phasor solver to be as accurate as possible.
Experiment Setup (concrete lab equipment)	The Simulink block diagram of the SuT is shown below.



The OLTC controller (red block) is tested in a monolithic simulation and is implemented as follows:



The following types are used to implement the interface variables which are described in the test setup section:

Name	Type	Unit	Description
MV	double, 3x1 array	[V]	Nodal voltages
LV	double, 3x1 array	[V]	Nodal voltages
LV_val	double	[V]	Voltage measurement
set-point	Uint	[V]	Voltage set-point
e	double	[V]	Voltage error
up	bool	[-]	Next transformer level (coil)
down	bool	[-]	Previous transformer level (coil)

Experimental Design and Justification

Induced MV-Variations: (at 20kV nominal voltage)

Start Time [s]	MV Set-Point [p.u.]
0	1
12	0.9
16	1

LV 3-Phase parallel RLC load:

Parameter	Value	Unit
Configuration	Y (Neural)	

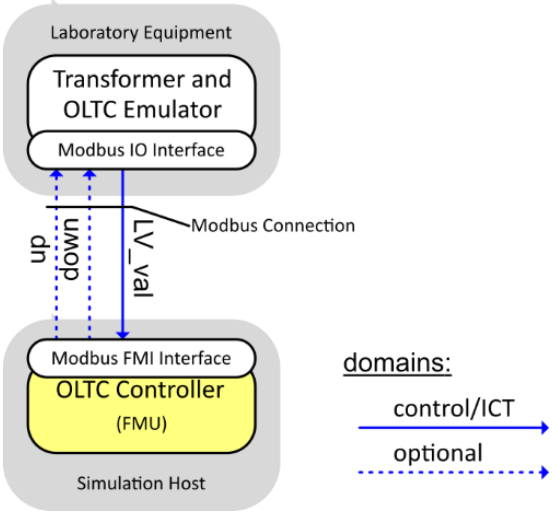
		Nominal Phase-to-phase voltage	420	[V]
		Unbalanced-Power	Off	
		Active Power	36	kW
		Inductive Reactive Power	0	[var]
		Capacitive Reactive Power	0	[var]
Precision of equipment	• relative solver tolerance = 1e-4.			
Uncertainty measurement	N/A			
Storage of data	For further evaluation, the simulation outcome will be stored in a CSV file on the simulation host.			

2.3.2 Experiment Specification JRA2-TC2.TS1.2

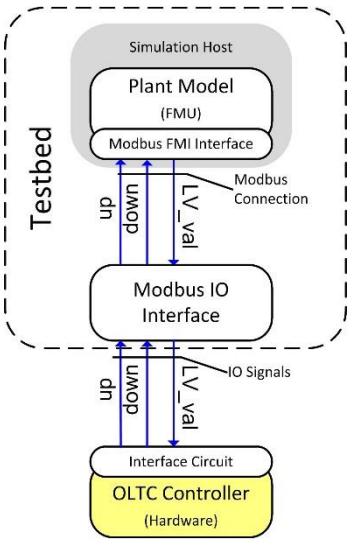
Reference to Test Specification	JRA2-TC2.TS1
Title of Experiment	Hardware OLTC Controller
Experiment Realisation	In the second experiment, the SuT is separated in two parts. The hardware part is composed by the controller of the medium voltage transformer built in an open-source electronics platform along with the transformer itself. The software part includes the simulation model built in Simulink Matlab. Once the first experiment is done correctly, we choose a new model based on a discrete solver (no continuous states) with fixed-step size=0.1 ms to facilitate its integration into the open-source electronics platform featuring an AT Mega 2560 microcontroller.
Experiment Setup (concrete lab equipment)	The Simulink block diagram of the SuT is identical to the block diagram of the first experiment. The OLTC controller is implemented in an Arduino card in order to test the communication between soft/hard enviroments. The implementation of the OLTC controller is also identical to the controller which is shown in experiment JRA2-TC2.TS1.1.
Experimental Design and Justification	The simulated MV value is adjusted in order to induce a voltage drop on the LV side. The applied MV pattern is determined during the experiment runs such that the LV values reside within all previously defined LV bands and such that all control actions of the OuI can be fully observed.
Precision of equipment	• fixed simulation and communication steps: 0.1 ms
Uncertainty measurement	Involved uncertainties are quantified through a direct comparison to the results off the reference simulation.
Storage of data	For further evaluation, recorded data points will be stored in a CSV file on the simulation host.

2.3.3 Experiment Specification JRA2-TC2.TS1.3

Reference to Test Specification	JRA2-TC2.TS1
Title of Experiment	OLTC Controller as FMU-ME
Experiment Realisation	This test concerns transferring the previously tested controller into an FMU for ME block. This block can be simulated with other system blocks or components in order to investigate and compare its behaviour to the case in experiment JRA2-TC2.TS1.1. The experiment covers a prototyping stage that integrates an emulated physical plant (i.e., the OLTC transformer and the measurement equipment represented by the analogue

	voltage measurement signals) with a simulated controller. Since the embedded controller on the Arduino platform is not capable of directly executing an FMU, an industrial communication protocol will be used to connect the simulation host, which executes the controller to the IO interfaces driving the plant emulation.
Experiment Setup (concrete lab equipment)	The grid supply, the OLTC including its electrical actuators, the transformer itself, the voltage sensors, and the electrical load will be emulated by the physical laboratory setup. The OLTC and the voltage readings can be accessed via industrial IO devices. As a communication protocol, Modbus RTU over EIT/TIA 485 or Modbus TCP/IP is used. In any case, the simulation host (x86-based Workstation) connected to the IO devices may actively poll all data points. Hence, the IO devices act as Modbus slaves. On the simulation host, the exported FMU and all interface components are executed such that end-to-end communication between the plant emulation and the simulated controller is achieved. The interface components periodically poll the voltage readings via Modbus and send the outputs of the controller to a logging facility. Logged data includes the control outputs and the inputs read from the plant emulator. Stored recordings allow to evaluate the controller FMU in detail and must also contain timing information up to the limits imposed by the communication infrastructure. The actual communication period depends on the capabilities of the equipment. A period of 100 ms to 200 ms is targeted. The following graphic illustrates the laboratory setup. The realization of the controller FMI is specified by the Simulink diagram in Experiment JRA2-TC2.TS1.1. The plant model in the previous experiment (the gird source, smart transformer, and load) is represented by the plant emulator in the current experiment. 
Experimental Design and Justification	For each experiment run, LV_val has to be dynamically adjusted within the permissible input range such that at least 50 control output transitions are triggered. Inputs may be manually adjusted and hence, the precise input voltage sequence may only be available after a single experiment run.
Precision of equipment	• relative solver tolerance: 1e-4 • event search precision: 1 ms • max. 200 ms Modbus polling cycle
Uncertainty measurement	• recording and evaluation of timing variations
Storage of data	For further evaluation, recorded data points will be stored in a CSV file on the simulation host.

2.3.4 Experiment Specification JRA2-TC2.TS1.4

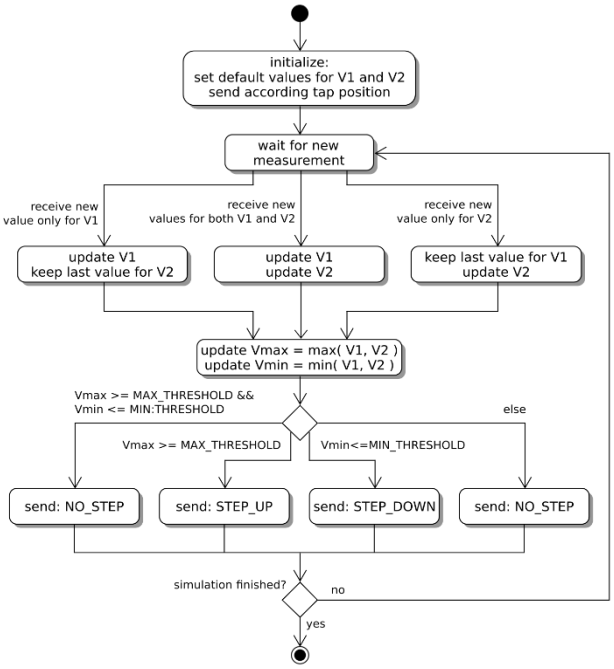
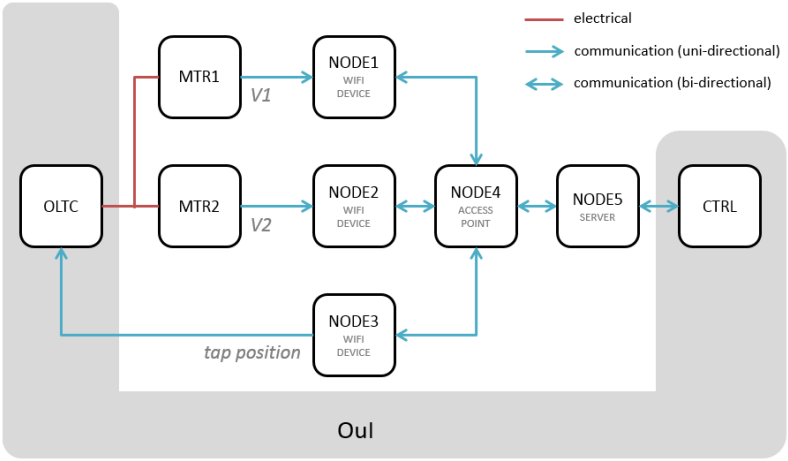
Reference to Test Specification	JRA2-TC2.TS1
Title of Experiment	FMI-based OLTC Controller Hardware in the Loop
Experiment Setup (concrete lab equipment)	The standalone control software is derived from the Simulink model and uploaded into the embedded controller board, which is also used in experiment JRA2-TC2.TS1.1. The LV_val IO signal of the controller is connected to the IO interface that drives the signal. Similarly, the digital output signals of the embedded controller are connected to the IO interface. The IO interface of the testbed is accessed via an industrial communication protocol. Modbus RTU over EIT/TIA 485 or Modbus TCP/IP is used between the IO device and the simulation host executing the plant model. The simulation host periodically polls the digital inputs and sets the analogue output via Modbus. The polling period depends on the capabilities of involved devices but a period of 100 ms to 200 ms is targeted. Interface components on the simulation host run the plant model encapsulated into an FMU and manage the communication between the IO interface and the FMU. The FMU itself contains an exported version of the Simulink plant model of experiment JRA2-TC2.TS1.1. The following figure illustrates the experimental setup. 
Experiment Realisation	In order to test the embedded OLTC controller including its IO interfaces, it will be coupled to a testbed mimicking the behaviour of the plant. The testbed may consist of industrial IO interfaces that drive the IO lines of the controller and a plant model that is interfaced via FMI for ME. Alternatively, the testbed may be directly added to the control software such that a Modbus testing interface is provided. The simulated low voltage value (LV_val) is transferred to the testbed that applies it to the controller. The signal is then processed by the physically available OLTC controller. Likewise, the control commands of the OLTC controller are sensed and transferred to the plant model. The software of the controller is still derived from the Simulink model, but in contrast to experiment JRA2-TC2.TS1.2, the controller is interfaced by its IO facilities.
Experimental Design and Justification	Induced MV variations: (at 20kV nominal voltage): **Start Time [s]** / **MV Set-Point [p.u.]** 0 / 1 5 / 0.9

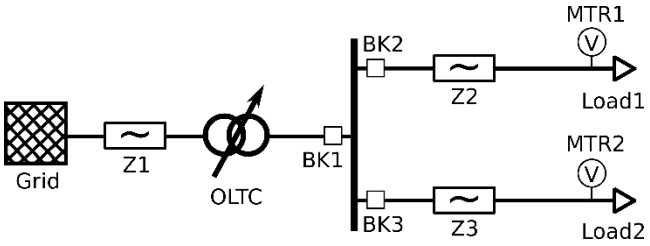
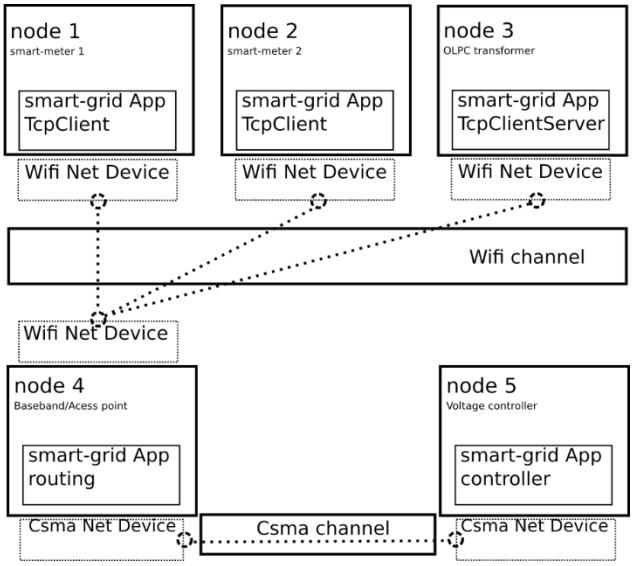
	<table><tr><td>15</td><td>1</td></tr><tr><td>25</td><td>0.8</td></tr><tr><td>35</td><td>1</td></tr><tr><td>45</td><td>0.5</td></tr><tr><td>50</td><td>0.8</td></tr><tr><td>60</td><td>1</td></tr></table> LV 3-phase parallel RLC load: <table><tr><th>Parameter</th><th>Value</th><th>Unit</th></tr><tr><td>Configuration</td><td>Y (Neural)</td><td></td></tr><tr><td>Nominal Phase-to-phase voltage</td><td>420</td><td>[V]</td></tr><tr><td>Unbalanced-Power</td><td>Off</td><td></td></tr><tr><td>Active Power</td><td>36</td><td>kW</td></tr><tr><td>Inductive Reactive Power</td><td>0</td><td>[var]</td></tr><tr><td>Capacitive Reactive Power</td><td>0</td><td>[var]</td></tr></table>
Precision of equipment	• relative solver tolerance: 1e-4 • event search precision: 1 ms • max. 200 ms Modbus polling cycle
Uncertainty measurement	• recording and evaluation of timing variations
Storage of data	For further evaluation, recorded data points will be stored in a CSV file on the simulation host.

3 Test Case Specification for TC3

3.1 Test Case

Name of the Test Case	JRA2-TC3
Narrative	This test case deals with the impact of ICT-related aspects in a simple low voltage distribution grid, where two meters send information about local voltage levels via a communication network to a remote controller. Based on these meter readings, the controller actuates the tap position of an OLTC transformer. ICT-related aspects of interest are technical features (communication delays, controller dead times) and consequences of cyber-security attacks (scaling attacks, ramping at-tacks, random scaling factor attacks, digital signal tap attacks). The aim of this test case is to demonstrate and assess the effect of communication networks on the actuation pattern of the controller and the resulting physical effects in the low voltage distribution system. Since this test case aims at providing an illustrative example of what problems may arise from poor controller designs, a fundamentally flawed approach for handling delays is implemented for the controller. Similarly, it is assumed that cyber-security measures are insufficient, opening the possibility to implement cyber-attacks. Moreover, this test case aims to demonstrate the importance of realistic simulation approaches for assessing distributed and centralized Smart Grid control algorithms as well as benchmarking communication network technologies and topologies for use in Smart Grid applications.

Function(s) under Investigation	The focus of this investigation is the actuation pattern of a voltage controller in the presence of communication delays, controller dead times and cyber-attacks. This controller calculates setpoints for the tap positions of an OLTC transformer based on the readings of two voltage meters. 
Object under Investigation	• voltage controller • OLTC transformer 
Domain under Investigation	• electrical (voltage levels) • ICT (data transmission, cyber-attacks) • control (calculation of setpoints, OLTC actuation)
Purpose of Investigation	Characterize the response of the voltage controller in the presence of communication delays, controller dead times and cyber-attacks.
System under Test	Controller: • simple rule-based control algorithm, calculating tap position setpoints for the OLTC transformer depending on the meter readings • runs on a dedicated server, separate from transformer and meters • when receiving a new measurement and computing a new tap position setpoint, the controller becomes unresponsive for a short time period (dead time), i.e., further measurements arriving during this time

	are not processed Low voltage distribution system: • OLTC MV/LV transformer • changing the OLTC's tap position is assumed to take 3s in total, during which the OLTC is not responsive to new setpoints • 2 loads with voltage meters (measurement devices and/or smart meters) that send their measurements at regular intervals to the controller  Communication network: • base station/access point for wireless communication • 1 node (sender) for each voltage meter, wireless connection to the base station • 1 node (receiver) for the transformer, wireless connection to the base station • 1 node (sender/receiver) for the server (controller), wired internet connection to the base station 
Functions under Test	• setpoint calculation from voltage controller • setpoint actuation at OLTC • data transmission of meter readings and controller setpoints
Test criteria	Even in the presence of communication delays, controller dead times and cyber-attacks, the actuation of the OLTC transformer should result in acceptable operational conditions (voltage levels according to grid codes). More specifically, the tap position should coincide with the "idealized" base case, where no communication delays, controller dead times or cyber-attacks are present.
target metrics (test factors)	• tap position • voltage levels
variability attributes	• T_{sender}: time between sending two measurements

		• t_{sender}: time offset between voltage measurements • t_{ctrl}: controller dead time • random number generator seed for ICT network simulator
	quality attributes (thresholds)	Acceptable operational conditions for the voltage levels are between 0,95 p.u. and 1,05 p.u.

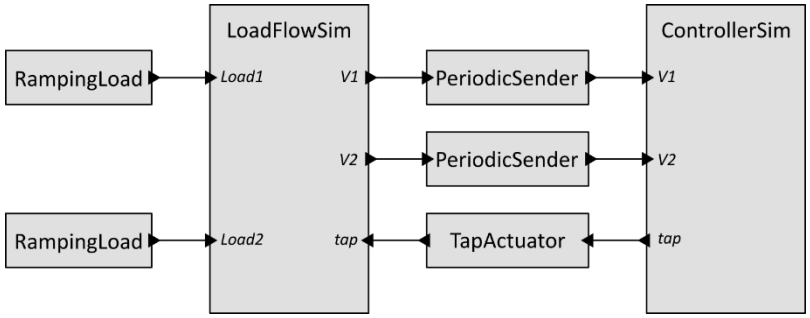
3.2 Qualification Strategy

3.2.1 Test Specification JRA2-TC3.TS1

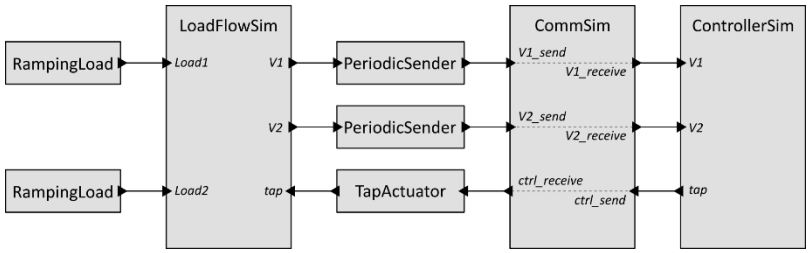
Reference to Test Case	JRA2-TC3
Title of Test	validation of network communication models
Test Rationale	This is a standalone experiment including only the communication network simulator, in order to test and validate the ns-3 models developed for the test case.
Specific Test System (graphical)	The test system comprises the communication network as described above.
Target measures	The simulated transmission of data between the nodes has to happen according to the defined protocols (Wi-Fi, Ethernet)
Input and output parameters	Measured parameters: • timing information about data packet transmission • end-to-end delays of data transmission between nodes
Test Design	• The meters send every 15 minutes a packet of fixed size (100 bytes) containing a voltage measurement to the access point (Wi-Fi protocol). Subsequently, the data is sent to the server (Ethernet protocol), where the CVC algorithm is implemented. • In the next minute after the packets are received, the controller sends a tap position setpoint to the OLTC transformer, which is also connected to the access point (Wi-Fi).
Initial system state	The meters start sending at t = 0 min, no other data traffic otherwise.
Evolution of system state and test signals	N/A
Other parameters	N/A
Temporal resolution	internal time resolution of communication network simulator
Source of uncertainty	communication delays
Suspension criteria / Stopping criteria	N/A

3.2.2 Test Specification JRA2-TC3.TS2_baseline

Reference to Test Case	JRA2-TC3
Title of Test	Baseline simulation without communication delays, controller dead times or cyber-attacks
Test Rationale	The outcome of this test is the reference for test specification JRA2-TC3.TS2. By neglecting ICT-related effects, this represents the “idealized” case.

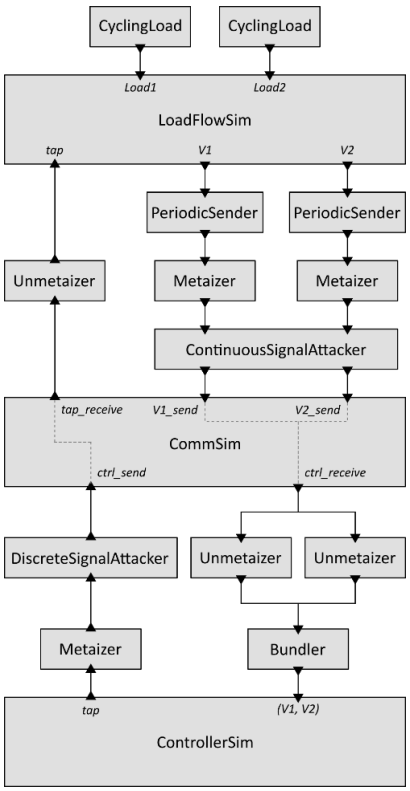
Specific Test System (graphical)	Overview of individual simulation components: 
Target measures	This test serves as baseline for reference for test specification JRA2-TC3.TS2. As such, there is no qualification strategy for the output of this test itself.
Input and output parameters	Controllable input parameters: • tap position Measured parameters: • voltages at loads Uncontrollable parameters: • power consumption of loads • T_{sender} = 1 min • t_{sender} = 0 s • t_{ctrl} = 0 s
Test Design	• The test takes 2 minutes of simulation time, during which both loads are linearly ramped up. • The meters send their measurements to the controller in regular intervals (T_{sender}=1 min) in perfect synchronization (t_{sender}=0 s), beginning at the start of the simulation (t=0 min). • Whenever the controller receives new measurements, a new value for the tap position is calculated and sent to the OLTC transformer. • The transmission of data from the meters to the controller (voltage measurements) and from the controller to the OLTC's tap actuator (tap position setpoint) happens without delays. • Voltage *V1* (voltage measured at *Load1*) is expected to stay within the operational limits throughout the test. Voltage *V2* (voltage measured at *Load2*) falls beyond the lower threshold within 1 minute, and a change in the tap position (from 0 to -1) is expected to happen the next time the meters transmit their measurements to the controller (t=1 min).
Initial system state	• initial tap position (at t=0 min): 0
Evolution of system state and test signals	• Load1: active power consumptions ramps linearly from 0 to 2 kW within 2 minutes • Load2: active power consumptions ramps linearly from 7 to 10 kW within 2 minutes • For the sake of simplicity, the effect of changing a tap should become effective at the end of the OLTC's actuation deadtime (instantaneous event, no continuous process).
Other parameters	N/A
Temporal resolution	1 second
Source of uncertainty	N/A
Suspension criteria / Stopping criteria	N/A

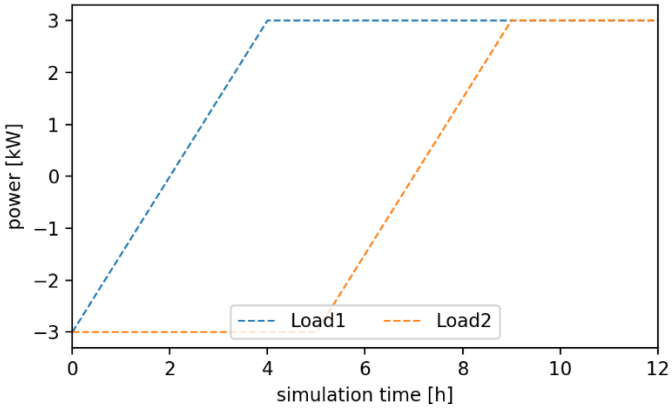
3.2.3 Test Specification JRA2-TC3.TS2

Reference to Test Case	JRA2-TC3
Title of Test	Assessment of impact of communication delays and controller dead times
Test Rationale	This test assesses the impact of communication delays and controller dead times on the actuation pattern of the OLTC and the voltage levels. The impact is evaluated by comparing the final realized tap position with the expected tap position (from the base line simulation JRA2-TC3.TS2_baseline). Furthermore, the voltage levels at the end of the simulation are expected to be within the operational limits.
Specific Test System (graphical)	Overview of individual simulation components:  Attention: The controller calculates and transmits tap position every time a new measurement arrives (using the latest values available).
Target measures	• expected final tap position (at t=2 min): -1 • voltage levels are expected to be within operational limits
Input and output parameters	Controllable input parameters: • tap position Measured parameters: • voltages at loads Uncontrollable parameters: • power consumption of loads • T_{sender} = 1 min • $\Delta t_{sender} \in$ {-14 ms, -12 ms, …, 12 ms, 14 ms} • $\Delta t_{ctrl} \in$ {2 ms, 10 ms, 20 ms}
Test Design	• The test takes 2 minutes of simulation time, during which both loads are linearly ramped up. • The meters send their measurements to the controller in regular intervals (T_{sender} = 1 min) with a small relative delay to each other (Δt_{sender}), beginning at the start of the simulation (t = 0 min). • Whenever the controller receives new measurements, a new value for the tap position is calculated and sent to the OLTC transformer. • The transmission of data from the meters to the controller (voltage measurements) and from the controller to the OLTC's tap actuator (tap position setpoint) happens with a delay (calculated by the communication network simulator). • After receiving a new voltage measurement, the controller enters its dead time (Δt_{ctrl}) and becomes unresponsive. • After receiving a new tap position setpoint, the tap actuator enters its dead time and becomes unresponsive. • Voltage *V1* (voltage measured at *Load1*) is expected to stay within the operational limits throughout the test. Voltage *V2* (voltage measured at *Load2*) falls beyond the lower threshold within 1 minute, and a change in the tap position (from 0 to -1) is expected to happen the

	next time the meters transmit their measurements to the controller (t = 1 min).
Initial system state	• initial tap position (at t = 0 min): 0
Evolution of system state and test signals	• Load1: active power consumptions ramps linearly from 0 to 2 kW within 2 minutes • Load2: active power consumptions ramps linearly from 7 to 10 kW within 2 minutes • For the sake of simplicity, the effect of changing a tap should become effective at the end of the OLTC's actuation deadtime (instantaneous event, no continuous process).
Other parameters	N/A
Temporal resolution	2 milliseconds
Source of uncertainty	communication delays
Suspension criteria / Stopping criteria	N/A

3.2.4 Test Specification JRA2-TC3.TS3_baseline

Reference to Test Case	JRA2-TC3
Title of Test	Baseline simulation without cyber-attacks
Test Rationale	The outcome of this test is the reference for test specification JRA2-TC3.TS3. By neglecting ICT-related effects this represents the "idealized" case.
Specific Test System (graphical)	Overview of individual simulation components: *Attention*: In this test, the controller periodically calculates and transmits tap position setpoints, using that latest values available. This means, that is does not transmit a new tap position setpoints every time a new measurement arrives (as is happening in JRA2-TC3.TS2). 

Target measures	This test serves as baseline for reference for test specifications JRA2-TC3.TS3_scaling, JRA2-TC3.TS3_ramping, JRA2-TC3.TS3_random and JRA2-TC3.TS3_tap_position. As such, there is no qualification strategy for the output of this test itself.
Input and output parameters	Controllable input parameters: • tap position Measured parameters: • voltages at loads Uncontrollable parameters: • power consumption of loads • T_{sender} = 1 min • T_{ctrl} = 15 min • Δt_{sender} = 3 s • Δt_{ctrl} = 0 s Attacker module parameters: • DisreteSignalAttacker=OFF • ContinuousSignalAttacker=OFF
Test Design	• The test takes 12 hours of simulation time, during which both loads are ramped up (see below). • The meters send their measurements to the controller in regular intervals (T_{sender} = 1 min) with a small relative delay to each other (Δt_{sender} = 3 s), beginning at the start of the simulation (t = 0 min). • The controller periodically calculates and transmits tap position setpoints (T_{ctrl} = 15 min), using that latest values available, beginning at the start of the simulation (t = 0 min). • The transmission of data from the meters to the controller (voltage measurements) and from the controller to the OLTC's tap actuator (tap position setpoint) happens over the communication network simulator ("CommSim" component).
Initial system state	• initial tap position (at t = 0 min): 0
Evolution of system state and test signals	The active power consumptions of Load1 and Load2 ramp according to the following chart: 
Other parameters	N/A
Temporal resolution	1 second
Source of uncertainty	communication delays
Suspension criteria / Stopping criteria	N/A

3.2.5 Test Specification JRA2-TC3.TS3_scaling

Reference to Test Case	JRA2-TC3
Title of Test	Assessment of scaling attacks
Test Rationale	This test characterizes the impact of a scaling attack (scaling the voltage measurements) on the OLTC's actuation pattern and the voltage levels.
Specific Test System	See test specification JRA2-TC3.TS3_baseline
Target measures	• tap actuation according to baseline (JRA2-TC3.TS3_baseline) • voltage levels are expected to be within operational limits
Input and output parameters	Attacker module parameters: • DisreteSignalAttacker=OFF • ContinuousSignalAttacker=ON • $\square_s$ = 0.01 Remaining parameters according to test specification JRA2-TC3.TS3_baseline.
Test Design	Basic design like in test specification JRA2-TC3.TS3_baseline. In addition, the scaling attack pattern is introduced. This means, both voltage measurements (*V1* and *V2*) are modified by the ContinuousSignalAttacker component, representing an influence of a cyber-attacker in the system and scaling them by the factor $\square_s$. Scaling rule for the voltage measurements is y(t) $\square$ (1 + $\square_s$).
Initial system state	• initial tap position (at t=0 min): 0 • attacker activation time at t=0 min
Evolution of system state and test signals	See test specification JRA2-TC3.TS3_baseline
Other parameters	N/A
Temporal resolution	See test specification JRA2-TC3.TS3_baseline
Source of uncertainty	See test specification JRA2-TC3.TS3_baseline
Suspension criteria / Stopping criteria	N/A

3.2.6 Test Specification JRA2-TC3.TS3_ramping

Reference to Test Case	JRA2-TC3
Title of Test	Assessment of ramping attacks
Test Rationale	This test characterizes the impact of a ramping attack (ramping the voltage measurements) on the OLTC's actuation pattern and the voltage levels.
Specific Test System	See test specification JRA2-TC3.TS3_baseline
Target measures	• tap actuation according to baseline (JRA2-TC3.TS3_baseline) • voltage levels are expected to be within operational limits
Input and output parameters	Attacker module parameters: • DisreteSignalAttacker=OFF • ContinuousSignalAttacker=ON • $\square_r$ = 2.4e-4

	Remaining parameters according to test specification JRA2-TC3.TS3_baseline.
Test Design	Basic design like in test specification JRA2-TC3.TS3_baseline. In addition, the ramping attack pattern is introduced. This means, both voltage measurements (*V1* and *V2*) are modified by the ContinuousSignalAttacker component, representing an influence of a cyber-attacker in the system and ramping them by the factor □ᵣ □ t, where t is the simulation time. The ramped signal attack pattern is y(t) + □ᵣ □ t.
Initial system state	• initial tap position (at t=0 min): 0 • attacker activation time at t=0 min
Evolution of system state and test signals	See test specification JRA2-TC3.TS3_baseline
Other parameters	N/A
Temporal resolution	See test specification JRA2-TC3.TS3_baseline
Source of uncertainty	See test specification JRA2-TC3.TS3_baseline
Suspension criteria / Stopping criteria	N/A

3.2.7 Test Specification JRA2-TC3.TS3_random

Reference to Test Case	JRA2-TC3
Title of Test	Assessment of the random attack pattern
Test Rationale	This test characterizes the impact of a random attack (adding random noise to the voltage measurements) on the OLTC's actuation pattern and the voltage levels.
Specific Test System	See test specification JRA2-TC3.TS3_baseline
Target measures	• tap actuation according to baseline (JRA2-TC3.TS3_baseline) • voltage levels are expected to be within operational limits
Input and output parameters	Attacker module parameters: • DisreteSignalAttacker=OFF • ContinuousSignalAttacker=ON Remaining parameters according to test specification JRA2-TC3.TS3_baseline.
Test Design	Basic design like in test specification JRA2-TC3.TS3_baseline. In addition, the random attack pattern is introduced. This means, both voltage measurements (*V1* and *V2*) are modified by the ContinuousSignalAttacker component, representing an influence of a cyber-attacker in the system with the modification pattern y(t) + rand(a, b) , where t is the simulation time and a and b are constants.
Initial system state	• initial tap position (at t=0 min): 0 • attacker activation time at t=0 min
Evolution of system state and test signals	See test specification JRA2-TC3.TS3_baseline
Other parameters	N/A
Temporal resolution	See test specification JRA2-TC3.TS3_baseline
Source of uncertainty	• random attack pattern • communication delays

Suspension criteria / Stopping criteria	N/A

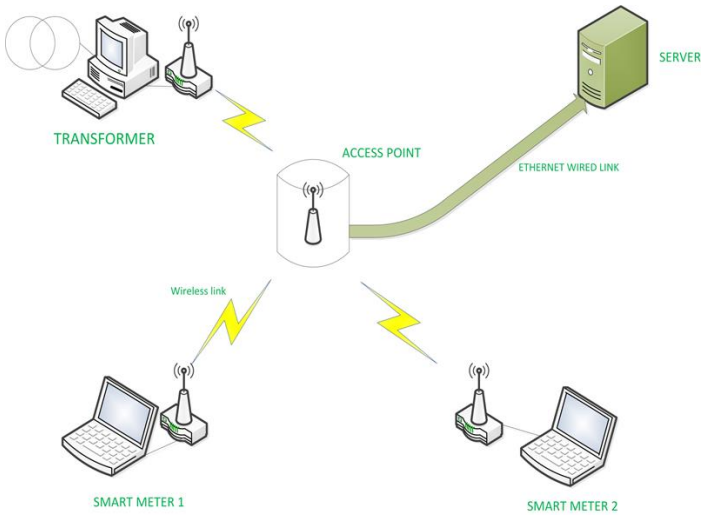
3.2.8 Test Specification JRA2-TC3.TS3_tap_position

Reference to Test Case	JRA2-TC3
Title of Test	Assessment of an attack on the tap setpoint commands
Test Rationale	This test characterizes the impact of a direct attack on the OLTC's actuation pattern, assessing the impact on the voltage levels.
Specific Test System	See test specification JRA2-TC3.TS3_baseline
Target measures	• tap actuation according to baseline (JRA2-TC3.TS3_baseline) • voltage levels are expected to be within operational limits
Input and output parameters	Attacker module parameters: • DisreteSignalAttacker=ON • ContinuousSignalAttacker=OFF Remaining parameters according to test specification JRA2-TC3.TS3_baseline.
Test Design	Basic design like in test specification JRA2-TC3.TS3_baseline, but with a total simulation time of only 5 hours. In addition, an attack pattern is introduced where the voltage measurements remain unmodified, but rather the OLTC tap position setpoints sent from the controller are intercepted and modified directly. This means that the voltage measurements sent to the voltage controller have the correct values and the controller will always calculate the correct setpoints based on the correct input. However, the attacker is assumed to be able to intercept the OLTC setpoint commands and modify them by decreasing their current value by 1. As a result, the voltages rise until the systems becomes unstable.
Initial system state	See test specification JRA2-TC3.TS3_baseline
Evolution of system state and test signals	See test specification JRA2-TC3.TS3_baseline
Other parameters	N/A
Temporal resolution	See test specification JRA2-TC3.TS3_baseline
Source of uncertainty	See test specification JRA2-TC3.TS3_baseline
Suspension criteria / Stopping criteria	N/A

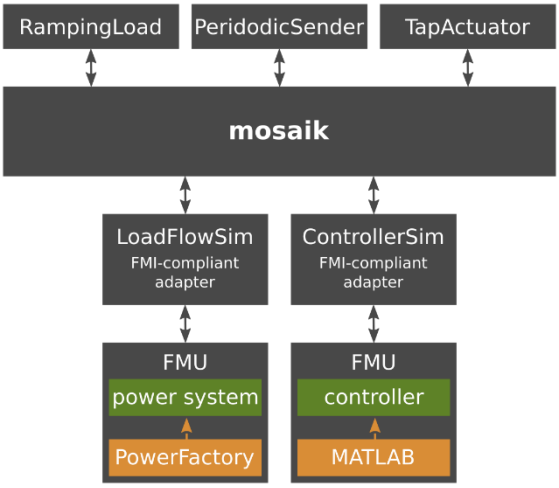
3.3 Mapping Strategy

3.3.1 Experiment Specification JRA2-TC3.TS1.ns-3

Reference to Test Specification	JRA2-TC3.TS1
Title of Experiment	Validation of network communication models in ns-3
Experiment Realisation	The experiment is implemented in the ns-3 communication network simulator.

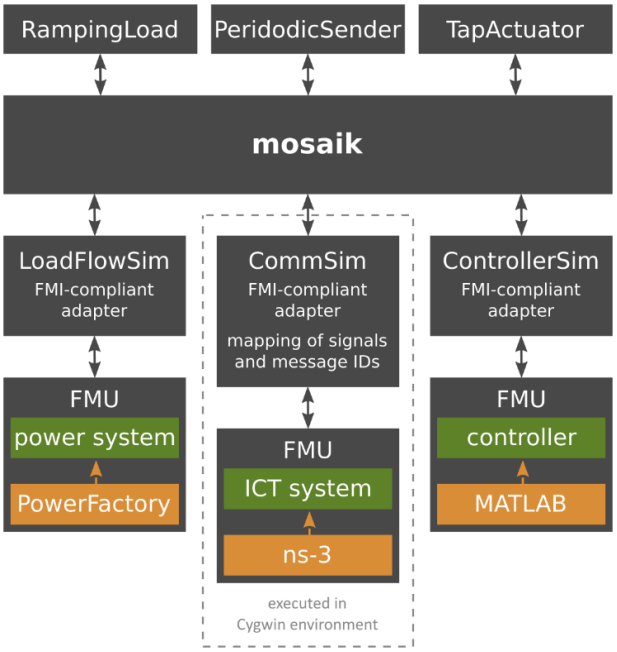
	
Experiment Setup	The ns-3 communication network simulator provides all models for simulating the data transfer via Wi-Fi and Ethernet. In addition, the following dedicated application layer models are used for simulating the nodes: • *Model Tc3ControllerServer*: This application layer model simulates the server functionality of a CVC controller device. The role of this model is the same as the role of a server in every network, i.e., it creates a socket where the smart meters connect and sends data. In addition, after a packet is received, the headers are checked, and the end-to-end delay of the transmission is calculated and stored. Later in the simulation, this delay is used to calculate the corresponding timestamp and add an event to the event queue. • *Model SmartmeterCustomClient*: This application model simulates a smart meter device. The model's purpose is to establish connection to the CVC's server socket and send a packet of fixed size (100 bytes). For the calculation of the end-to-end delay, the time of the packet creation is added to it as part of a header. • *Model Tc3ControllerClient*: This application model simulates the CVC controller's client aspect and helps to establish the connection between the controller and the OLTC transformer. More specifically, it implements a UDP client-like functionality, managing the creation and sending of packets (containing data associated with new setpoints) to the transformer. For the calculation of the end-to-end delay, the time of the packet creation is added to it as part of a header. • *Model OltcCustomServer*: This application model simulates the transformer server aspect and helps to establish the connection between the controller and OLTC controller. More specifically, it implements a UDP server-like functionality, receiving the packets (containing data associated with new setpoints) sent by the controller. Here the header, containing the time the packet was sent, by the controller is retrieved and the end-to-end delay is calculated.
Experimental Design and Justification	This is a basic ns-3 simulation using the dedicated application layer models implemented for this test case.
Precision of equipment	N/A
Uncertainty measurement	N/A
Storage of data	Information regarding data packet transfer is visualized and stored (graphically) via the pyViz tool. End-to-end delays are stored in CSV files for further evaluation.

3.3.2 Experiment Specification JRA2-TC3.TS2_baseline.mosaik

Reference to Test Specification	JRA2-TC3.TS2_baseline
Title of Experiment	Implementation of base line simulation in mosaik
Experiment Setup (concrete lab equipment)	Dedicated simulation components are implemented as FMUs for Co-Simulation: • Power system simulation: the power system is implemented as PowerFactory model, using consecutive power flow calculations to simulate the power system • Controller: the algorithm for calculating the tap position setpoint is implemented as a (simple) MATLAB script The other simulation components and the FMI-compliant adapters are implemented in Python on top of mosaik's high level API. The use of PowerFactory requires this simulation to use Windows as operating system.
Experiment Realisation	The experiment is implemented as co-simulation using mosaik with a constant simulation step size of 1 second. 
Experimental Design and Justification	This is a basic co-simulation setup using the mosaik environment with FMUs.
Precision of equipment	N/A
Uncertainty measurement	N/A
Storage of data	The output from the individual simulation components is stored as time series data (HDF5 data format).

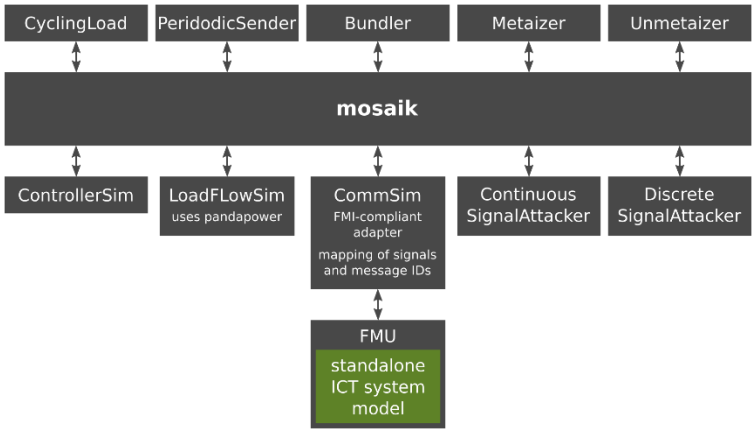
3.3.3 Experiment Specification JRA2-TC3.TS2.mosaik

Reference to Test Specification	JRA2-TC3.TS2
Title of Experiment	Characterization of effect of communication delays and controller dead times using mosaik

Experiment Setup (concrete lab equipment)	Dedicated simulation components are implemented as FMUs for Co-Simulation: • Power system simulation: the power system is implemented as PowerFactory model, using consecutive power flow calculations to simulate the power system • Controller: the algorithm for calculating the tap position setpoint is implemented as a (simple) MATLAB script • Communication network simulation: the communication network delays are simulated with the help of ns-3 The other simulation components and the FMI-compliant adapters are implemented in Python on top of mosaik's high level API. The use of PowerFactory requires this simulation to use Windows as operating system. However, since ns-3 is developed for Linux operating systems, it is run in a Cygwin environment.
Experiment Realisation	The experiment is implemented as co-simulation using mosaik with a constant simulation step size of 2 milliseconds. 
Experimental Design and Justification	This is an advanced co-simulation setup using FMUs and communication delays. In order to incorporate the "randomness" of the communication delays, an ensemble of simulation runs with different random number generator seeds has to be evaluated for every considered combination of Δt_{sender} and Δt_{ctrl} (Monte Carlo approach). The communication network model uses message IDs as inputs and outputs, with a message ID equal to 0 indicating that no signal is present. Inside the ns-3 model, these message IDs are associated to dummy messages (of configurable size), which are used to simulate the processing of the message within the communication network. However, the power system model and the voltage controller expect real-valued numbers as inputs and outputs and the corresponding tools (i.e., PowerFactory and MATLAB). Therefore, the mosaik wrapper for the ns-3 FMU implements a mapping between message IDs and signal values. Furthermore, all FMU wrappers and mosaik simulators are implemented such that they understand an input of type *None* as absent signal and react accordingly (e.g., remain idle in case the signal is absent).
Precision of equipment	N/A

Uncertainty measurement	Since this is a computer simulation, there is no real source of uncertainty or randomness. The communication network simulator uses an integer-valued seed for its pseudo random number generator.
Storage of data	The output from the individual simulation components is stored as time series data (HDF5 data format).

3.3.4 Experiment Specification JRA2-TC3.TS3.mosaik

Reference to Test Specification	JRA2-TC3.TS3_baseline, JRA2-TC3.TS3_scaling, JRA2-TC3.TS3_ramping, JRA2-TC3.TS3_random, JRA2-TC3.TS3_tap_position
Title of Experiment	Cyber-attack assessment
Experiment Realisation	The experiment is implemented as co-simulation using mosaik with a constant simulation step size of 1 second. 
Experiment Setup (concrete lab equipment)	The communication network delays are simulated with the help of a simple standalone ICT system model, which calculates delays by drawing from a random distribution. This standalone model is provided as an FMU for CS. Cyber-attacks are simulated via the ContinuousSignalAttacker and DiscreteSignalAttacker components, which can be turned on/off and parameterized to yield the desired attack pattern (scaling, ramping, etc.). All simulation components, including the FMI-compliant adapter, are implemented in Python on top of mosaik's high level API.
Experimental Design and Justification	This is a co-simulation setup that can be used for part of the risk assessment of cyber-attacks, as suggested by the SPARKS methodology. It assists experts in performing such risk assessments, as the results of the simulations enable better risk perception and decisions during the risk treatment phase. The communication network model uses message IDs as inputs and outputs, see experiment specification JRA2-TC3.TS2.mosaik.
Precision of equipment	N/A
Uncertainty measurement	Since this is a computer simulation, there is no real source of uncertainty or randomness. The communication network simulator and the random attack pattern use an integer-valued seed for their pseudo random number generator.
Storage of data	The output from the individual simulation components is stored as time series data (HDF5 data format).