CIE- Microprocessor_Unit-5

atul.22010970@viit.ac.in Switch account

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CIE -5 QUESTIONS

Linear address is .... *

○ obtained after physical address in paging

○ converted to logical address in segmentation

● obtained after converting logical address in segmentation

○ the address where the data is located physically in memory

CR2 contains....... *

○ Page directory base register

● page fault linear address

○ page table address

○ none of the above

TLB HIT will reduce the access to *

- ☑ Page directory
- ☑ Page table
- ☐ Control register
- ☐ none of the above

Which of the following is not true about segments? *

- ☑ All segments have variable size
- ☐ All segments have a descriptor
- ☐ All segments are areas of memory
- ☑ none of the above

Which of the following is true *

- ☐ 80386 can switch into real mode at any point of time
- ☐ 80386 can switch into virtual mode only from protected mode
- ☐ real mode is 80386 natural 32-bit environment
- ☐ all of the above

The capabilities of paging mechanism are *

- ☐ page translation & protection
- ☐ Address translation and page protection
- ☐ segment translation
- ☐ all of the above

The segment descriptors are to be kept in one group and placed one after the other in contiguous locations. This arrangement is called *

○ segment table

◉ descriptor table

○ Interrupt descriptor table

.... is true about LDT *

☑ It is located in GDT

☑ It is used in multi user system

☑ It is optional

☐ LDTs are assigned in IDT

If the 2nd bit in selector (selector bit starting from 0) is set, then it indicates *

○ Page table

◉ LDT

○ descriptor privilege

○ none of the above

When loading segment selectors, 80386 checks if.. *

○ The selector index is within the page table limit

◉ It references the correct descriptor

○ The page table has correct privileges

○ none of the above

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