Optics Letters

High-performance sub-wavelength grating-based resonator sensors with substrate overetch

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Received 14 October 2019; revised 4 November 2019; accepted 7 November 2019; posted 8 November 2019 (Doc. ID 380097); published 6 December 2019

We propose a strategy to improve sensing performance of sub-wavelength-grating (SWG) waveguide-based sensors by introducing a substrate-overetch (SOE) geometry. The proposed SOE-SWG waveguide shows enhanced analyte interaction and a reduced group index, which improves the sensitivity of resonator-based sensors. The SiO₂ overetch process was realized in Ar/C₄F₈/O₂ plasma for 40 sec with a SiO₂/Si selectivity of 10:1, obtaining a 285-nm anisotropic overetch in the SiO₂ layer. Sensor performance of the SOE-SWG architecture is characterized by using isopropyl alcohol solutions, indicating an enhanced bulk sensitivity up to 575 nm/RIU (479 nm/RIU before the SOE), and a maximum waveguide mode sensitivity larger than one. © 2019 Optical Society of America

https://doi.org/10.1364/OL.44.005981

Leveraging the compatibility of complementary metal-oxidesemiconductor (CMOS) manufacturing facilities, silicon photonics is regarded as an emerging and economical approach to address the demand for high-throughput data communications. Beyond data communications, a vast number of applications have been explored for complex silicon photonics systems, including nano-optomechanics and condensed matter physics, nonlinear optics, biosensing, novel light sources, signal processing, integrated optoelectronics, etc [1]. Among them, biosensing is one of the most promising applications. Due to the small footprint, silicon photonics devices enable the development of miniaturized compact sensing devices for multiplexed diagnostics [2]. Moreover, silicon photonics is an excellent substrate for label-free detection: the wavelength (or phase) shift or intensity change is linearly proportional to the mass change due to the adsorption at the surface, offering continuous and quantitative detection in real time.

Sub-wavelength gratings (SWGs) have been considered to be an appealing metamaterial for the development of next-generation photonic integrated circuits (PICs) [3]. Compared to the conventional silicon-on-insulator (SOI) waveguide that has only two parameters (thickness and width), SWG metamaterials provide more parameters to control optical properties, such as the period (Λ), duty cycle (η), waveguide width (W), and waveguide thickness (t). SWG-based SOI sensors have been

investigated to improve sensing performance, showing a bulk sensitivity (S_{bulk}) as high as 490 nm/RIU and an enhanced surface sensing capability [4–6]. Recently Wangüemert-Pérez et al. proved that a narrower and thicker SWG pillar could improve the waveguide mode sensitivity (S_{wg}) [7]. By applying SWG of W=350 nm and t=300 nm, S_{wg} shows an improved performance over 0.9 RIU/RIU. However, n_{eff} is not a directly measurable value and requires sensing architectures to convert it into a detectable quantity. For a resonator-based sensor, the sensitivity (S_{res}) consists of the architecture sensitivity (S_{arch}) and waveguide mode sensitivity, i.e., $S_{\text{res}} = S_{\text{arch}} \times S_{\text{wg}}$, which are defined as [7]

$$S_{\rm arch} = \frac{\lambda_{\rm res}}{n_{\rm g}},$$
 (1)

$$S_{\rm wg} = \partial n_{\rm eff} / \partial \Gamma,$$
 (2)

respectively, where λ_{res} is the resonant wavelength, n_g is the group index, ∂n_{eff} is the change of the effective index, and $\partial \Gamma$ is the variation of any physical parameter around the waveguide [the refractive index (RI) change or the adlayer thickness change]. Therefore, not only a large S_{wg} but a small n_g is necessary to improve the sensitivity for the resonator-based sensor. Chang et al. developed a pedestal SWG-based resonator sensor, where periodic pillars are semi-suspended onto the SiO₂ substrate by isotropic etching processes [8]. The proposed SWG geometry gives a lower n_g and higher index profile symmetry of the waveguide, thus a larger bulk sensitivity, roughly 545 nm/RIU. However, due to the isotropic etching, the robustness of the sensor is unguaranteed, and the etching depth (\sim 50 nm) is limited by the width of the SWG pillar, which hinders the potential for further improving sensor performance. Moreover, although the quality factor of the proposed SWG resonator is not presented in Ref. [8], isotropic etching does make the transmission performance of the resonator worse.

In this Letter, we introduce a new approach to improve the sensitivity of SWG-based sensors. Instead of etching the substrate isotropically, we used the anisotropic etching process with ${\rm Ar/C_4F_8/O_2}$ as the etchant, which gives vertical SiO₂ etching down to the buried oxide (BOX) layer and results in the substrate-overetch SWG (SOE-SWG) pillar, as shown in Fig. 1.

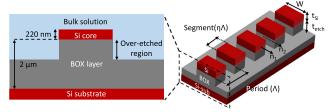


Fig. 1. Schematic of the SWG-based waveguide geometry with the substrate overetch (Λ is the SWG period, W is the waveguide width, t_{Si} and t_{etch} are the thickness of silicon pillars and BOX pedestals, and n_1 and n_2 represent high and low refractive indices in the SWG waveguide, respectively).

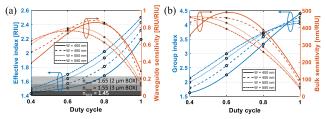


Fig. 2. (a) Simulated effective index (left) and waveguide mode sensitivity (right) versus the duty cycle of SWG waveguides with different widths. Three different grayscale regions represent the RI of the BOX layer (dark gray), and the minimum *n*_{eff} of SWG waveguides for 3-μm (gray) and 2-μm (light gray) thick BOX layers to minimize the substrate leakage [9]. (b) Simulated group index (left) and bulk sensitivity (right) versus the duty cycle of the SWG waveguides with different widths.

Anisotropic etching is no longer limited by the SWG geometry and provides more stable support.

Simulations for SWG-based configurations were realized based on Bloch boundary conditions using a fully vectorial three-dimensional finite-difference time-domain (3D-FDTD) approach for band structure calculations of periodic structures. To maintain a subwavelength-guided wave propagating in the proposed waveguide, we fixed the SWG period of 250 nm to allow all investigated SWG-based geometries to be in the sub-wavelength regime ($\Lambda \ll \lambda/(2n_{\rm eff})$) [3]. Figure 2 shows the simulation results of SWG-based waveguides with a varied duty cycle ($\eta = 0.4 - 1$) in the TE mode. For SWG waveguides with narrower widths (W = 400 nm and 450 nm), S_{wg} shows an improved value compared to 500 nm or 550 nm SWG waveguides [Fig. 2(a)], which agrees well with the result in Ref. [7]. However, for sensitivity, the maximum value does not appear at the same duty cycle condition like S_{wg} does, as depicted in Fig. 2(b). That is due to the drop in n_g at the low η region, resulting in a growth of S_{bulk} .

Figure 3(a) shows cross sections of the electric field distribution for SOE-SWG, standard-SWG, and thick-SWG geometries, respectively, in both silicon pillars and gaps in the TE mode. The duty cycle for each geometry is based on the minimum $n_{\rm eff}$ for a 2- μ m-thick BOX layer to minimize the substrate leakage [9]. Compared to standard SWGs ($W=500\,$ nm, $t_{\rm Si}=220\,$ nm), both SOE-SWG and thick-SWG geometries show an extended mode profile into the cladding. Similar to Fig. 2, we compared the waveguide properties among these SWG geometries and plotted results in Figs. 3(b) and 3(c).

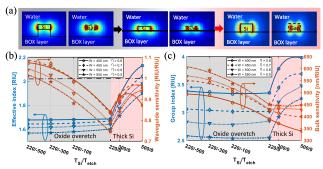


Fig. 3. (a) Cross sections of the electric field distribution of three different SWG silicon pillars and gaps in the TE mode. (b) Simulated effective index (left) and waveguide mode sensitivity (right), and (c) simulated group index (left) and bulk sensitivity (right) versus different thicknesses of silicon and overetch substrate layers. The gray region represents the SOE-SWG geometry, and the pink region represents the thick-SWG geometry.

 $T_{\rm Si}/T_{\rm etch}$ represents the thickness of the silicon pillar/the overetch substrate in each geometry. It is observed that for the thick-SWG geometry (pink region), both n_{eff} and n_{g} increase significantly as the pillar thickness increases. Although S_{wg} also grows (except SWG waveguide with W = 400 nm and $t_{Si} = 500$ nm, which may not support a propagation mode), S_{bulk} presents a downward trend as a function of the pillar thickness. For the SOE-SWG geometry (gray region), the overetch substrate does not influence $n_{\rm eff}$ and $n_{\rm g}$ (blue curves) much, but improves the waveguide mode sensitivity to more than one [orange curves above the dashed line in Fig. 3(b)], which matches the findings in Ref. [10]. It can be explained by the high susceptibility of the SOE-SWG geometry: a slight cladding index variation changes the mode profile, resulting in a larger mode effective index change. Therefore, an enhanced S_{bulk} is obtained for the resonator-based SOE-SWG sensor compared to other geometries, as presented in Fig. 3(c).

Sensing architectures were fabricated using electron-beam lithography (EBL) with plasma etching on an SOI platform $(t_{Si} = 220 \text{ nm}, t_{BOX} = 2 \text{ }\mu\text{m})$ by Applied Nanotools Inc., with fabrication details provided in Ref. [11]. Before the anisotropic SOE process, we characterized optical and sensing performance of fabricated SWG sensors and compared them with the simulation results (shown in Fig. 4). The bulk sensitivity was demonstrated by introducing a series of IPA (purity \geq 98%) solutions, where RIs of dilutions were estimated based on the volume ratio, through a polydimethylsiloxane (PDMS, SYLGARD 184, Dow Corning) microfluidic gasket. The temperature was controlled at 25°C during the experiment by a temperature controller (LDC501, Stanford Research Systems). The group index of each geometry was calculated using $n_g = \lambda^2/(2\pi R \times FSR)$, where R is the radius $(R = 30 \mu m)$, and FSR is the free spectral range of the ring resonator. Figure 4(a) shows the wavelength shift of SWG geometries, with varied W and η , as a function of the cladding index change due to different IPA concentrations. The slope of each curve represents the bulk sensitivity, which is depicted in Fig. 4(b). Among them, a bulk sensitivity of multi-box SWG sensors was also measured, presenting S_{bulk} of 570 nm/RIU, close to the previous measurement [11]. n_g and S_{wg} were calculated based on the aforementioned equations, where FSRs were

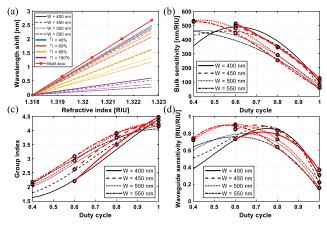


Fig. 4. (a) Measured wavelength shift versus the RI change in cladding for each sensing architecture. Measured (red curves) and simulated (black curves) (b) bulk sensitivities, (c) group indices, and (d) waveguide mode sensitivities versus the duty cycle of SWG-based sensors with different widths.

measured from transmission spectra at 1550 nm, and $\partial\Gamma$ was the cladding index change, plotted in Figs. 4(c) and 4(d). No obvious resonant peaks for SWG sensors with W=400 nm and 450 nm at $\eta=0.4$ were observed due to the low waveguide confinement, thus not presented in Fig. 4. Compared to the simulation results (black curves), measurements (red curves) show a slightly higher S_{bulk} at the low η region ($\eta=0.4-0.6$). That can be explained due to the fabrication imperfection, such as overexposure, which has a stronger influence under low η conditions.

After characterization, the chip was cleaned by piranha solution (3:1H₂SO₄:H₂O₂) at 100°C for 10 min. Then, a photoresist (AZ 5214E-IR, Capitol Scientific) was spin-coated on the chip and patterned through photolithography, where all SWG microring resonators (MRRs) were exposed, but grating couplers and waveguides were protected. The SiO₂ SOE process was realized by using a deep reactive ion etching (DRIE) system (SPTS Rapier) with $Ar/C_4F_8/O_2$ gas at 300:65:35 sccm. The pressure was set to 150 mT, with inductively coupled plasma (ICP) power of 1000 W and platen power of 400 W, respectively. The platen temperature was 10°C during the etching. To obtain a 300-nm-deep overetch, the chip was etched for 40 sec. Last, the chip was immersed in acetone to remove the photoresist and rinsed with IPA and DI water. After drying, SOE-SWG devices were characterized by using a scanning electron microscope (SEM, Helios NanoLab 650) system, as depicted in Fig. 5. It can be observed in Fig. 5(b) that approximately 285 nm SiO₂ and 30 nm Si have been etched, respectively, during the SOE process, indicating a SiO₂/Si etch selectivity of 10:1. However, not only the top surface but also sidewalls around each Si pillar were influenced by the etchant, which turns the SWG block into a trapezoidal object. In addition, the sidewall roughness became worse compared to the one with no SOE process [presented in Figs. 5(b) and 5(c)], which may induce more losses in the resonator. Cross-sectional images of the SOE-SWG waveguide were achieved by using a focused ion beam (FIB) milling system, in the propagation and transverse directions. A 2-µm-thick platinum (Pt) layer was deposited as the protection layer before the FIB. As shown in Fig. 5(d), the Si pillar shows a corn-like shape in the propagation direction, with a sidewall angle of 80°,

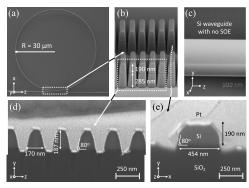


Fig. 5. SEM images of the SOE-SWG device, with the (a) top view of the MRR, and the (b) 50-deg-tilted side view at the coupling region. (c) SEM image of the side-view of a strip waveguide before the SOE process. SEM images with the FIB-milled SOE-SWG waveguide ($W = 500 \, \text{nm}, \, \eta = 60\%$) cross sections in the (d) propagation direction and (e) transverse direction.

close to the waveguide with no SOE process in Ref. [12]. In the transverse direction [Fig. 5(e)], the SWG pillar shows a width of 454 nm. Roughly 50 nm of Si have been etched away.

Transmission spectra of the proposed SWG sensors were re-measured under water cladding after the SOE process. Based on measurement results, the quality factor ($Q = \lambda_{\rm res}/\Delta\lambda_{\rm FWHM}$, where $\Delta\lambda_{\rm FWHM}$ is the full width at half-maximum of the resonant peak) and the group index were extracted and are plotted in Figs. 6(a) and 6(b). In contrast with standard-SWG MRRs (blue curves), 285-nm SOE-SWG MRRs (orange curves) show reduced Q and $n_{\rm g}$ values, which results from the undesired silicon pillar etching during the SOE process. In addition, due to the relatively low etch selectivity, transmission plots for SOE-SWG MRRs with $\eta = 40\%$ and W = 400 nm to 550 nm, and with $\eta = 60\%$ and W = 400 nm present no resonant peaks.

To compare bulk sensitivities, the same IPA dilutions, from 2% to 8% (v/v), were employed again for SOE-SWG

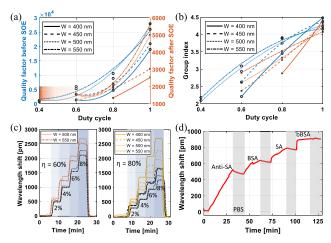


Fig. 6. Measured (a) quality factors and (b) group indices versus the duty cycle of SWG waveguides before (blue) and after (orange) the SOE process. (c) Resonant wavelength shift as a function of IPA concentrations. Orange steps (left) and yellow steps (right) represent SOE-SWG rings with $\eta = 60\%$ and 80%, respectively. Black steps are wavelength shifts before the SOE process. (d) Surface bio-sandwich sensing results on the SOE-SWG sensor with W = 500 nm and $\eta = 60\%$.

Width (nm)	Duty Cycle	S _{bulk} (nm/RIU)		S_{wg} (RIU/RIU)		<i>i</i> DL (RIU)	
		before SOE	after SOE	before SOE	after SOE	before SOE	after SOE
400	60%	514	N/A	0.732	N/A	2.15×10^{-3}	N/A
	80%	348	569	0.786	1.055	9.46×10^{-4}	2.01×10^{-3}
450	60%	500	N/A	0.847	N/A	5.84×10^{-4}	N/A
	80%	345	480	0.835	1.011	6.59×10^{-4}	1.69×10^{-3}
500	40%	533	N/A	0.719	N/A	4.15×10^{-3}	N/A
	60%	479	575	0.905	0.966	5.48×10^{-4}	1.75×10^{-3}
	80%	292	411	0.730	0.883	7.71×10^{-4}	1.88×10^{-3}
550	40%	527	N/A	0.741	N/A	2.45×10^{-3}	N/A
	60%	447	530	0.889	0.990	5.78×10^{-4}	1.83×10^{-3}
	80%	253	349	0.638	0.917	5.77×10^{-4}	2.02×10^{-3}

Table 1. Sensor Performance of SWG Architectures before and after the SOE Process at 1550 nm

MRR sensors. Resonant wavelength shifts as a function of the IPA concentration are presented in Fig. 6(c) for SWG architectures before (orange and yellow) and after (black) the SOE process, among which a maximum bulk sensitivity is achieved for the SOE-SWG MRR with W = 500 nm and $\eta = 60\%$ ($S_{\text{bulk}} = 575 \text{ nm/RIU}$), roughly 1.2-times standard-SWG MRRs [5]. According to the measured Q and $n_{\rm g}$ in Figs. 6(a) and 6(b), the waveguide mode sensitivity, as well as the intrinsic detection limit (iDL), can be obtained at 1550 nm wavelengths for SWG architectures before and after the SOE process. The intrinsic detection limit describes the change in index corresponding to one resonator linewidth shift $[iDL = \lambda_{res}/(S \times Q)]$, which eliminates the uncertainty among sensors with different assays and experimental systems [13]. As listed in Table 1, after the SOE process, sensor performances in terms of the S_{bulk} and S_{wg} are improved. Especially for the MRR with W = 400 nm and 450 nm, S_{wg} exceeds one and is close to the aforementioned simulation result in Fig. 3(b). However, due to the sharply reduced Q, iDL gets worse to the order of 10^{-3} RIU after the SOE process. Last, a standard bio-sandwich assay was introduced to the SOE-SWG MRR sensor (W = 500 nm and $\eta = 60\%$) for biosensing demonstration. By sequentially injecting protein A, anti-streptavidin (anti-SA), bovine serum albumin (BSA), streptavidin (SA), and biotinylated-BSA (bBSA) solutions, biomolecular interactions with specific and non-specific targets were performed on the proposed sensor surface [Fig. 6(d)]. Each solution injection was followed by a 10-min PSB buffer rinse (gray areas) to remove unbound molecules. Details of the bio-sandwich assay can be found in Ref. [5]. The total wavelength shift for surface interactions is $\sim 900\,$ nm, lower than the former result in Ref. [5] because of the shorter reaction time.

In conclusion, we have demonstrated a SOE-SWG-based silicon architecture for sensor performance enhancement. By vertically overetching the SiO₂ between each silicon pillar, the SWG-based waveguide achieves a reduced group index and an enlarged waveguide mode sensitivity simultaneously. Experiment results indicate that the SOE-SWG configuration has improved sensor performance, with a bulk sensitivity as high as 575 nm/RIU. However, due to the low etch selectivity, the etchant also etches the silicon layer (~30 nm) during the 285-nm SOE process, which decreases the thickness and increases the sidewall roughness of silicon boxes. This results in higher substrate leakage losses and sidewall scattering losses,

both of which reduce the Q, thus increasing the $i\mathrm{DL}$. Further work will focus on optimizing the etching process to improve the etch selectivity, and compensating for the etching effect by pre-enlarging the silicon pillar in the as-drawn layout.

Funding. China Scholarship Council; Natural Sciences and Engineering Research Council of Canada.

Acknowledgment. The authors would like to thank Lumerical Inc. for the simulation software, Matthias Köfferlein's KLayout for the layout tool, Applied Nanotools Inc. for chip fabrication, 4D LABS at Simon Fraser University for etching, and Dr. Gethin Owen for SEM imaging.

Disclosures. The authors declare no conflicts of interest.

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