

Family name: ..... First name: ..... Group: .....

**ANSWER SHEET****Exercise 1**

1.

Q2	Q1	Q0	D2	D1	D0
1	1	1			
1	0	1			
1	0	0			
0	1	1			
0	1	0			
0	0	1			
0	0	0			

2.

	Q1 Q0				
	D0	00	01	11	10
Q2	0				
	1				

**D0 =**

	Q1 Q0				
	D1	00	01	11	10
Q2	0				
	1				

**D1 =**

	Q1 Q0				
	D2	00	01	11	10
Q2	0				
	1				

**D2 =****Exercise 2**

1. ROM:  RAM:  P1:  P2:	2. Device-selection bits:
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3. $CS_{ROM} =$  $CS_{RAM} =$	$CS_{P1} =$  $CS_{P2} =$
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4.

Device	Lowest Address	Highest Address
ROM		
RAM		
P1		
P2		

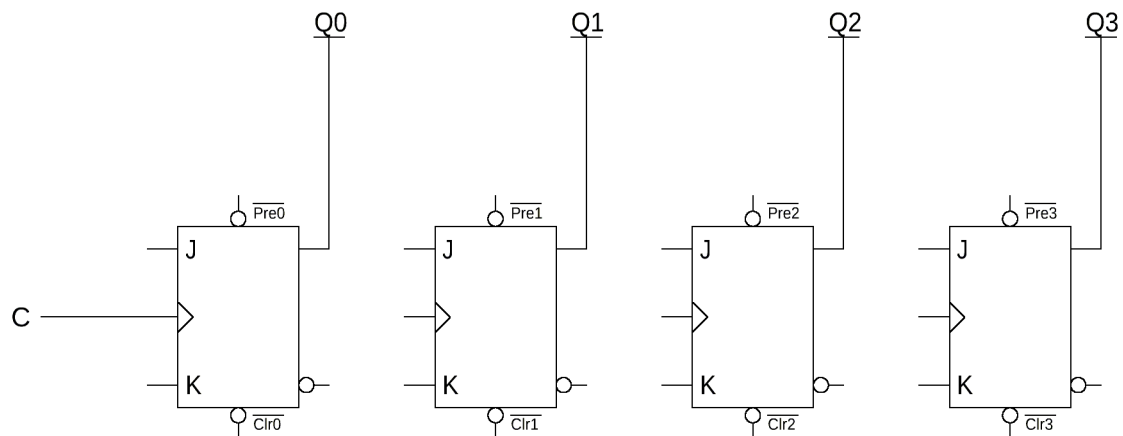
**Exercise 3**

Figure 1

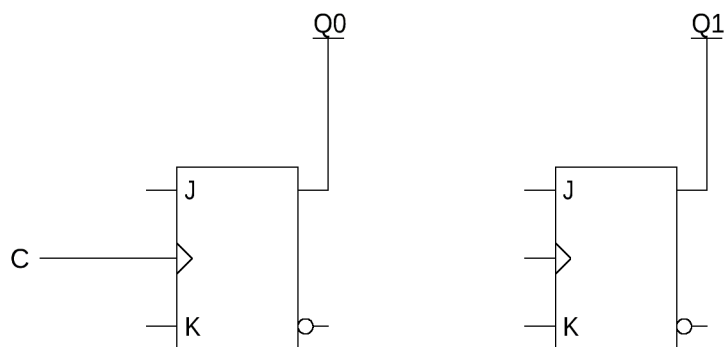


Figure 2

**Exercise 4**

1.

Number	S	E	M
428			
51.078125			

2.

IEEE-754 Representation	Associated Representation
4354000000000000 <sub>16</sub>	
0010100000000000 <sub>16</sub>	

**Exercise 5**

Question about memory devices	Answer
How can we connect memory devices in order to enlarge the depth?	
A memory has a width of 4 bits and a capacity of 64 KiB. How many address lines does this memory have?	
A memory has an 8-bit data bus and a 15-bit address bus. In a power of two, what is the capacity in bits of this memory?	
An <b>M1</b> memory has an 8-bit data bus and a 16-bit address bus. Two <b>M1</b> memories are connected in series to build an <b>M2</b> memory. What is the size of the address bus of the <b>M2</b> memory?	

Feel free to use the blank space below if you need to: