Two in One Low power XOR/XNOR Gate

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Abstract

With the increasing technology, the size of the transistors is reducing. The reducing size leads to the tradeoff between power, efficiency and switching time. Because of which there is requirement to design low power transistor with less area and lesser number of gates. The design should use lesser power as well. Thus, making it more and more efficient.

1 Reference Circuit Details

As shown in the figure we have two cross coupled circuits of PMOS logic and NMOS logic as shown in the figure.

On the PMOS logic we are getting the output as XOR while in the NMOS block we get the output as XNOR.

The transistors M4 and M3 behave as a pass transistor and pass the output of M1, M2 and M5, M6 respectively.

The advantage of the above circuit is that it uses only 6 transistors and gives both outputs of XOR and XNOR while the general circuit uses 8 transistors with only one output either XOR or XNOR.

This way it consumes less space and less power and is efficient in many ways.

2 Implemented Circuit

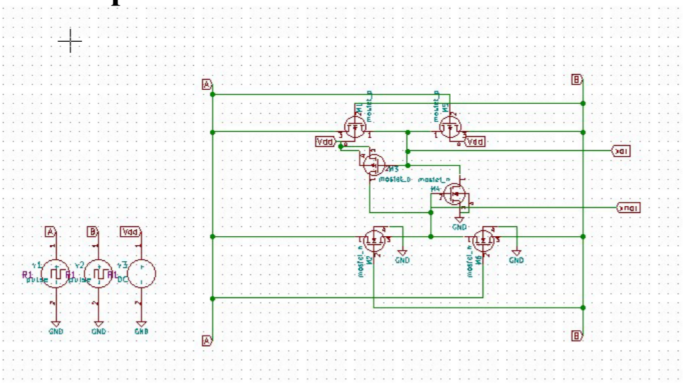

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

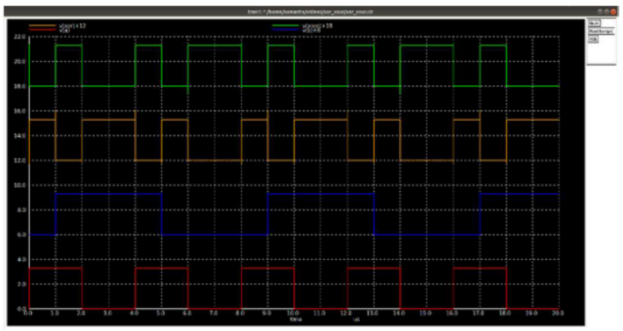

Figure 2: Implemented waveform.

References

1. K. Ravali, N. R. Vijay, S. Jaggavarapu and R. Sakthivel, "Low power XOR gate design and its applications," *2017 Fourth International Conference on Signal Processing, Communication and Networking (ICSCN)*, 2017, pp. 1-4, doi: 10.1109/ICSCN.2017.8085699.