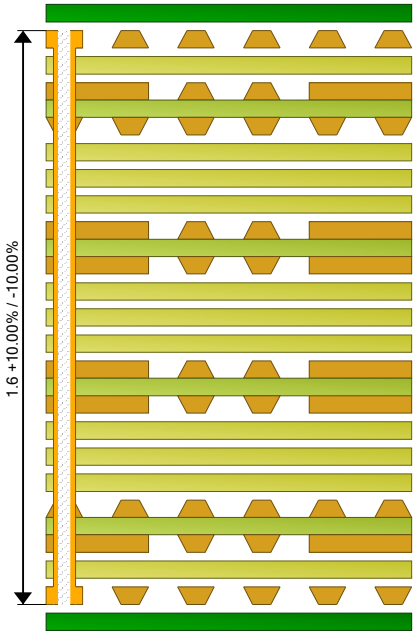
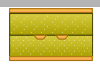
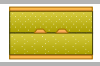


Layer	Stack up	Description	Base Thickness	Finish Thickness	Mask Thickness	εr	Resin Content	Impedance ID	Type	Notes-1	Data Filenames
		Soldermask			0.020	4.100			SolderMask	10	
1		Foil	0.018	0.043				1, 2, 3	Foil	0	
		VT47-1080	0.074	0.074		3.950	0.000		PREPREG		
2			0.018	0.018							
		VT-47	0.102	0.102		4.120	0.000		Core		
3			0.018	0.018				4, 5, 6			
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
4			0.018	0.018							
		VT-47	0.102	0.102		4.120	0.000		Core		
5			0.018	0.018							
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
6			0.018	0.018							
		VT-47	0.102	0.102		4.120	0.000		Core		
7			0.018	0.018							
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
		VT47-2113	0.094	0.094		4.060	0.000		PREPREG		
8			0.018	0.018				7, 8, 9			
		VT-47	0.102	0.102		4.120	0.000		Core		
9			0.018	0.018							
		VT47-1080	0.074	0.074		3.950	0.000		PREPREG		
10		Foil	0.018	0.043				10, 11, 12	Foil	0	
		Soldermask			0.020	4.100			SolderMask	10	

Copper Thickness = 0.228 | Dielectric Thickness = 1.400 | Solder Mask Thickness = 0.040 | Stack Up Thickness = 1.628 | Stack Up Thickness with Soldermask = 1.668 |

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Broadside 2nd Layer	Calculated Impedance	Target Impedance	Tol (+/- %)
1		Coated Microstrip 1B	1	2	0	0.114	0.000	0.000	0	49.580	50.000	10.000
2		Edge Coupled Coated Microstrip 1B	1	2	0	0.114	0.160	0.000	0	89.630	90.000	10.000
3		Edge Coupled Coated Microstrip 1B	1	2	0	0.100	0.220	0.000	0	98.920	100.000	10.000
4		Offset Stripline 1B1A	3	2	4	0.120	0.000	0.000	0	50.320	50.000	10.000

StackName: Fedevel_OpenRex PCB V1I1_10L_VT47_v04	Version:	Revision:	Modification:	Date of Revision:	Editor	Page 1/2
Date: 06/1/2016	Associated Documents:					
Author: Mostefa Abdali						
Department: IDS						
Site: Tewkesbury						

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Broadside 2nd Layer	Calculated Impedance	Target Impedance	Tol (+/- %)
5		Edge Coupled Offset Stripline 1B1A	3	2	4	0.130	0.190	0.000	0	90.730	90.000	10.000
6		Edge Coupled Offset Stripline 1B1A	3	2	4	0.110	0.210	0.000	0	98.990	100.000	10.000
7		Offset Stripline 1B1A	8	7	9	0.120	0.000	0.000	0	50.320	50.000	10.000
8		Edge Coupled Offset Stripline 1B1A	8	7	9	0.130	0.190	0.000	0	90.730	90.000	10.000
9		Edge Coupled Offset Stripline 1B1A	8	7	9	0.110	0.210	0.000	0	98.990	100.000	10.000
10		Coated Microstrip 1B	10	9	0	0.114	0.000	0.000	0	49.580	50.000	10.000
11		Edge Coupled Coated Microstrip 1B	10	9	0	0.114	0.160	0.000	0	89.630	90.000	10.000
12		Edge Coupled Coated Microstrip 1B	10	9	0	0.100	0.220	0.000	0	98.920	100.000	10.000

Column Position	Drill Image	1st Layer	2nd Layer	Drill Type	Fill Type	Minimum Size	Data Filenames
1		1	10	Mechanical PTH	None	0.200	

Notes

StackName: Fedevel_OpenRex PCB V1I1_10L_VT47_v04	Version:	Revision:	Modification:	Date of Revision:	Editor	Page 2/2	eXception PCB SOLUTIONS
Date: 06/1/2016	Associated Documents:						
Author: Mostefa Abdali							
Department: IDS							
Site: Tewkesbury							