Features

- Compatible with HDMI 1.4a
- Supports 2.5 Gbps signaling rate for 480i/p, 720i/p, and 1080i/p resolutions up to 12-bit color depth
- Integrated receiver termination
- Adaptive receiver equalization to accommodate to different input cable lengths
- DDC buffer link
- CEC buffer link
- Intra-pair skew < 40 ps
- Inter-pair skew < 65 ps
- ***System Level ESD Protection Exceeds 8 kV (direct contact) for TMDS Inputs and DDC Interface***
- Supply voltage, VCC= 3.3 V +/- 5%
- Controllable shutdown and standby modes for power saving
- Controllable logic states for HPD output
- 5-V tolerance on all side band signals
- 64-pin LQFP package
- ***Green part*** and 260 °C reflow rated

Applications

- Digital TV
- Digital projector
- Digital monitor
- Audio/video receiver

Description

The AZHW371 is a 3-port High-Definition Multimedia Interface (HDMI) or DVI switch which allows up to 3 HDMI or DVI ports to be switched to a single display terminal. Four TMDS channels, one hot plug detector, and a digital display control (DDC) interface are supported on each port. Each TMDS channel allows signaling rates up to 2.5 Gbps to allow 1080p resolution in 12-bit color depth.

With two control pins, the AZHW371 can be operated at the shutdown mode. At this condition, all TMDS input terminations are disconnected and at the state of high impedance. Moreover, the DDC links are disabled due to that all internal devices are turned off and all HPD outputs are connected to the HPD_SINK. This allows the initiation of the HDMI physics address discovery process. Termination resistor (50-Ω), pulled up to VCC, are integrated at each TMDS receiver input. External terminations are not required as shown in Fig.1.

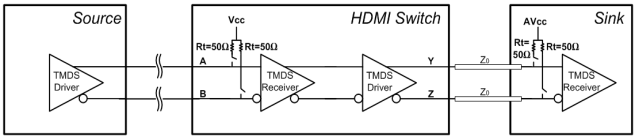


Fig.1. TMDS internal termination

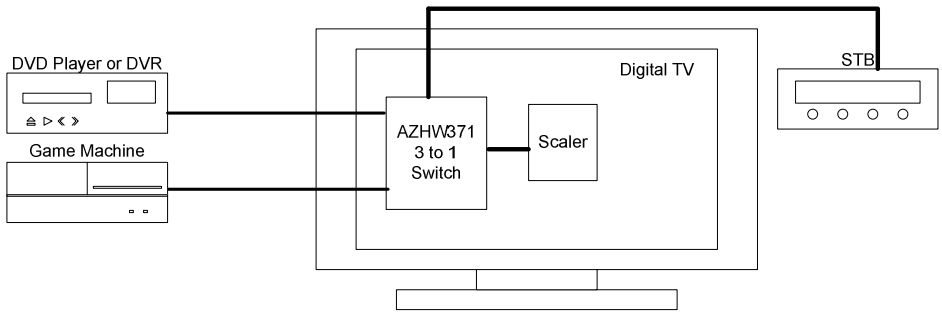
The AZHW371 provides adaptive input equalization for different ranges of cable lengths. Each TMDS receiver owns frequency responsive equalization circuits. A 5k-ohm (recommended value) calibration resistor is tied to GND for EQ pin, the receiver with optimized equalization supports the connection in different range HDMI cables. Moreover, A 9k-ohm (recommended value) calibration resistor is tied to GND for RP1 (pin 49) pin, the receiver of port 1, port 2 and port 3 with adaptive equalization supports the input connection in different range HDMI cables. The AZHW371 supports two types of power saving operations. When a system is under shutdown mode and there is no digital audio/visual content from a connected source to minimize power

consumption from TMDS inputs, outputs, and internal circuits. When a system is under standby mode (PS at logic high), only TMDS clock inputs, outputs and termination are turned on, and the selected DDC repeater link from the source to sink. At this state, the system can be quick recovery as the digital audio/visual content from a connected source. Otherwise, to filter supply noise, all VCC pins are recommended to have a 0.01 uF capacitor tied from each VCC pin to ground directly. For the ESD protection function, the AZHW371 is designed to withstand the ESD level (IEC61000-4-2) to contact mode 8 kV. For the requirements of application, a higher protection level is needed. The AZHW371 can provide TMDS pairs, DDC, and HPD pins' ESD levels (IEC61000-4-2) to contact mode 8 kV. And external ESD components are not required for the criteria of ESD contact mode 8 kV.

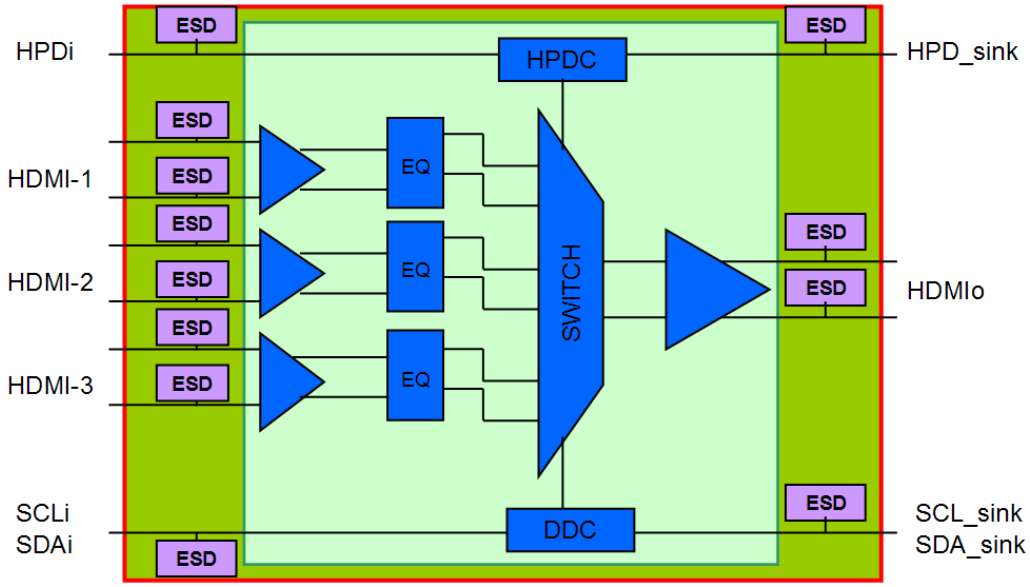
Furthermore, the AZHW371 also provides controllable states of HPD outputs. When HPD_ctl set high, all HPD outputs can follow HPD_SINK. For the VSADJ pin, it is recommended to be tied a 6.2-kΩ resistor (10% precision) to control the output swing to the HDMI compliance test.

Finally, the AZHW371 also integrates an HDMI compliant I/O to enable Consumer Electronics Control (CEC) in a DTV. The CEC I/O meets all HDMI compliance test and eliminates the need for additional external components. The device is characterized for operation from 0 °C to 70 °C.

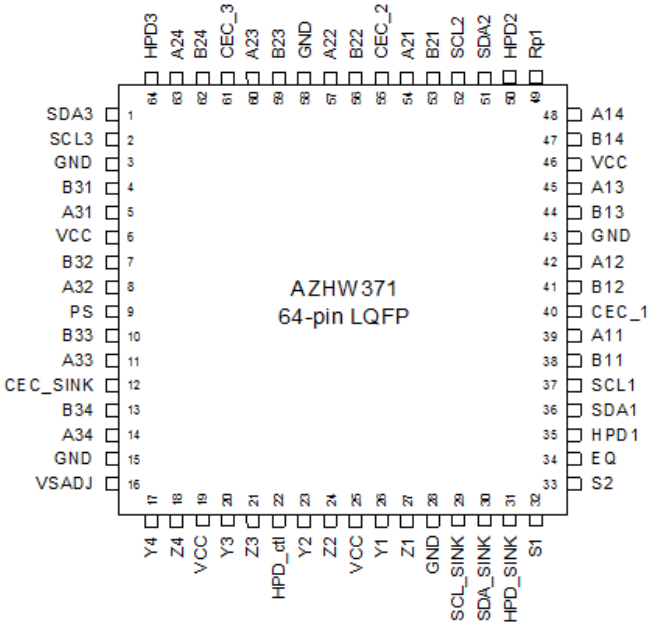
Typical application



Circuit diagram



Pin Configuration



TERMINAL FUNCTIONS

TERMINAL		I/O	Description
NAME	NO.		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
A31, A32, A33, A34	5, 8, 11, 14	I	Source port 3 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
B31, B32, B33, B34	4, 7, 10, 13	I	Source port 3 TMDS negative inputs
GND	15, 28, 43, 58	---	Ground
EQ	34	I	TMDS input equalization calibration
PS	9	I	Power saving selector PS= high---standby mode PS= low---normal mode
HPD_ctl	22	I	HPD output selector HPD_ctl= high---all HPD output follows HPD_SINK HPD_ctl=low---only selected HPD output follows HPD_SINK
HPD1	35	O	Source port 1 hot plug detector output
HPD2	50	O	Source port 2 hot plug detector output
HPD3	64	O	Source port 3 hot plug detector output
HPD_SINK	31	I	Sink port hot plug detector input
SCL1	37	I/O	Source port 1 DDC I^2C clock line
SCL2	52	I/O	Source port 2 DDC I^2C clock line
SCL3	2	I/O	Source port 3 DDC I^2C clock line
SCL_SINK	29	I/O	Sink port DDC I2C clock line
SDA1	36	I/O	Source port 1 DDC I^2C data line
SDA2	51	I/O	Source port 2 DDC I^2C data line
SDA3	1	I/O	Source port 3 DDC I^2C data line
SDA_SINK	30	I/O	Sink port DDC I^2C data line
S1, S2	32,33	I	Source selector

TERMINAL		I/O	Description
NAME	NO.		
VCC	19, 25, 46	---	Power supply
V_{sadj}	16	I	TMDS compliant voltage swing control
CEC_1, CEC_2, CEC_3	40, 55, 61	I/O	Source port 1,2,3 CEC line
CEC_SINK	12	I/O	Sink port CEC line
Y1, Y2, Y3, Y4	26, 23, 20, 17	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	27, 24, 21, 18	O	Sink port TMDS negative outputs
RP1	49	---	Calibration resistor (tied to VCC)

Note. **A11, B11, A21, B21, A31, B31 are TMDS clock inputs. Y1 and Z1 are TMDS clock outputs.**

Table-1-1: Source Selection Lookup (Normal operation)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	H	L	L	**A1/B1 50Ω Terminations are connected** A2/B2 and A3/B3 50Ω Terminations are disconnected	SCL1 SDA1	HPD_SINK	L	L
L	H	L	L	**A2/B2 50Ω Terminations are connected** A1/B1, A3/B3 50Ω Terminations are disconnected	SCL2 SDA2	L	HPD_SINK	L
L	L	L	L	**A3/B3 50Ω Terminations are connected** A1/B1, A2/B2 50Ω Terminations are disconnected	SCL3 SDA3	L	L	HPD_SINK

***Note.* H: logic high; L: logic low.**

Table-1-2: Source Selection Lookup (Normal operation)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	H	L	H	**A1/B1 50Ω Terminations are connected** A2/B2 and A3/B3 50Ω Terminations are disconnected	SCL1 SDA1	HPD_SINK	HPD_SINK	HPD_SINK
L	H	L	H	**A2/B2 50Ω Terminations are connected** A1/B1, A3/B3 50Ω Terminations are disconnected	SCL2 SDA2	HPD_SINK	HPD_SINK	HPD_SINK
L	L	L	H	**A3/B3 50Ω Terminations are connected** A1/B1, A2/B2 50Ω Terminations are disconnected	SCL3 SDA3	HPD_SINK	HPD_SINK	HPD_SINK

***Note.* H: logic high; L: logic low.**

Table-1-3: Source Selection Lookup (Standby mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	H	H	L	**A11/B11 are active** A12, B12, A13, B13, A14, B14, A2n, B2n, A3n, B3n are inactive	SCL1 SDA1	HPD_SINK	L	L
L	H	H	L	**A21/B21 are active** A22, B22, A23, B23, A24, B24, A1n, B1n, A3n, B3n are inactive	SCL2 SDA2	L	HPD_SINK	L
L	L	H	L	**A31/B31 are active** A32, B32, A33, B33, A34, B34, A1n, B1n, A2n, B2n are inactive	SCL3 SDA3	L	L	HPD_SINK

***Note.* H: logic high; L: logic low.**

Table-1-4: Source Selection Lookup (Standby mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	**S2**	**PS**	**HPD_ctl**	**Y/Z**	**SCL_sink SDA_sink**	**HPD1**	**HPD2**	**HPD3**
H	H	H	H	**A11/B11 are active** A12, B12, A13, B13, A14, B14, A2n, B2n, A3n, B3n are inactive	SCL1 SDA1	HPD_SINK	HPD_SINK	HPD_SINK
L	H	H	H	**A21/B21 are active** A22, B22, A23, B23, A24, B24, A1n, B1n, A3n, B3n are inactive	SCL2 SDA2	HPD_SINK	HPD_SINK	HPD_SINK
L	L	H	H	**A31/B31 are active** A32, B32, A33, B33, A34, B34, A1n, B1n, A2n, B2n are inactive	SCL3 SDA3	HPD_SINK	HPD_SINK	HPD_SINK

Note. **H: logic high; L: logic low.**

Table-1-5: Source Selection Lookup (Shutdown mode)

CONTROL PINS				I/O SELECTED		HOT PLUG DETECT STATUS		
S1	S2	PS	HPD_ctl	Y/Z	SCL_sink SDA_sink	HPD1	HPD2	HPD3
H	L	L	H	**A/B are all inactive**	Be pulled high by external pull-up termination	HPD_SINK	HPD_SINK	HPD_SINK

Note. **H: logic high; L: logic low;**

ABSOLUTE MAXIMUM RATINGS

			UNIT
Supply voltage range	VCC		-0.5V to 4V
Voltage range	Anm, Bnm		2.5V to 4V
	Ym, Zm, VSADJ, EQ, HPDn, PS, HPD_ctl, CEC_n, CEC_SINK		-0.5V to 4V
	SCLn, SCL_SINK, SDAn, SDA_SINK, HPD_SINK, S1, S2		-0.5V to 5.5V
Electrostatic discharge	System level (direct contact) (1)	Anm, Bnm, SCLn, SDAn, HPDn, CEC_n	+/-8 KV
	Human body model (2)	Anm, Bnm, SCLn, SDAn, HPDn	+/- 8 KV
		All pins	+/- 4 KV
	Machine model (2)	All pins	+/- 200V
	Charged-device model (2)	All pins	+/- 1000V

*(1) System level: tested in accordance with IEC61000-4-2
*(2) Tested in accordance with JEDEC Standard 22

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
VCC Supply voltage	3.135	3.3	3.465	V
T_A Operating free-air temperature	0	25	70	°C
TMDS differential pins				
V_{IC} Input common mode voltage	VCC-0.4		VCC+0.01	V
V_{ID} Receiver peak-to-peak differential input voltage	150		1560	mV_{P-P}
R_{VSADJ} Resistor for TMDS compliant voltage swing range		6.2		KΩ
RP1 Resistor for TMDS calibration		9		KΩ
EQ Resistor for TMDS equalization calibration		5		KΩ
AV_{CC} TMDS output termination voltage		3.3		V
R_T Termination resistance	45	50	55	Ω
Signaling rate	0		2.5	Gbps
Control pins (PS, HPD_ctl)				
V_{IH} LVTTL High-level input voltage	2		VCC	V
V_{IL} LVTTL Low-level input voltage	GND		0.8	V
DDC I/O pins				
$V_{I(DDC)}$ DDC input voltage	GND		5.5	V
Status and source selector pins (S1, S2, HPD_SINK)				
V_{IH} LVTTL High-level input voltage	1.5		5.5	V
V_{IL} LVTTL Low-level input voltage	GND		0.8	V

Electrical Characteristics
Over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_{CC} Supply current	R_T = 50 Ω VCC = 3.3V AV_{CC} = 3.3V Data pattern = 2.5 Gbps Clock = 250 MHz	S1/S2= L/H H/H L/L PS=L		170		mA
		S1/S2= H/L		1		mA
		S1/S2= L/H H/H L/L PS=H		2		mA
TMDS DIFFERENTIAL PINS (A/B; Y/Z)						
V_{OH} Single-ended high-level output Voltage	R_T = 50 Ω VCC = 3.3V AV_{CC} = 3.3V		AVCC -10	AVCC	AVCC +10	mV
V_{OL} Single-ended low-level output voltage			AVCC -700	AVCC -460	AVCC - 400	mV
V_{swing} Single-ended output swing voltage			400	460	700	mV
$I_{(os)}$ Short circuit output current				11.5	14	mA
R_{INT} Input termination resistance	V_{IN} = 2.9 V		45	50	55	Ω
STATUS AND SOURCE SELECTOR PINS						
V_{IH} TTL High-level input voltage			2.5		5.5	V
V_{IL} TTL Low-level input voltage			GND		0.8	V

Electrical Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DDC I/O PINS					
$C_{IO(sink)}$ Input/output capacitance	$V_{I(PP)}$ = 1V, 100 kHz		6		pF
$V_{IH(sink)}$ High-level input voltage		2.0		5.5	V
$V_{IL(sink)}$ Low-level input voltage		GND		0.8	V
$C_{IO\ (port\ 1:3)}$ Input/output capacitance	$V_{I(PP)}$ = 1V, 100 kHz		6		pF
$V_{IH(port\ 1:3)}$ High-level input voltage		2.0		5.5	V
$V_{IL(port\ 1:3)}$ low-level input voltage		GND		0.8	V
STATUS AND SOURCE SELECTOR PINS					
V_{IH} TTL High-level input voltage		2.5		5.5	V
V_{IL} TTL Low-level input voltage		GND		0.8	V

- **(1) All typical values are at 25 °C and with a 3.3-V VCC supply.**

SWITCHING CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted)

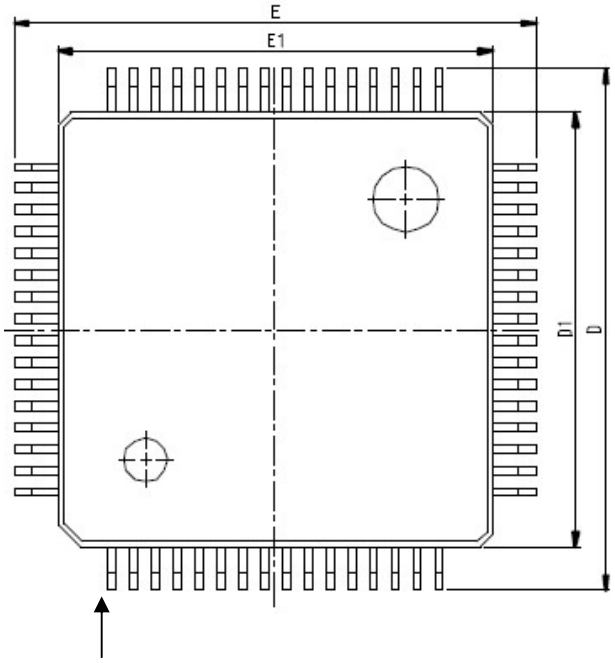
PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TMDS DIFFERENTIAL PINS (Y/Z)					
t_{PLH} Propagation delay time, low-to-high-level output	R_T = 50 Ω AV_{CC} = 3.3V Am/Bm (1) = 250 MHz clock Am/Bm (2:4) = 2.5 Gbps pattern		1200	1500	ps
t_{PHL} Propagation delay time, high-to-low-level output			1200	1500	ps
t_r Differential output signal rise time		75		240	ps
t_f Differential output signal fall time		75		240	ps
$t_{sk(p)}$ Pulse skew (t_{PHL}-t_{PLH})			10	50	ps
$t_{sk(D)}$ Intra-pair differential skew			20	40	ps
$t_{sk(0)}$ Inter-pair differential skew			18	65	ps
$t_{jt(PP)}$ Peak-to-peak output jitter(Y1/Z1)			40	50	ps
$t_{jt(PP)}$ Peak-to-peak output jitter (Y2/Z2; Y3/Z3;Y4/Z4)			75	120	ps
t_{sx} Select to switch output			25	60	ns

***(1) All typical values are at 25℃ and with a 3.3-V VCC supply.**

64-pin LQFP

PACKAGE DIAGRAMS

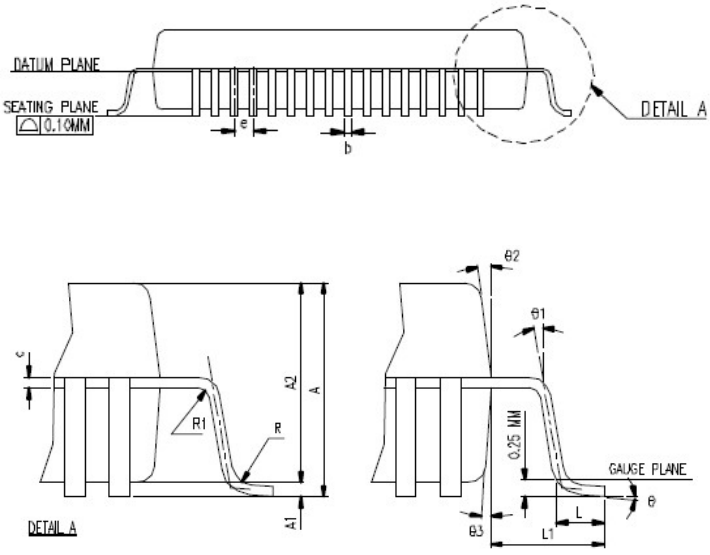
TOP VIEW



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BCD)					

⚠ NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSIN IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

SIDE VIEW



Marking Code

Part Number	Marking Code
AZHW371	AZHW371

Revision History

Revision	Modification Description
Revision 2012/03/09	Preliminary Release.
Revision 2012/05/21	Formal release. Rp1 is changed from 5k to 9k.
Revision 2012/07/31	Formal release. Icc current is changed from 180 mA to 170 mA.
	Standby current is changed from 8 mA to 2 mA.