Department of Electrical and Electronic Engineering

Project Report Submission

Semester: *Fall 2023*
Course Code: *EEE283L*
Course Title: *Digital Logic Design (Laboratory)*
Section: *02*

Project Title: Designing an Electronic Voting System

Group No.: 01

Group members:

Sl.	***Name***	***ID***
1.	Md. Reshad Al Muttaki	22121091
2.	Mohammad Fasiul Abedin Khan	22121092
3.	Mushfeka Anika Bushra	21321070
4.	Prapty Majumder Golpa	22121032

Date of Submission: *16th December, 2023*

Table of Contents

EEE283
Open Ended Project

Project Title: Designing an Electronic Voting System.

Problem Statement: Suppose you are an employee of a company and you are advised to develop a majority voting system for electing the 2023 Executive body of the company using logic gate, synchronous, combinational, and arithmetic circuit etc. 60 members in the company can cast votes. Consider you have 6 participants for three positions. The three positions are chairman, vice chairman, and secretary. Develop a system so that the majority vote wins and show the winner and vote counting in multiple 7-segment Displays.

Objectives: The objective of this project include:

- Designing a voting system for 6 candidates and 60 voters.
- Displaying the number of votes for each candidate.
- Selecting Chairman (highest number of votes), Vice-Chairman (second highest number of votes) and Secretary (third highest number of votes) after all the votes are casted.
- Displaying the winners using 7 segment Display.
- Ensuring fair election process.

Background: The democratic process is a fundamental pillar of any society that values the voices and choices of its citizens. Elections, as a part of this process, play a crucial role in shaping the future of a nation or an organization. In the digital age, electronic voting systems have gained prominence due to their potential to streamline the voting process and enhance its integrity (*The Evolution of Voting Technology in America: From Paper to Pixels*, 2023). The proposed project of developing a majority voting system for electing the 2023 Executive body of a company using logic gate, synchronous, combinational, and arithmetic circuit is a practical application of the principles of democratic elections. This project mirrors the electoral process, where individuals cast their votes to elect representatives for various positions.

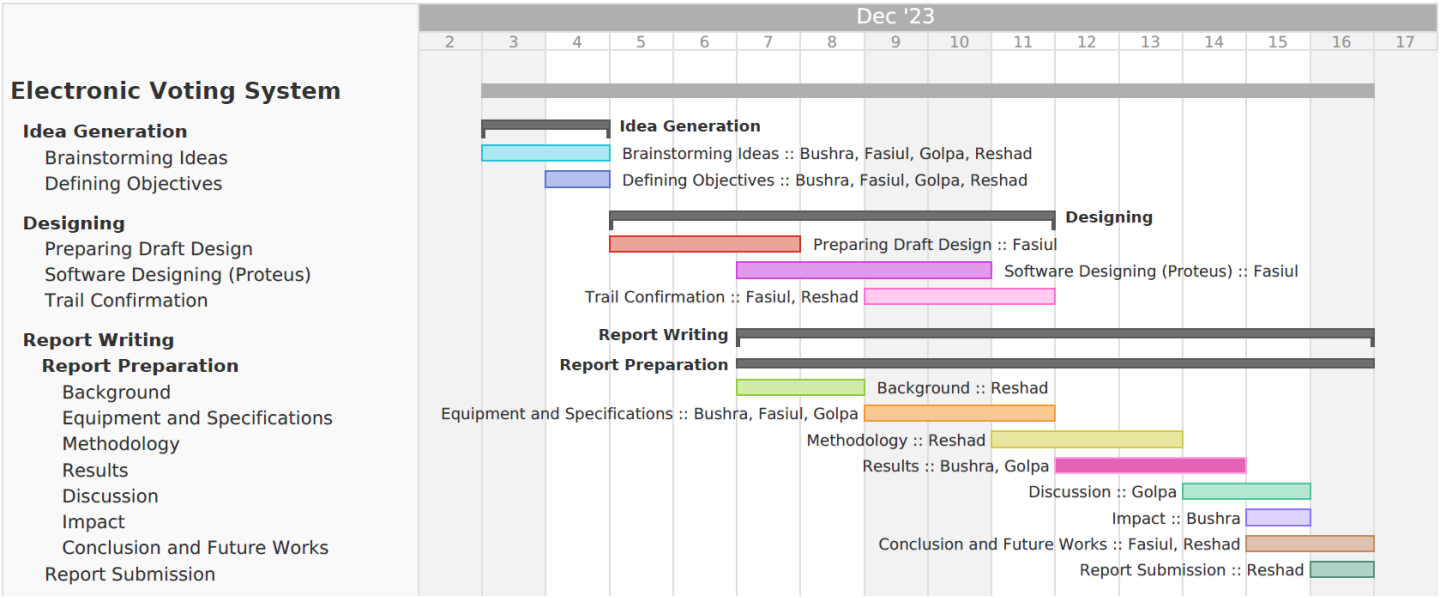
In the context of Bangladesh, the importance of this project is amplified considering the upcoming 2024 National Election. Elections are a fundamental aspect of democracy, allowing citizens to select their leaders and hold them accountable for their performance. The National Election of Bangladesh, scheduled for the first week of January 2024, is a significant event where the citizens exercise their right to vote, influencing the country's governance and future direction (Alamgir, 2023).

The importance of automated election systems extends beyond national boundaries. Automated election systems use appropriate technology to accomplish tasks such as voting, counting, consolidating, canvassing, and transmission of election results (*Online/Automated Elections in the Philippines - Iskomunidad*, 2011). They ensure a fair and transparent election process, reduce human error, and provide quick and accurate results.

The proposed voting system project, therefore, serves as a practical application of these democratic principles within a corporate environment. By developing a system that accurately

counts votes and displays the results in real-time, we can ensure a fair and transparent election process. This not only upholds the democratic values within the organization but also provides a hands-on understanding of the electoral process, reinforcing the importance of active participation in elections.

Gantt Chart:



Workflow Diagram:

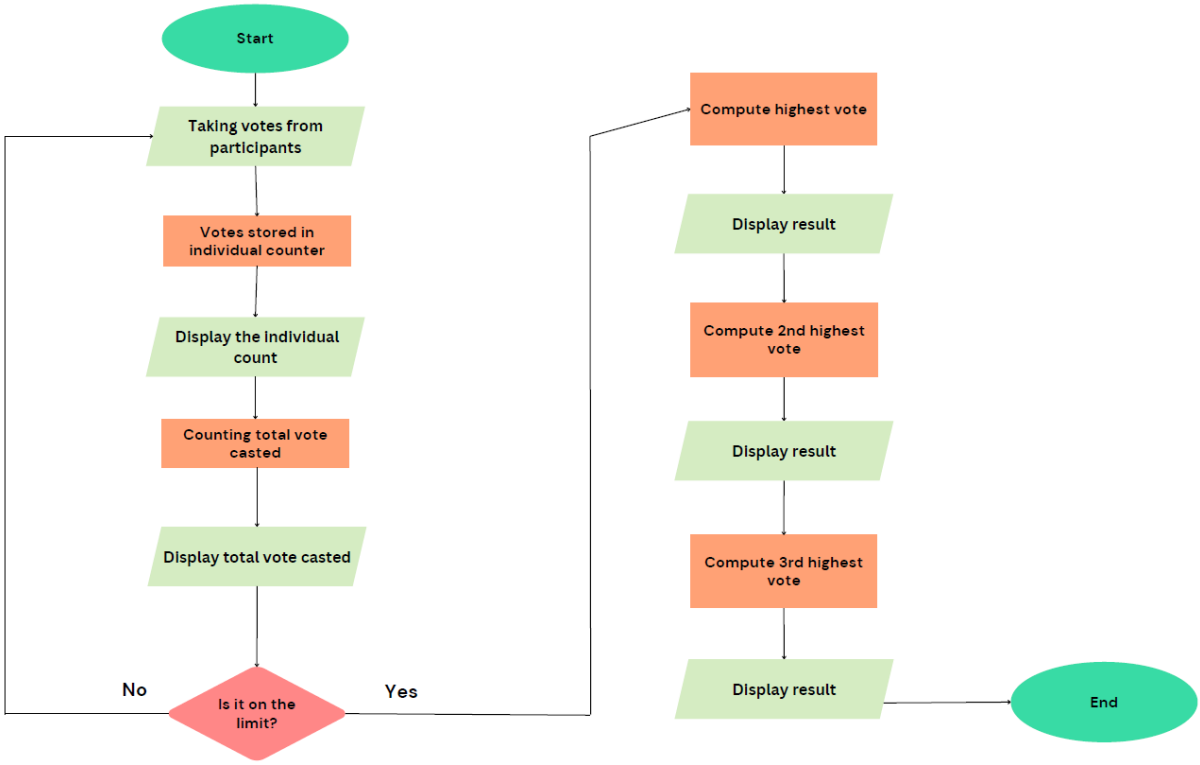


Figure: Flowchart

Equipment and Requirements:

- Basic Gates (AND, OR, NOT)
- Logic Toggle
- 4510 IC (4-bit Up/Down Counter with Preset)
- 7485 IC (4-bit Magnitude Comparator)
- Encoder
- 7 Segment Display
- Power
- Wire
- Ground

In our system design, we used the Basic Gates of various inputs. But the functionality and logic of these gates across various number of inputs are similar. So, the truth tables for 2 input basic gates are shown.

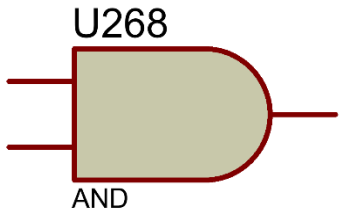


Figure: A 2 input AND gate

Truth Table for a 2 input AND Gate:

Input A	Input B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1

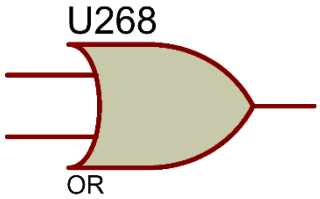


Figure: 2 input OR Gate

Truth Table for a 2 input OR Gate:

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1

1	1	1

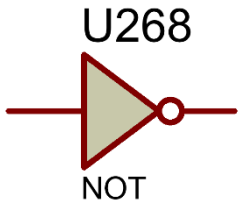


Figure: NOT Gate (Inverter)

Truth Table for a NOT Gate (Inverter):

Input A	Output Y
0	1
1	0

Again, we used 4510 IC as 4-bit Up Counter and cascading 2 such ICs together, we converted it into 8-bit Up Counter and used it as a MOD-256 counter which can count from 0 to 60, i.e., it resets after 60.

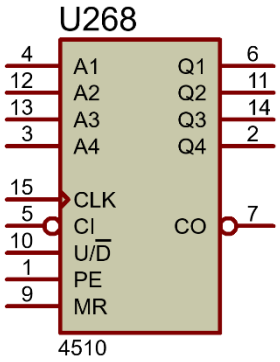


Figure: 4510 IC (4-bit Up/Down Counter with Preset)

Truth Table for a MOD-256 Counter Counting from 0 to 60:

Input (Binary)	**Output (Decimal)**
000000	0
000001	1
…	…
001100	12
…	…
111011	59

111100	60
111101	0 (overflow)
…	…
111111	4 (overflow)

Besides these, we used 7485 IC as 4-bit Magnitude Comparator and cascading two of them together designed a 8-bit Magnitude Comparator and used it inside of the Comparator subcircuit in order to compare the number of votes between the 6 participants.

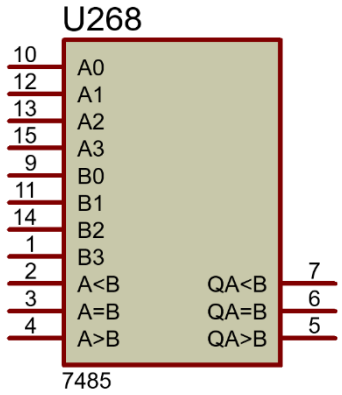


Figure: 7485 IC (4-bit Magnitude Comparator)

Truth Table for a 4-bit Magnitude Comparator:

Comparing Inputs				Cascading Inputs			Outputs		
				A > B	A < B	A = B	A > B	A < B	A = B
$A_3 > B_3$	×	×	×	×	×	×	1	0	0
$A_3 < B_3$	×	×	×	×	×	×	0	1	0
$A_3 = B_3$	$A_2 > B_2$	×	×	×	×	×	1	0	0
$A_3 = B_3$	$A_2 < B_2$	×	×	×	×	×	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	×	×	×	×	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	×	×	×	×	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	×	×	×	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	×	×	×	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	1	0	0	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	1	0	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	0	1	0	0	1
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	×	×	1	0	0	1
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	1	1	0	0	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	0	0	1	1	0

Methodology: The system aims to determine the winners for three positions - chairman, vice chairman, and secretary - through a logic gate-based approach, synchronous design, combinational circuits, and arithmetic circuits.

1. System Architecture

1.1 Overall Circuit Diagram

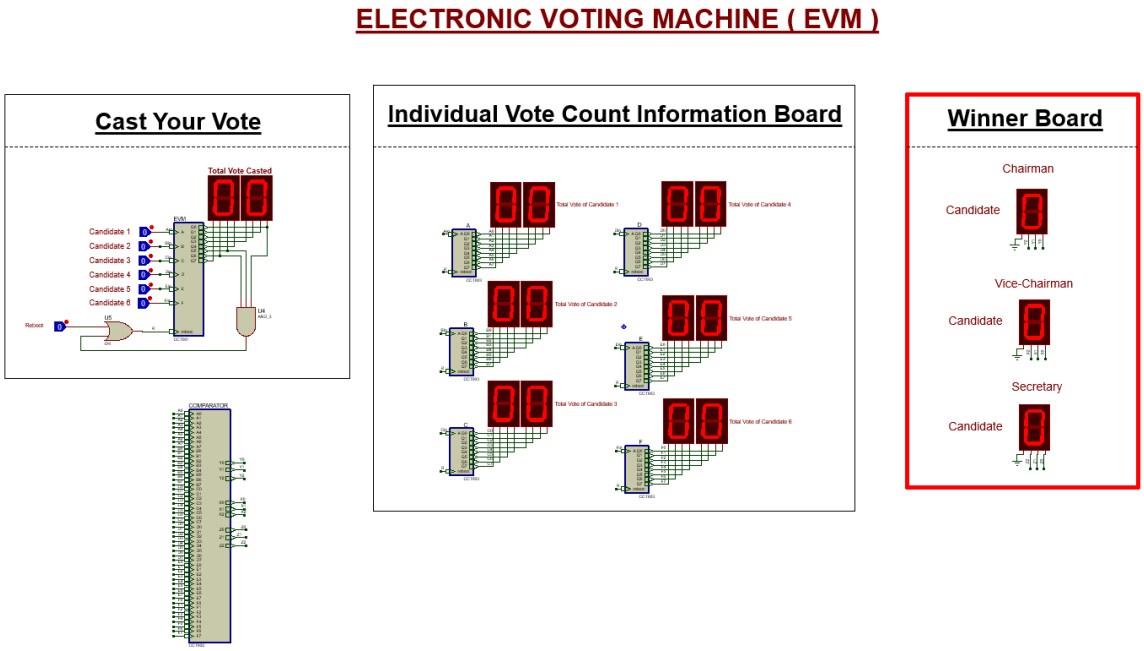


Figure: The Complete Electronic Voting System

1.3 Components

1. The EVM Machine: The EVM machine is the heart of our designed system. All the other components revolve around it. The machine subcircuit contains a counter which takes the votes of each of the participants. The counter subcircuit contains a MOD-256 Up Counter which has clear as the reset. Again, this subcircuit contains two 4510 ICs which are used as 4-bit Up Counters and cascaded together as a 8-bit Up Counter.

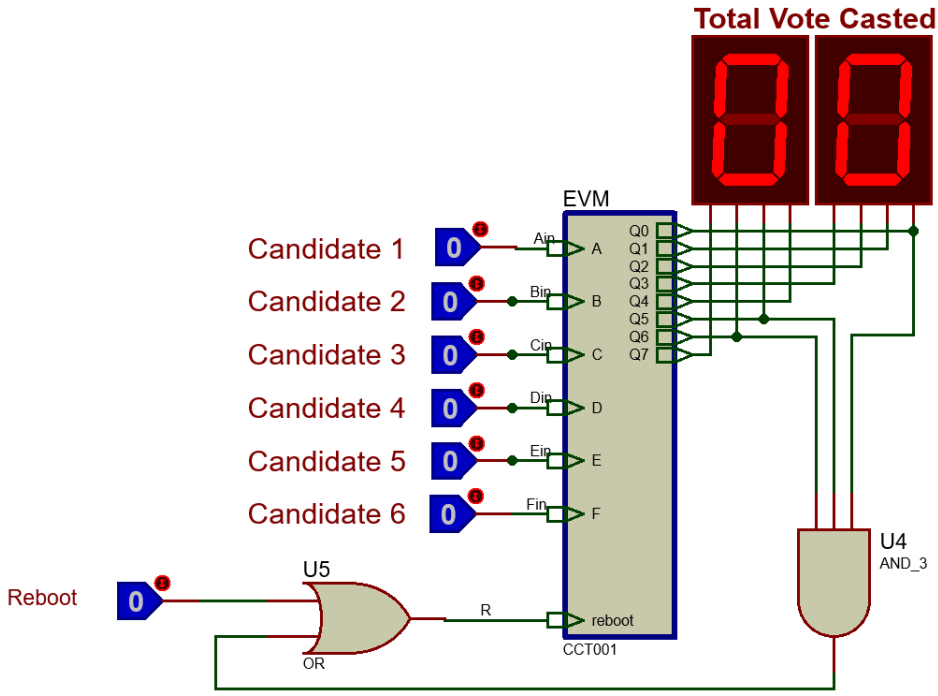


Figure: The Electronic Voting Machine

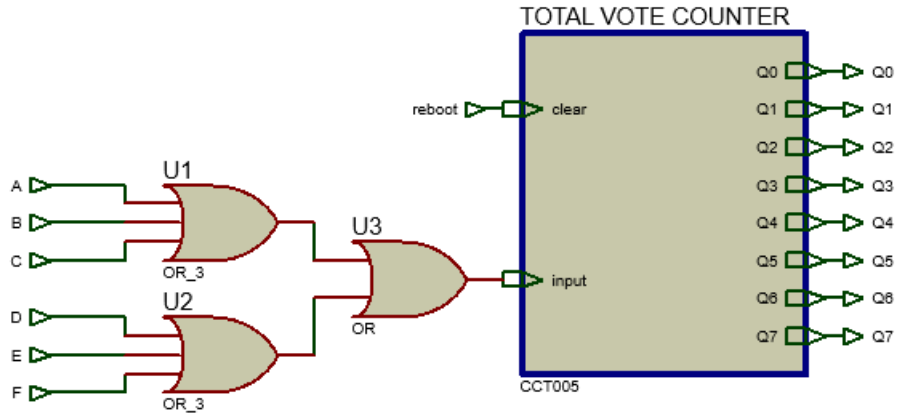


Figure: Child Sheet of the EVM

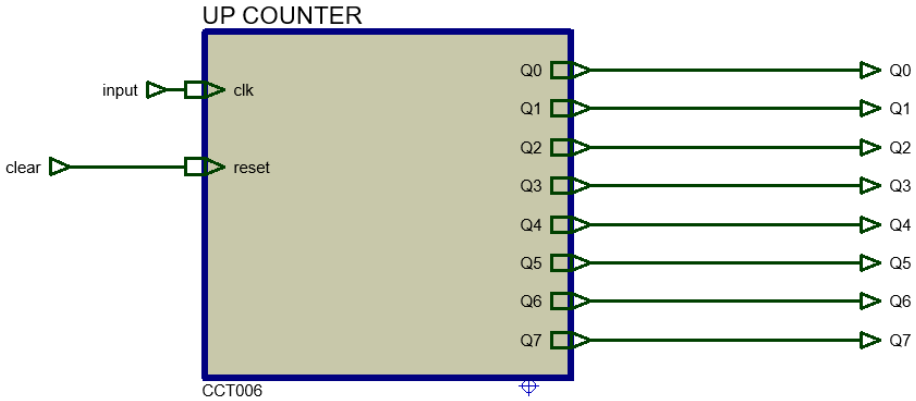


Figure: Child Sheet of the Total Vote Counter

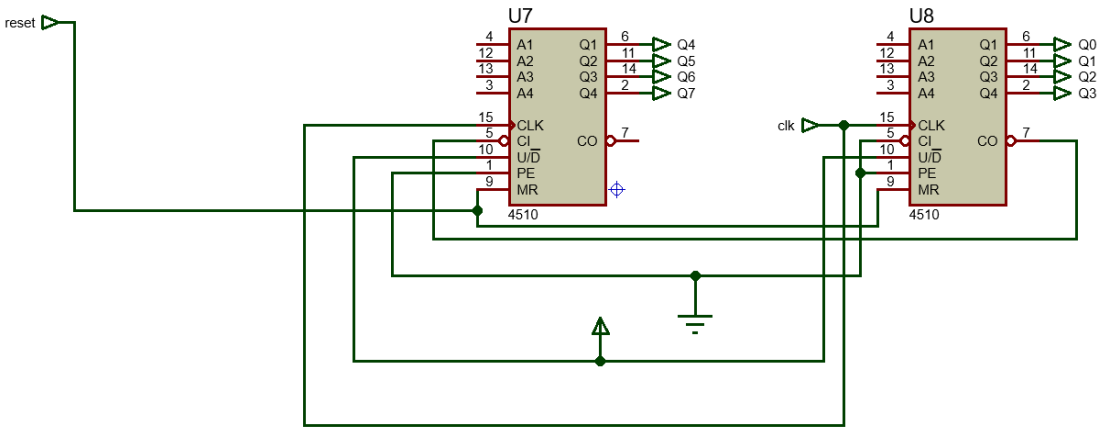


Figure: Child Sheet of the Up Counter

2. Individual Vote Counter: As the name suggests, the individual vote counter counts the votes of individual participants in the electoral system. Each of these counters contains the child sheet of the total vote counter same as the EVM. That is, each of them contains a 0-60 Up counter. All 6 of these have the same architecture. So, only one is shown as reference.

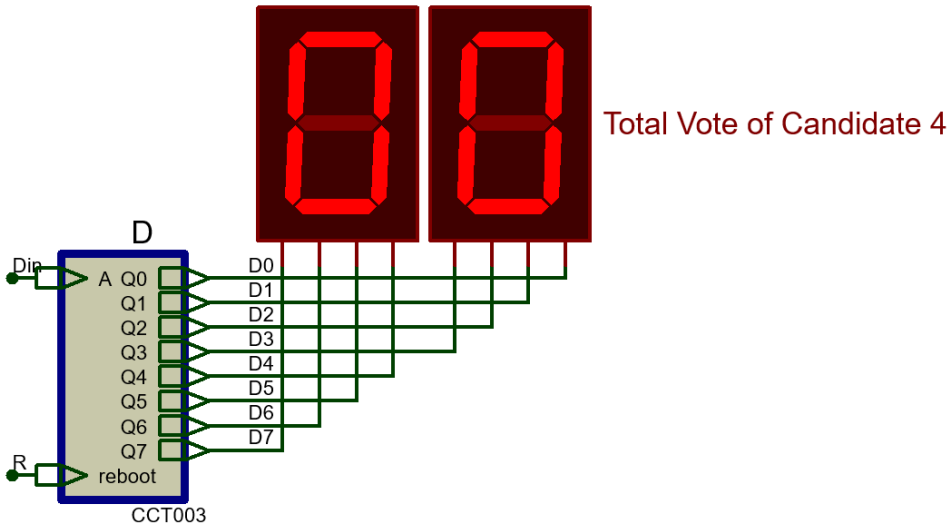


Figure: Individual Vote Counter for Candidate 4

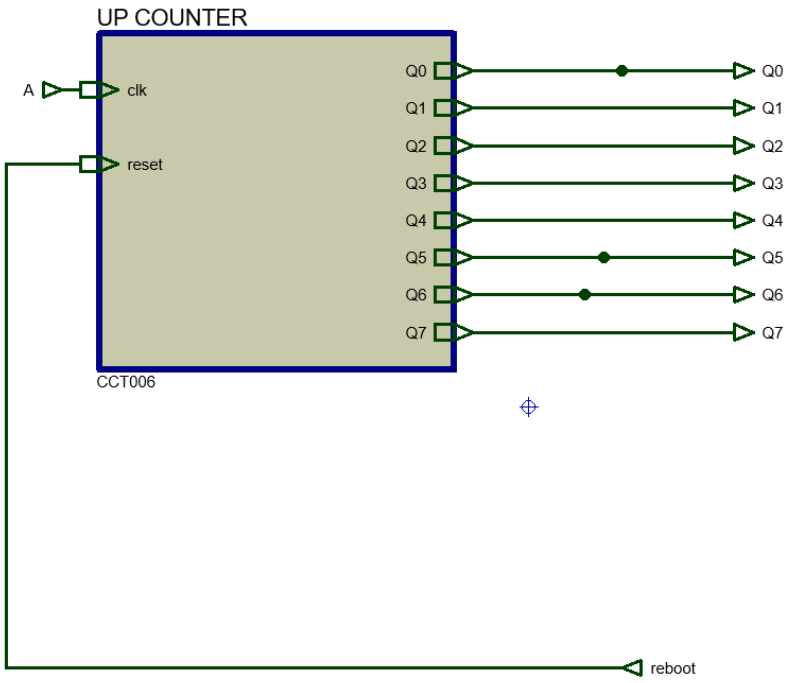


Figure: Child Sheet for Individual Vote Counter for Candidate 4

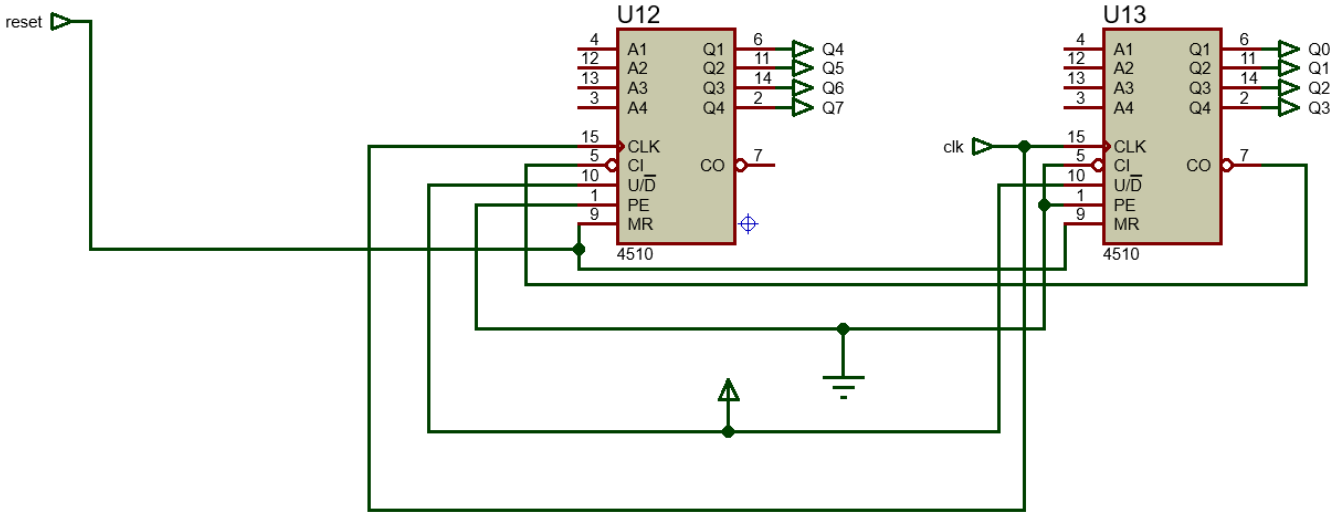


Figure: Child Sheet for the UP Counter for Candidate 4

3. Comparator: The comparator sub circuit compares the votes that the individual members got. The circuits in child sheet compares the number of votes that each and every member got and displays the winner candidate on the output display. The candidate getting the highest number of votes will be the Chairman, the second highest will be the Vice Chairman and the third highest will be the Secretary.

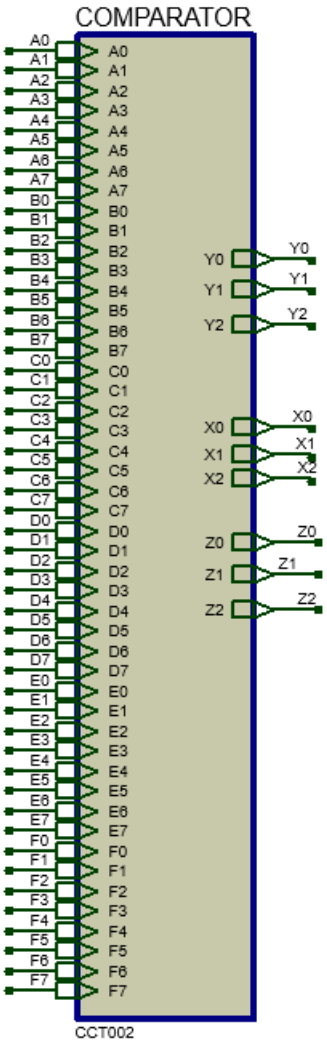


Figure: Main Comparator Subcircuit

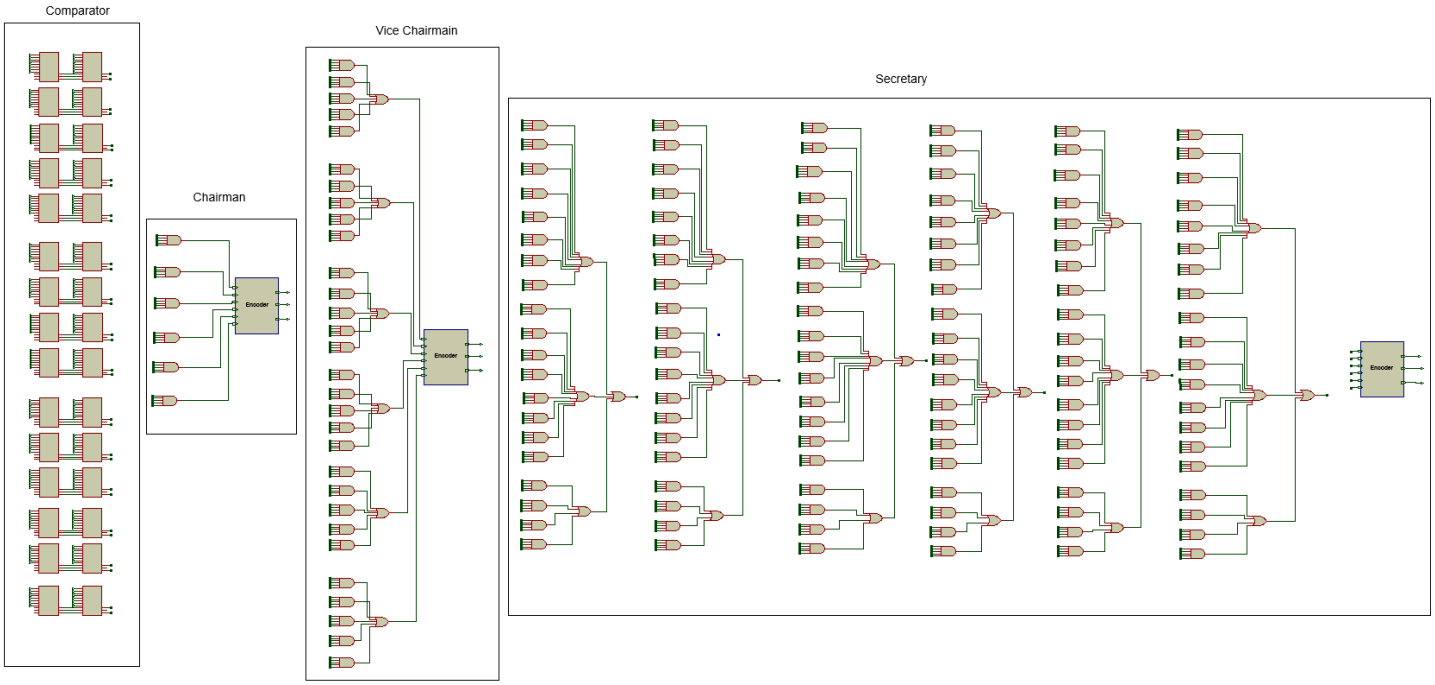


Figure: Child Sheet of the Main Comparator

Here, all the votes are compared for the three positions, Chairman, Vice Chairman and the Secretary. Different parts of this child sheet are given below:

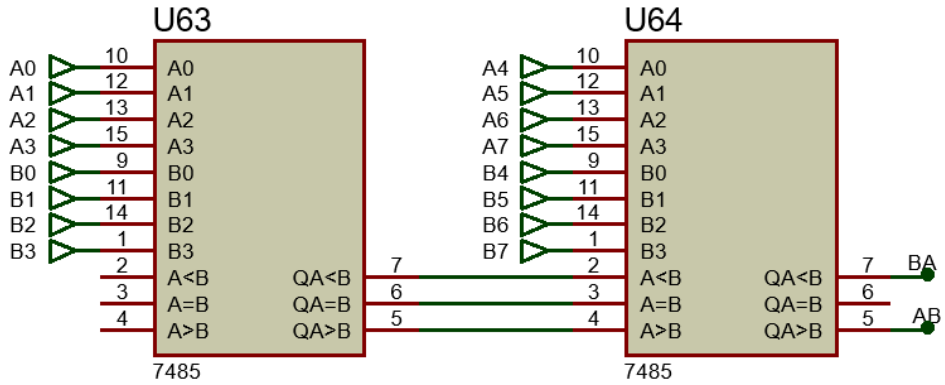


Figure: Cascaded Comparators (15 Sets for different combinations)

Two 4-bit magnitude comparator are cascaded together in order to make an 8-bit comparator. This circuit is repeated 15 times for 15 different combinations and possibilities. The final results of the voting system is processed in this part of the circuit.

In Case of the Chairman:

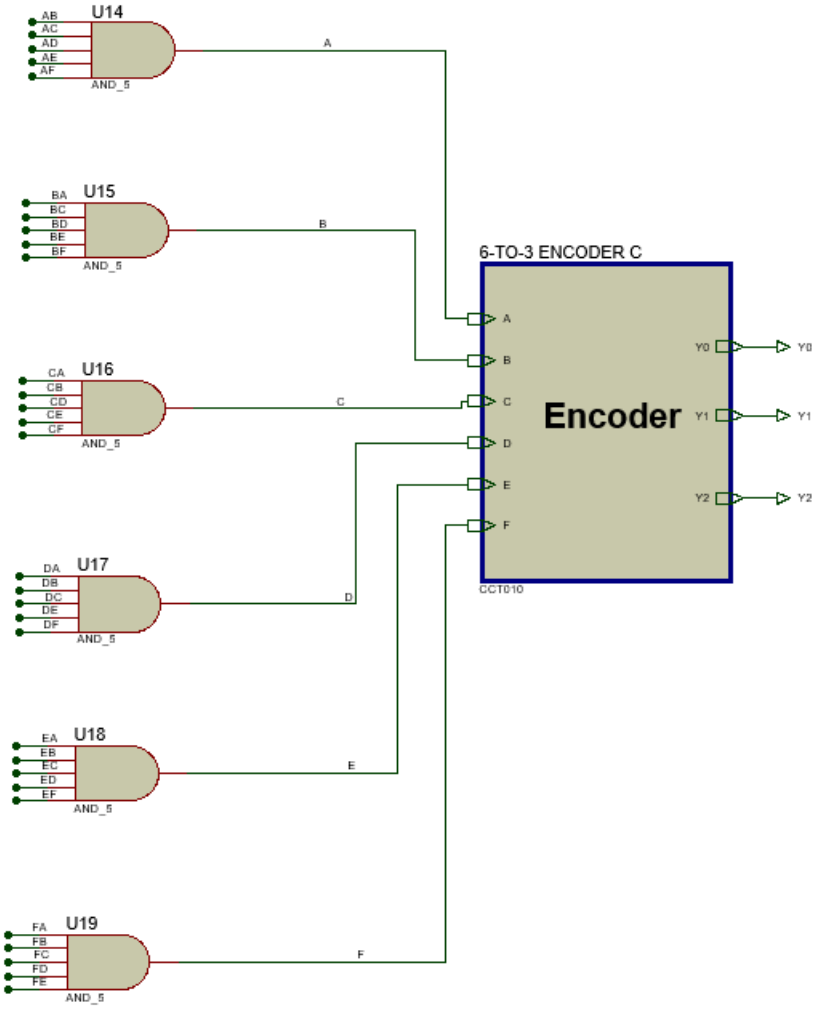


Figure: Logic Circuit for Determining the Chairman

In case of the Vice Chairman:

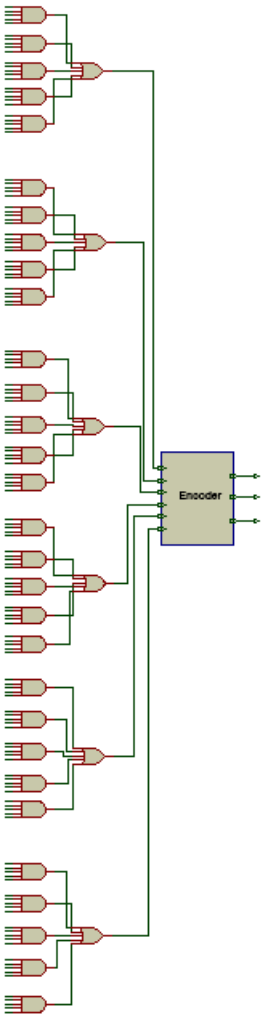
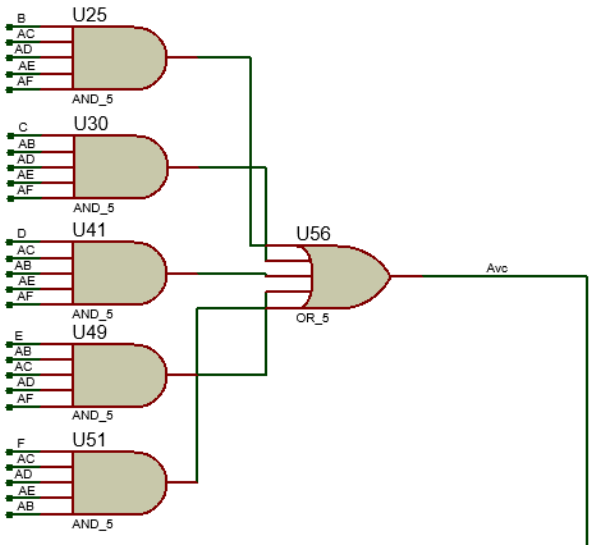


Figure: Logic Circuit for Determining the Vice Chairman



This circuit combination is repeated six times in the circuit and connected to each of the inputs of the Encoder

In Case of The Secretary:

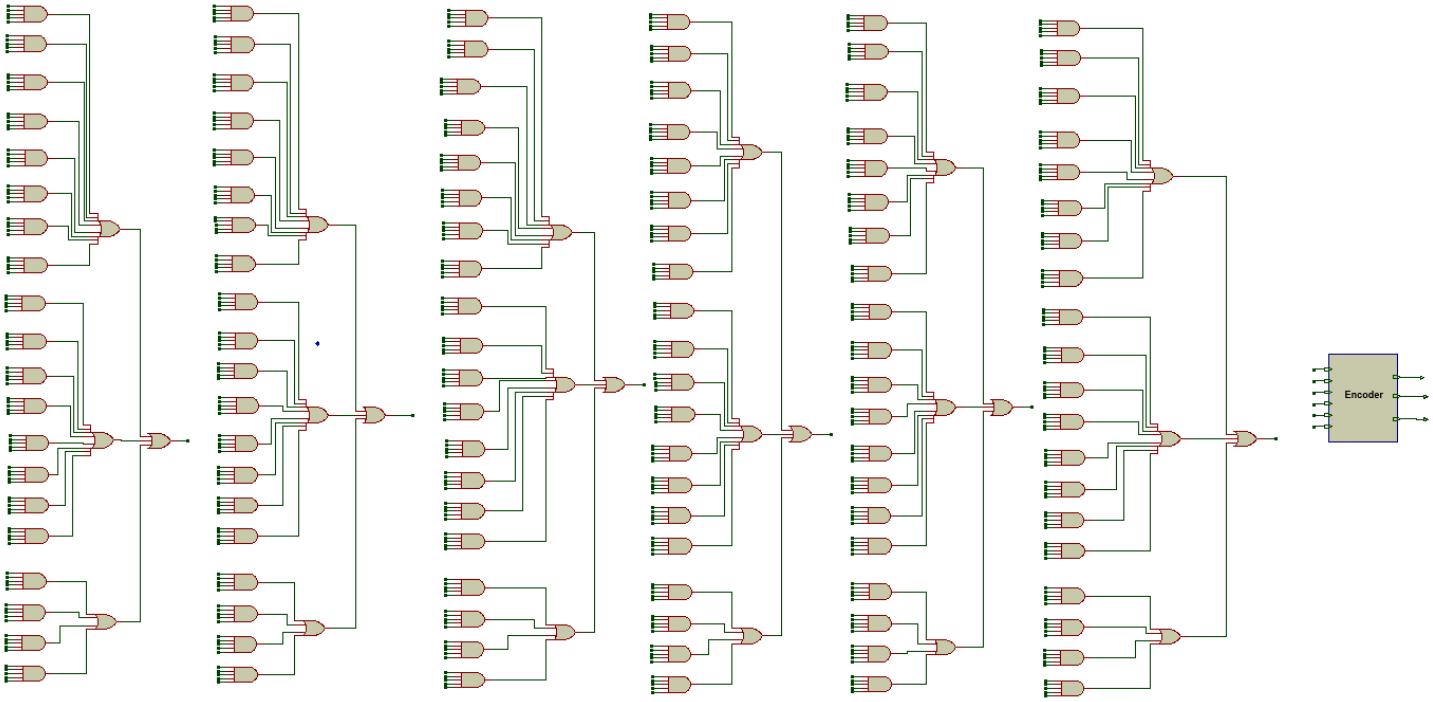
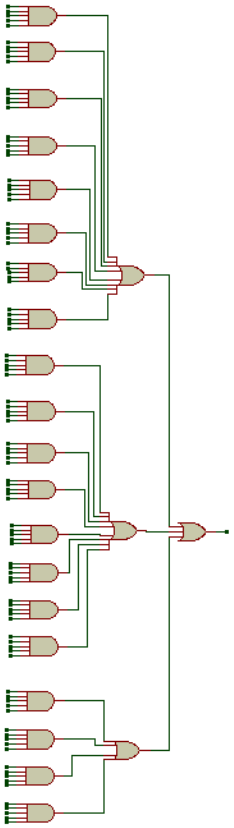


Figure: Logic Circuit for Determining the Secretary



This circuit combination is repeated six times in the circuit and connected to each of the inputs of the Encoder

The Encoder used in all the three cases have similar design. So, only one is shown as reference.

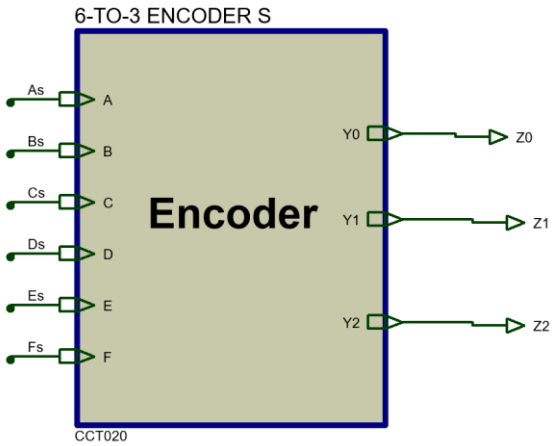


Figure: 6 to 3 Encoder

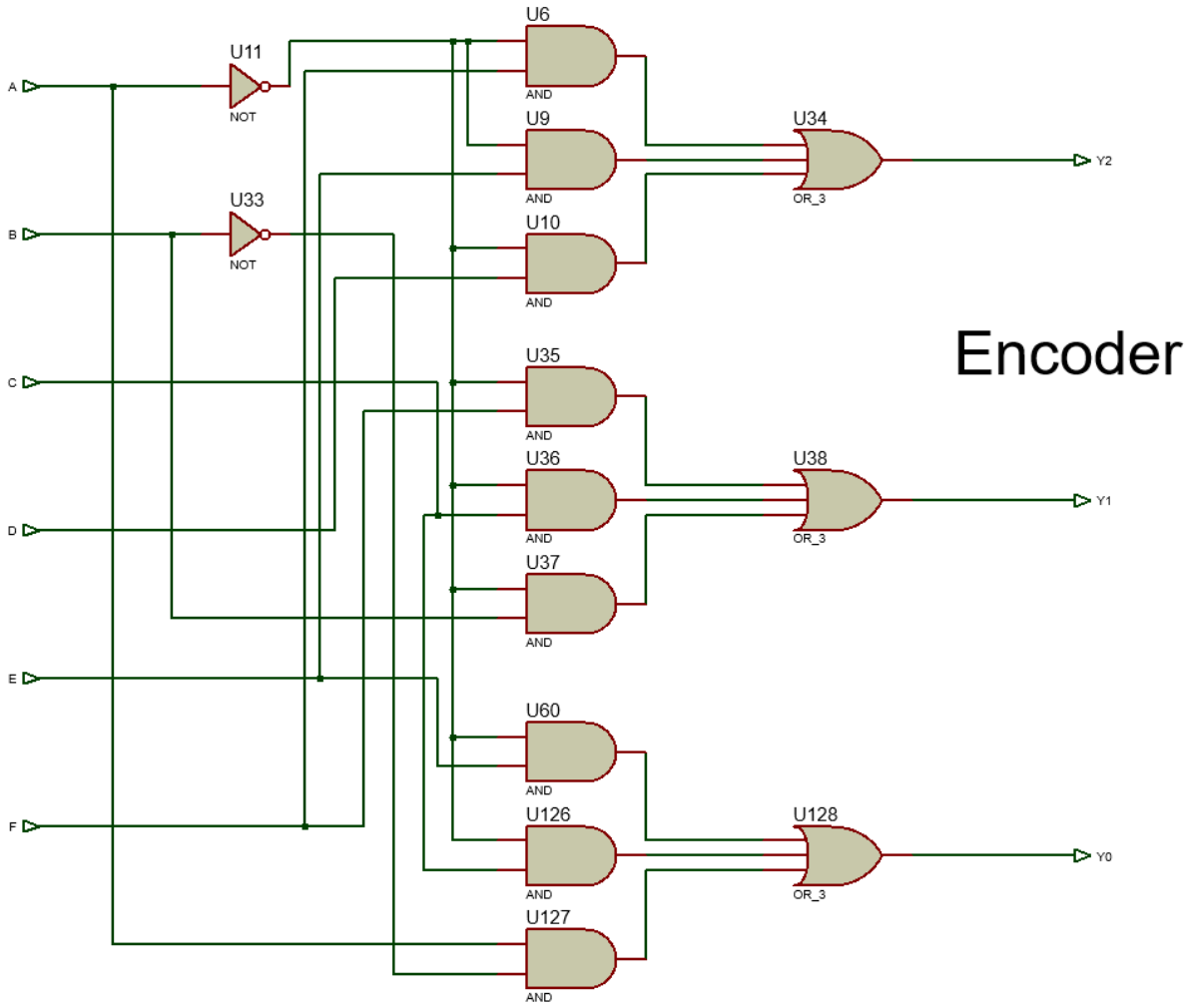


Figure: Child Sheet of the 6 to 3 Encoder.

N.B.: The outputs of the encoders are connected to the 7 segment display of the winner board.

Truth Table of the 6 to 3 Encoder:

Input						Output		
F	E	D	C	B	A	X_2	X_1	X_0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1
0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	1	1	1
0	0	1	0	0	0	1	0	0
0	1	0	0	0	0	1	0	1
1	0	0	0	0	0	1	1	0
1	1	1	1	1	1	0	0	0

KMAP for X_2:

Map

	$\bar{D}.\bar{E}.F$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$\bar{D}.E.\bar{F}$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.F$	$D.E.\bar{F}$
$\bar{A}.\bar{B}.\bar{C}$	0	1	x	1	1	x	x	x
$\bar{A}.\bar{B}.C$	0	x	x	x	x	x	x	x
$\bar{A}.B.C$	x	x	x	x	x	x	x	x
$\bar{A}.B.\bar{C}$	0	x	x	x	x	x	x	x
$A.\bar{B}.\bar{C}$	0	x	x	x	x	x	x	x
$A.\bar{B}.C$	x	x	x	x	x	x	x	x
$A.B.C$	x	x	x	x	x	x	0	x
$A.B.\bar{C}$	x	x	x	x	x	x	x	x

Map Layout

	$\bar{D}.\bar{E}.\bar{F}$	$\bar{D}.\bar{E}.F$	$\bar{D}.E.F$	$\bar{D}.E.\bar{F}$	$D.\bar{E}.\bar{F}$	$D.\bar{E}.F$	$D.E.F$	$D.E.\bar{F}$
$\bar{A}.\bar{B}.\bar{C}$	0	1	3	2	4	5	7	6
$\bar{A}.\bar{B}.C$	8	9	11	10	12	13	15	14
$\bar{A}.B.C$	24	25	27	26	28	29	31	30
$\bar{A}.B.\bar{C}$	16	17	19	18	20	21	23	22
$A.\bar{B}.\bar{C}$	32	33	35	34	36	37	39	38
$A.\bar{B}.C$	40	41	43	42	44	45	47	46
$A.B.C$	56	57	59	58	60	61	63	62
$A.B.\bar{C}$	48	49	51	50	52	53	55	54

Groups

(1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31)	$\bar{A}.F$
(2,3,6,7,10,11,14,15,18,19,22,23,26,27,30,31)	$\bar{A}.E$
(4,5,6,7,12,13,14,15,20,21,22,23,28,29,30,31)	$\bar{A}.D$

$$X_2 = \bar{A}F + \bar{A}E + \bar{A}D$$

KMAP for X_1:

Map

	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}E\bar{F}$	$\bar{D}EF$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$	DEF
$\bar{A}\bar{B}\bar{C}$	0	1	x	0	0	x	x	x
$\bar{A}\bar{B}C$	1	x	x	x	x	x	x	x
$\bar{A}B\bar{C}$	x	x	x	x	x	x	x	x
$\bar{A}BC$	1	x	x	x	x	x	x	x
$A\bar{B}\bar{C}$	0	x	x	x	x	x	x	x
$A\bar{B}C$	x	x	x	x	x	x	x	x
$AB\bar{C}$	x	x	x	x	x	x	0	x
ABC	x	x	x	x	x	x	x	x

Map Layout

	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}E\bar{F}$	$\bar{D}EF$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$	DEF
$\bar{A}\bar{B}\bar{C}$	0	1	3	2	4	5	7	6
$\bar{A}\bar{B}C$	8	9	11	10	12	13	15	14
$\bar{A}B\bar{C}$	24	25	27	26	28	29	31	30
$\bar{A}BC$	16	17	19	18	20	21	23	22
$A\bar{B}\bar{C}$	32	33	35	34	36	37	39	38
$A\bar{B}C$	40	41	43	42	44	45	47	46
$AB\bar{C}$	56	57	59	58	60	61	63	62
ABC	48	49	51	50	52	53	55	54

Groups

(1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31)	$\bar{A}F$
(8,9,10,11,12,13,14,15,24,25,26,27,28,29,30,31)	$\bar{A}C$
(16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31)	$\bar{A}B$

$$X_2 = \bar{A}F + \bar{A}C + \bar{A}B$$

KMAP for X_0:

Map

	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}E\bar{F}$	$\bar{D}EF$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$	DEF
$\bar{A}\bar{B}\bar{C}$	0	0	x	1	0	x	x	x
$\bar{A}\bar{B}C$	1	x	x	x	x	x	x	x
$\bar{A}B\bar{C}$	x	x	x	x	x	x	x	x
$\bar{A}BC$	0	x	x	x	x	x	x	x
$A\bar{B}\bar{C}$	1	x	x	x	x	x	x	x
$A\bar{B}C$	x	x	x	x	x	x	x	x
$AB\bar{C}$	x	x	x	x	x	x	0	x
ABC	x	x	x	x	x	x	x	x

Map Layout

	$\bar{D}\bar{E}\bar{F}$	$\bar{D}\bar{E}F$	$\bar{D}E\bar{F}$	$\bar{D}EF$	$D\bar{E}\bar{F}$	$D\bar{E}F$	$DE\bar{F}$	DEF
$\bar{A}\bar{B}\bar{C}$	0	1	3	2	4	5	7	6
$\bar{A}\bar{B}C$	8	9	11	10	12	13	15	14
$\bar{A}B\bar{C}$	24	25	27	26	28	29	31	30
$\bar{A}BC$	16	17	19	18	20	21	23	22
$A\bar{B}\bar{C}$	32	33	35	34	36	37	39	38
$A\bar{B}C$	40	41	43	42	44	45	47	46
$AB\bar{C}$	56	57	59	58	60	61	63	62
ABC	48	49	51	50	52	53	55	54

Groups

(2,3,6,7,10,11,14,15,18,19,22,23,26,27,30,31)	$\bar{A}E$
(8,9,10,11,12,13,14,15,24,25,26,27,28,29,30,31)	$\bar{A}C$
(32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47)	$A\bar{B}$

$$X_0 = \bar{A}E + \bar{A}C + A\bar{B}$$

4. 7-Segment Displays: Multiple 7-segment displays are employed to visually represent the results, displaying the names of the elected candidates for each position.

Figure: Two 7 Segment Displays to Show the Total No. of Votes Casted

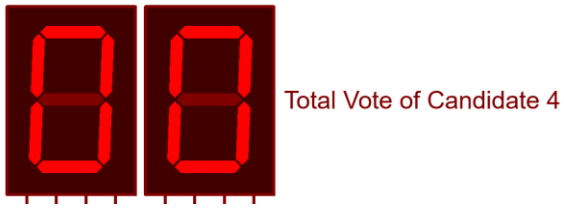


Figure: Two 7 Segment Displays to Show the Total No. of Votes for Candidate 4

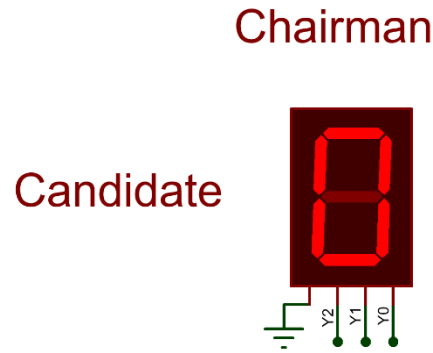


Figure: 7 segment Display to Show the Winning Candidate Number

Truth Table for 7 Segment BCD Display:

BCD Signal				Display	BCD Signal				Display
D	C	B	A		D	C	B	A	
0	0	0	0	0	0	1	0	1	5
0	0	0	1	1	0	1	1	0	6
0	0	1	0	2	0	1	1	1	7
0	0	1	1	3	1	0	0	0	8
0	1	0	0	4	1	0	0	1	9

0 = logic low 1 = logic high

2. Methods of Research

The research methods primarily used by us during various stages of this project were a combination of primary and secondary research. We first collected relevant information regarding ‘Electronic Voting System’ from various articles, research papers, websites and YouTube videos. The research involves a combination of literature review and practical experimentation. Relevant studies on electronic voting systems, sensor technologies, and election automation are reviewed to inform the design and development of the proposed system. After that, different components of our simulated circuit went through various trail and errors before settling to our final circuit.

3. Methods of Data Collection

The Data collection involves the voting preferences of 60 members. Binary data is collected for each participant's choice for chairman, vice chairman, and secretary positions. A mod-256 counter is used for taking the votes of the 60 voters.

4. Methods of Analysis

4.1 Data Preparation

Raw data collected by the Logic Toggles and switches is processed and formatted for input into the Proteus-based monitoring system.

4.2 Software Used

Proteus is employed as the primary software for designing, simulating, and testing the Electronic Voting System. The software allows for a virtual representation of the system’s components and functionalities.

5.3 Statistical Methods

We used basic arithmetic operations and tally in order to calculate total votes and determine winners based on the majority.

5. Evaluate and Justify Methodological Choices

5.1 Why This Methods?

The chosen approach in our opinion is the most suitable as it aligns with the project's objectives, leveraging well-established principles of logic design and electronic systems. The simplicity of the methodology ensures a practical and effective solution for the company's voting requirements.

5.2 Strengths and Weaknesses

Strengths:

- Logical and straightforward approach for the given problem.
- Efficient use of resources without unnecessary complexity.
- Can take up to 256 votes by changing the inputs of the AND gate in the counter.

Weaknesses:

- Limited application beyond the specific context of majority voting in this organizational setting.
- Use of a lot of logic gates which might result in delays.

6. Obstacles and Debugging Techniques

The main obstacle that we faced during the project was while trying to display the winners for the position of Vice-Chairman and Secretary. We designed the circuit and implemented all the logics accordingly, but output was experiencing delay. This was because of using a lot of logc gates in the circuit.

So, in order to tackle this situation, we used counter ICs instead of designing them using flipflops and logic gates.

Results: After casting all the votes, the winners and the number of votes will be displayed in the following manner:

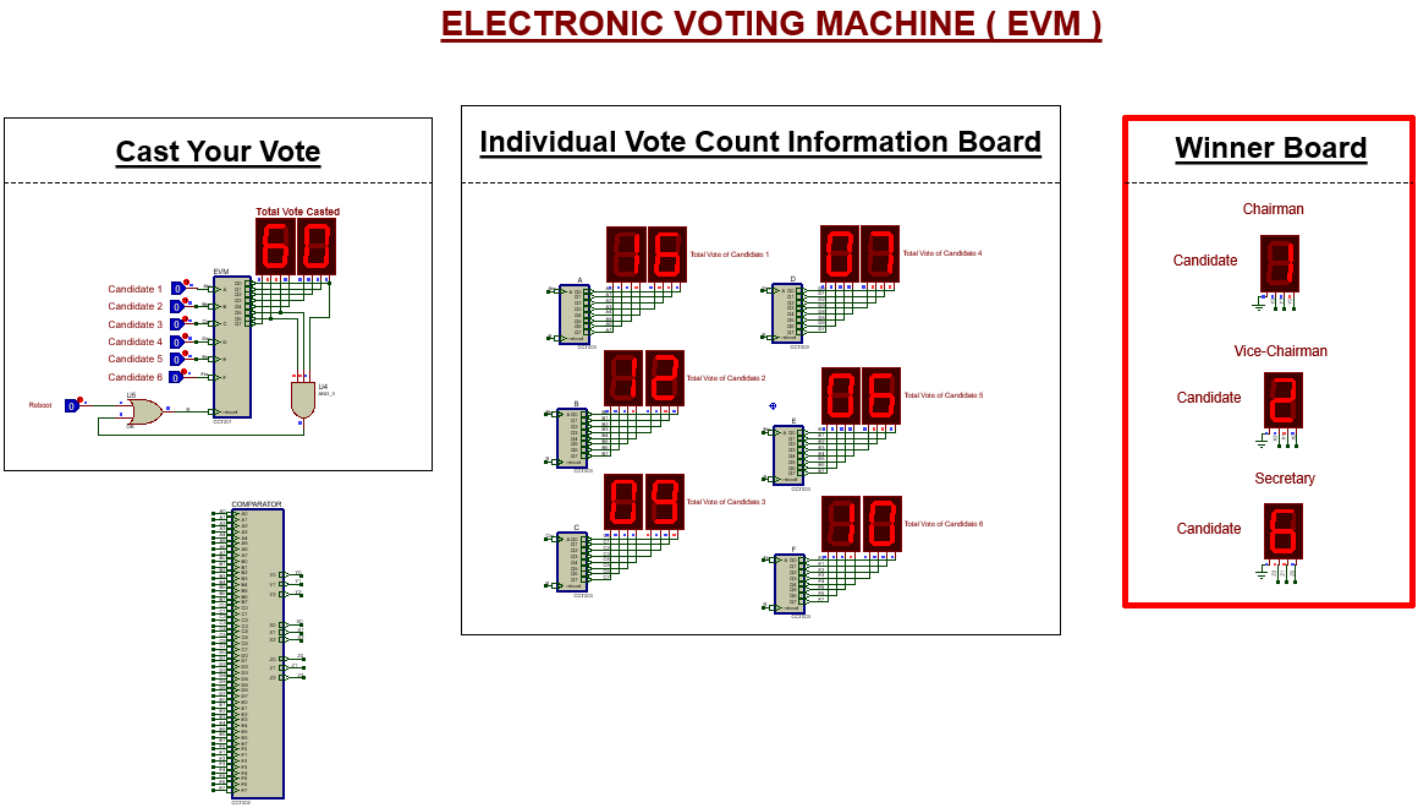


Figure: The Complete Voting System

Here, we take votes from the Voting Machine in the Cast Your Vote sections via the logic toggles. Each Candidate has one logic toggle and the voters will cast their votes clicking on one of them. There is a system to Reboot the whole system in case of any unfair or unexpected situations.

In the given condition, Candidate 1 got the highest number of votes (16) followed by Candidate 2 (12) and Candidate 6 (10). So, Candidate 1 is shown as the Chairman, Candidate 2 as the Vice-Chairman and Candidate 6 as the secretary.

The system will automatically reset after 60 votes are casted. So, if anyone tries to pursue any sorts of unfair means in the election, or cast more than one vote, the system will reset after all the voters cast their votes.

But there could be another condition. If any of the two members have the same number of votes, so according to most of the electoral systems, there has to be a revote. So, if our designed system faces a situation like this, where 2 or more candidates have the same number of votes, the system would not display the result.

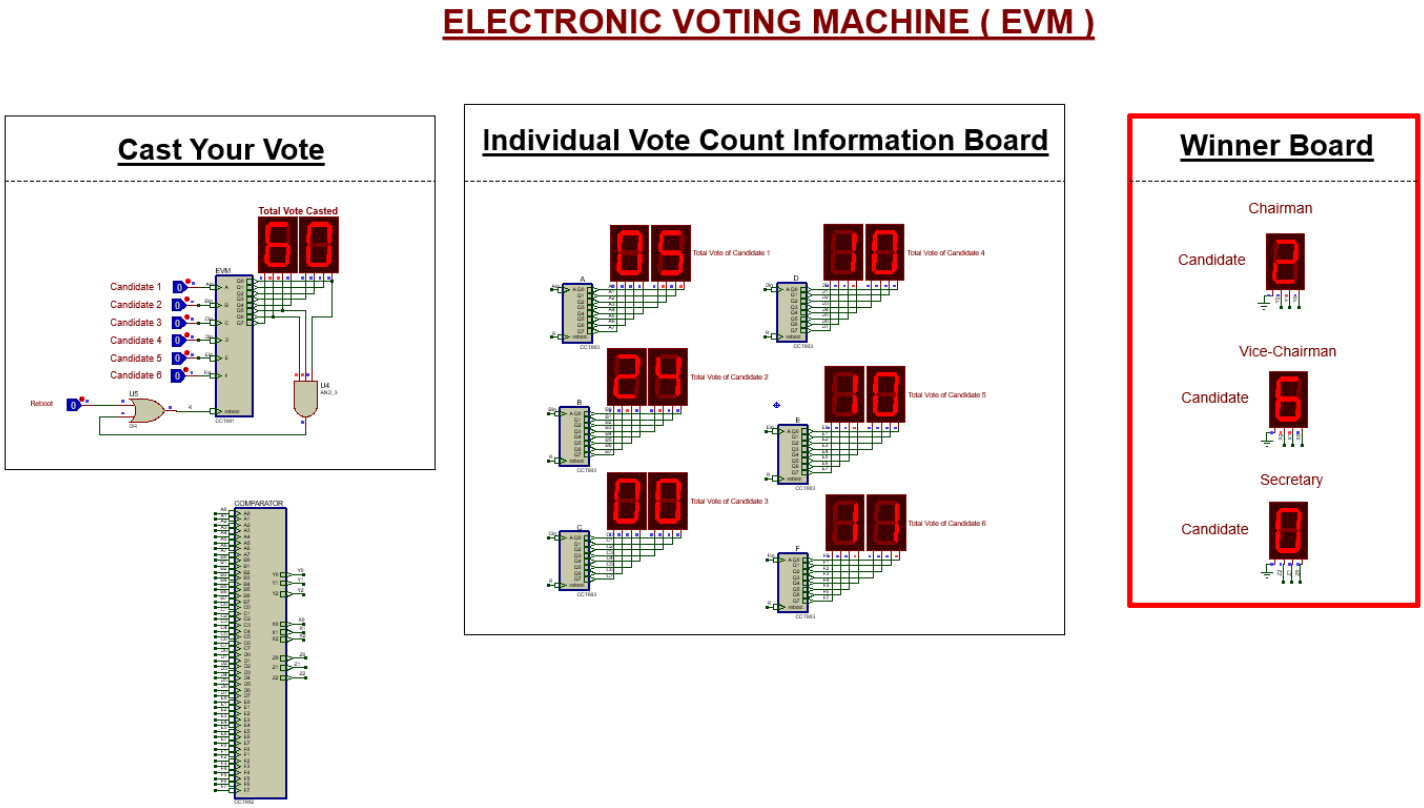


Figure: Same Number of Vote Condition

Here, we can see that, the 3rd highest number of votes is 10 and both Candidate 4 and Candidate 5 have 10 votes. That is why, the display for declaring the Winner of secretary is displaying candidate 0.

So, we can conclude saying that, our designed circuit is fulfilling the requirements of the given problem statement.

Discussion: To achieve the mentioned objectives, the project involved the implementation of various electronic circuits, including logic gates for processing votes, synchronous circuits for coordinated operations, combinational circuits for logical decision-making, and arithmetic

circuits for vote counting. The use of 7-segment displays will enhance the user experience by providing a clear and concise visual representation of the election results.

The development of such a system demands careful consideration of security measures to prevent unauthorized access and tampering. Implementing reboot option for the election organizers will contribute to the overall integrity of the voting process.

In conclusion, this project not only addresses the technical aspects of creating an electronic voting system but also emphasizes the importance of fairness, transparency, and security in the democratic process. The successful implementation of this system may pave the way for more advanced and secure electronic voting systems in various domains, contributing to the evolution of democratic practices.

Impact: The designed project can have significant impacts in the context of Bangladesh and fair elections as a whole:

1. **Enhancing Transparency and Trust:** The system can enhance transparency and trust in the election process. By displaying the number of votes for each candidate and the winners, it provides clear and immediate results, reducing the chances of disputes (*What Is Electronic Voting and Its Advantages?*, 2019).
2. **Ensuring Fairness:** The system ensures a fair election process by allowing only the majority vote to win. This can prevent manipulation and ensure that the elected officials truly represent the majority of the voters (*Free and Fair Elections: Definition, 8 Standards to Meet*, 2021).
3. **Improving Efficiency:** The use of a 7-segment display to show the winners can improve the efficiency of the election process. It eliminates the need for manual counting, which can be time-consuming and prone to errors (Peralta, n.d.).
4. **Potential for Wider Application:** Electronic voting machines (EVMs) were introduced in Bangladesh to resolve problems of using paper ballots. They were first successfully used in 2007 for the election of the working committee of Dhaka Officers' Club (*Electronic Voting in Bangladesh*, n.d.). While this system is designed for a company election, it has the potential to be applied to larger scales, such as local or national elections in Bangladesh. This could contribute to the overall improvement of the electoral system in the country.
5. **Encouraging Technological Advancement:** The development and implementation of such a system can encourage technological advancement and innovation in Bangladesh. The development and implementation of such a system can encourage technological advancement and innovation in Bangladesh. It can inspire more initiatives to leverage technology for societal benefits (Rahman, 2022).

In the context of fair elections globally, this project can serve as a model for other countries or organizations seeking to improve their voting systems. It demonstrates how technology can be used to ensure a transparent, fair, and efficient election process. However, it's important to note that while technology can enhance the election process, it's also crucial to address other aspects

such as voter education, legal framework, and safeguards against potential technological failures or cyber threats (*Free and Fair Elections — Principles of Democracy*, n.d.).

Conclusion and Future Works: So, to conclude, this project has not only provided a practical solution for electing the 2023 Executive body of the company but also demonstrated how technology can be leveraged to enhance transparency, fairness, and efficiency in elections. It has shown the potential of electronic voting systems in improving the electoral process, not just within the company, but potentially on a larger scale.

Moving forward, there are several areas that could be explored to further improve this system and our group will try to work on it as we know more and more about EEE and electronics as a whole. Some of our future ideas are mentioned here:

1. **Security Measures:** While the current system ensures a fair election process just using a reboot button, our future work will focus on enhancing the security measures to protect against potential cyber threats.
2. **Scalability:** The system could be tested and modified for larger elections with more voters and candidates.
3. **User Interface:** The user interface will be improved to make it more user-friendly and accessible to all voters.
4. **Integration with Other Systems:** The system could be integrated with other systems (like voter registration databases) to streamline the entire electoral process.

By addressing these areas, the Electronic Voting System could be further refined and potentially serve as a model for fair and efficient elections in other contexts.

References:

Alamgir, M. (2023, November 16). Bangladesh parliamentary elections on January 7, 2024 | Next nat'l election on Jan 7. *The Daily Star*. https://www.thedailystar.net/news/bangladesh/elections/news/next-natl-election-jan-7-3470736

Electronic voting in Bangladesh. (n.d.). Wikipedia. Retrieved December 16, 2023, from https://en.wikipedia.org/wiki/Electronic_voting_in_Bangladesh

The Evolution of Voting Technology in America: From Paper to Pixels. (2023, November 5). LinkedIn. Retrieved December 8, 2023, from https://www.linkedin.com/pulse/evolution-voting-technology-america-from-paper-pixels-dale-gibler-tbpsc

Free and fair elections: definition, 8 standards to meet. (2021, July 8). Civil Liberties Union for Europe. Retrieved December 16, 2023, from https://www.liberties.eu/en/stories/free-and-fair-elections/43642

Free and Fair Elections — Principles of Democracy. (n.d.). Principles of Democracy. Retrieved December 16, 2023, from https://www.principlesofdemocracy.org/election-dem

Online/Automated Elections in the Philippines - Iskomunidad. (2011, August 11). Iskomunidad. Retrieved December 8, 2023, from https://iskomunidad.upd.edu.ph/index.php/Online/Automated_Elections_in_the_Philippines

Peralta, R. (n.d.). *Electronic voting | Benefits, Challenges & Security*. Britannica. Retrieved December 16, 2023, from https://www.britannica.com/topic/electronic-voting

Rahman, S. (2022, January 31). *Blockchain based "online voting system" for free, fair election.* The Daily Star. Retrieved December 16, 2023, from https://www.thedailystar.net/news/bangladesh/elections/news/blockchain-based-online-voting-system-free-fair-election-2951221

Supporting Free and Fair Elections | Democracy, Human Rights & Governance | U.S. Agency for International Development. (n.d.). USAID. Retrieved December 16, 2023, from https://www.usaid.gov/democracy/supporting-free-and-fair-elections

What is Electronic Voting and its Advantages? (2019, September 27). Smartmatic. Retrieved December 16, 2023, from https://elections.smartmatic.com/electronic-voting-advantages/

Proteus Files

https://drive.google.com/drive/folders/1tZqIhqn8Df3Dlm40LclOrFvSiGNOpNP6?usp=drive_link