FD-JL-PCB-MB

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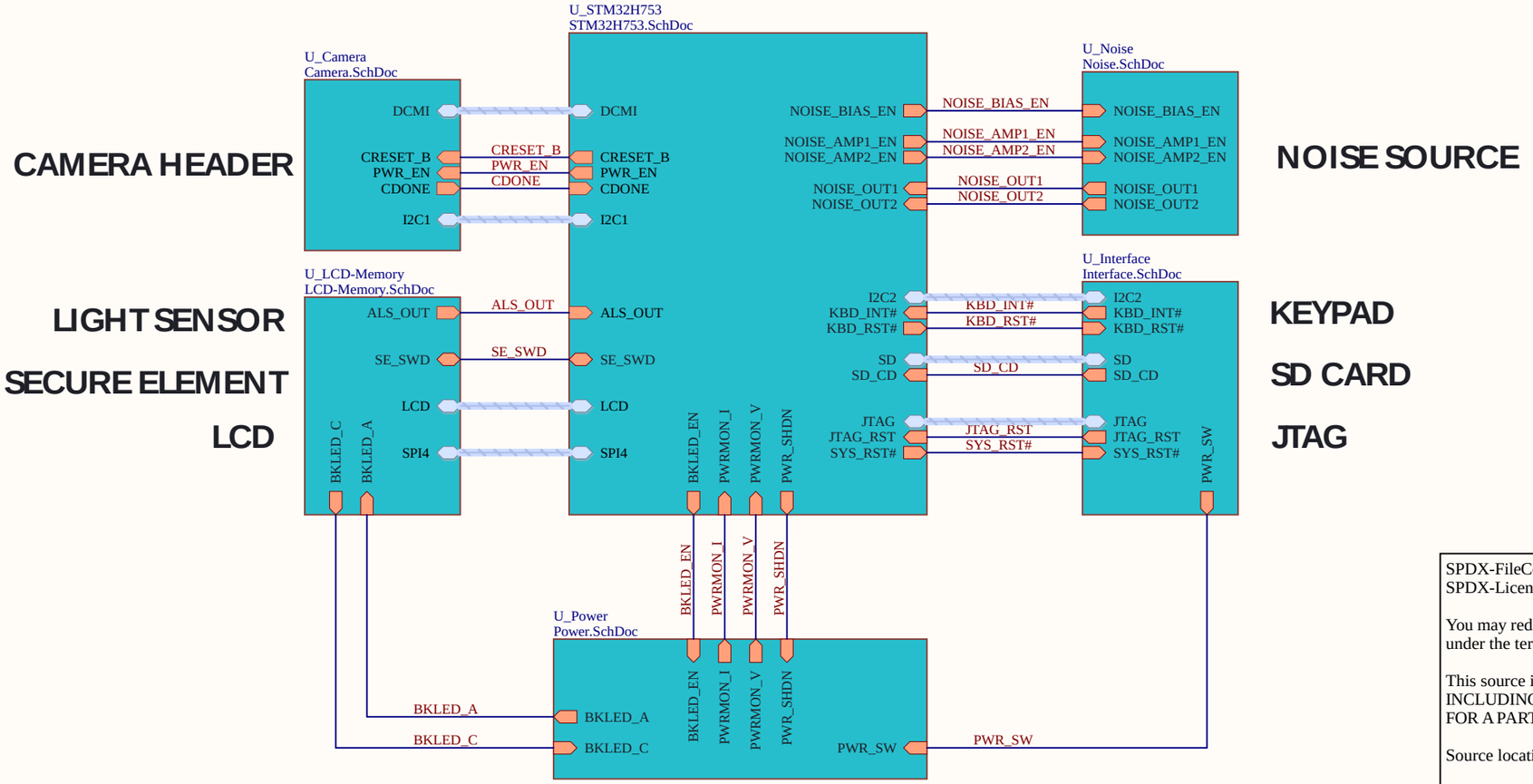
Revisions

Rev	Description	Date	Approved
C1	Release for Production	11/09/2020	M. Beach

STM32H753



PCB1 C1

PCB

FD-JL-PCB-MB

LICENCE: CERN-OHL-S v2

Engineer: M. Beach	FOUNDATION	Foundation Devices Inc 6 Liberty Sq #6018 Boston, MA 02109
Designer: M. Beach	Drawing Title: FD-JUL-MB.PrjPcb	
Approved: M. Beach Date: 11/09/2020	Page Title: Title.SchDoc	
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STM32H753

Supply Supervisor

U3 TPS3840DL27DBVR

Design Note:
tD = 618937 * CCT_EXT + 50 µs
tD = 618937 * 1.5E-9F + 50us
tD = 0.978 ms

Fiducials

FID1 FID1X2R · FID2 FID1X2R · FID3 FID1X2R
FID4 FID1X2R · FID5 FID1X2R · FID6 FID1X2R

Mounting Holes

ST1 TH-D2_45 · ST2 TH-D2_45

Decap

C5 100nF · C6 100nF · C7 100nF · C8 100nF · C9 100nF · C10 100nF · C11 100nF · C12 100nF

Design Note:
Stabalization for main regulator

C13 2.2uF · C58 2.2uF

U2 STM32H753VIT6

VCC: VDD ×5, VDDA, VREF+, VBAT
Reset: RST
Boot Mode: BOOT0
JTAG: PB3 (JTDO/TRACESWO), PA13 (JTMS-SWDIO), PA14 (JTCK- SWCLK), PB4 (NJTRST)
OSC: PC14-OSC32 IN, PC15-OSC32 OUT, PH0-OSC IN, PH1-OSC OUT
USB: PA9/OTG_FS_VBUS, PA11/OTG_FS_DM, PA12/OTG_FS_DP, PA10/OTG_FS_ID
SDMMC: PC8/SDMMC1_D0, PC9/SDMMC1_D1, PC10/SDMMC1_D2, PC11/SDMMC1_D3, PC12/SDMMC1_CK, PD2/SDMMC1_CMD
VSS: VSSA, VSS ×5
MISC: PB2/RTC_OUT, PC13, PD0/UART4_RX, PD1/UART4_TX, PD4, PD5, PD6, PD7, PD8/USART3_TX, PD9/USART3_RX, PD10, PD14, PD15, PE2, PE3, PE7, PE8, PE9, PE10, PE15
TIMx: PA8/TIM1_CH1, PB0/TIM8_CH2N, PB1/TIM3_CH4, PB8/TIM4_CH3
ADC: PC0/ADC123_INP10, PC1/ADC123_INP11, PC2_C/ADC3_INP0, PC3_C/ADC3_INP1, PC4/ADC12_INP4, PC5/ADC12_INP8
USART: PA0/UART4_TX/USART2_CTS, PA1/USART2_RTS, PA2/USART2_TX, PA3/USART2_RX
SPI: PA5/SPI1_SCK, PA7/SPI1_MOSI, PA15/SPI1_NSS (JTDI), PB13/SPI2_SCK, PB14/SPI2_MISO, PB15/SPI2_MOSI, PE11/SPI4_NSS, PE12/SPI4_SCK, PE13/SPI4_MISO, PE14/SPI4_MOSI
I2C: PB5/I2C1_SMBA, PB6/I2C1_SCL, PB9/I2C1_SDA, PB12/I2C2_SMBA, PB10/I2C2_SCL, PB11/I2C2_SDA, PD11/I2C4_SMBA, PD12/I2C4_SCL, PD13/I2C4_SDA
DCMI: PA4/DCMI_HSYNC, PB7/DCMI_VSYNC, PA6/DCMI_PIXCLK, PC6/DCMI_D0, PC7/DCMI_D1, PE0/DCMI_D2, PE1/DCMI_D3, PE4/DCMI_D4, PD3/DCMI_D5, PE5/DCMI_D6, PE6/DCMI_D7

Board Revision

Design Note: Board Revision Ladder
Rev X1: 0V
Rev A5: 0.5V
Rev B4: 1.0V
Rev C1: 1.5V

FOUNDATION

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Interfaces

Keypad Controller

Keyboard

1[3C] I2C2 I2C SDA SCL

1[3C] KBD_INT#

1[3C] KBD_RST#

+3V0

R10 4.7k, R11 4.7k, R12 4.7k, R13 4.7k

I2C2_SDA, I2C2_SCL, KBD_INT#, KBD_RST#

+3V0

C14 100nF

GND

U4 ADP5587ACPZ-R7

21 VCC

22 SDA

23 SCL

24 INT

20 RST

25 EP

19 GND

Buttons

R0 8 KBD_K7
R1 7 KBD_K16
R2 6 KBD_K15
R3 5 KBD_K12
R4 4 KBD_K17
R5 3 KBD_K13
R6 2 KBD_K4
R7 1 KBD_K14

C0 9 KBD_K11
C1 10 KBD_K10
C2 11 KBD_K2
C3 12 KBD_K6
C4 13 KBD_K5
C5 14 KBD_K9
C6 15 KBD_K8
C7 16 KBD_K0
C8 17 KBD_K3
C9 18 KBD_K1

GND

Design Note:
Keyboard controller has internal pullups and debouncing.

Buttons

KBD_K[17..0]

KBD_K0 KBD_K1 KBD_K2 KBD_K3 — 6-SNL-170(N) SW7, SW10, SW13, SW16 — GND

KBD_K4 KBD_K5 KBD_K6 KBD_K7 — 6-SNL-170(N) SW8, SW11, SW14, SW17 — GND

KBD_K8 KBD_K9 KBD_K10 KBD_K11 — 6-SNL-170(N) SW9, SW12, SW15, SW18 — GND

KBD_K12 — 6-SNL-170(N) SW1

KBD_K17 — 6-SNL-170(N) SW2

KBD_K13 — 6-SNL-170(N) SW3

KBD_K14 — 6-SNL-170(N) SW4

KBD_K15 — 6-SNL-170(N) SW5

KBD_K16 — D1 RB751S40T1G — 6-SNL-170(N) SW6 — GND

PWR_SW 1[2B]

Micro SD Card

SD Card

1[3C] SD SD_Card: D0 D1 D2 D3 CK CMD

1[3C] SD_CD

+3V0

R16 10k, R17 10k, R18 10k, R19 10k, R20 10k, R21 10k, R22 10k

+3V0

J1 SD CARD

4 VDD
7 DAT0
8 DAT1
1 DAT2
2 CD/DAT3
5 CLK
3 CMD
6 VSS
DET
POL
GND G1
GND G2
GND G3
G5
G4

SD_D0 SD_D1 SD_D2 SD_D3 SD_CK SD_CMD

GND

0475710001

GND_EARTH_SD

SD_CD

C18 100nF

GND

C17 1nF 1kV

R24 1M 1206

GND

GND_EARTH_SD

U6 PUSB3AB4Z

U7 PUSB3AB4Z

GND

+3V0

C15 100nF, C16 4.7uF

GND

JTAG Testpoints

+3V0

R14 4.7k, R15 4.7k

JTAG

1[3B] JTAG: TDI TDO TMS TCK

JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TCK

1[3B] SYS_RST#

SYS_RST#

1[3B] JTAG_RST

JTAG_RST

+3V0

J4 'Plug of Nails' JTAG - SWD — JTAG-TC2050-IDC

1 VCC - VCC
8 TDI - NC
6 TDO - SWO
2 TMS - SWDIO
4 TCK - SWCLK
10 RESET - RESET
9 NC - nTRST
7 NC - RTCLK
5 GND/5V - GND/5V
3 GND - GND

GND

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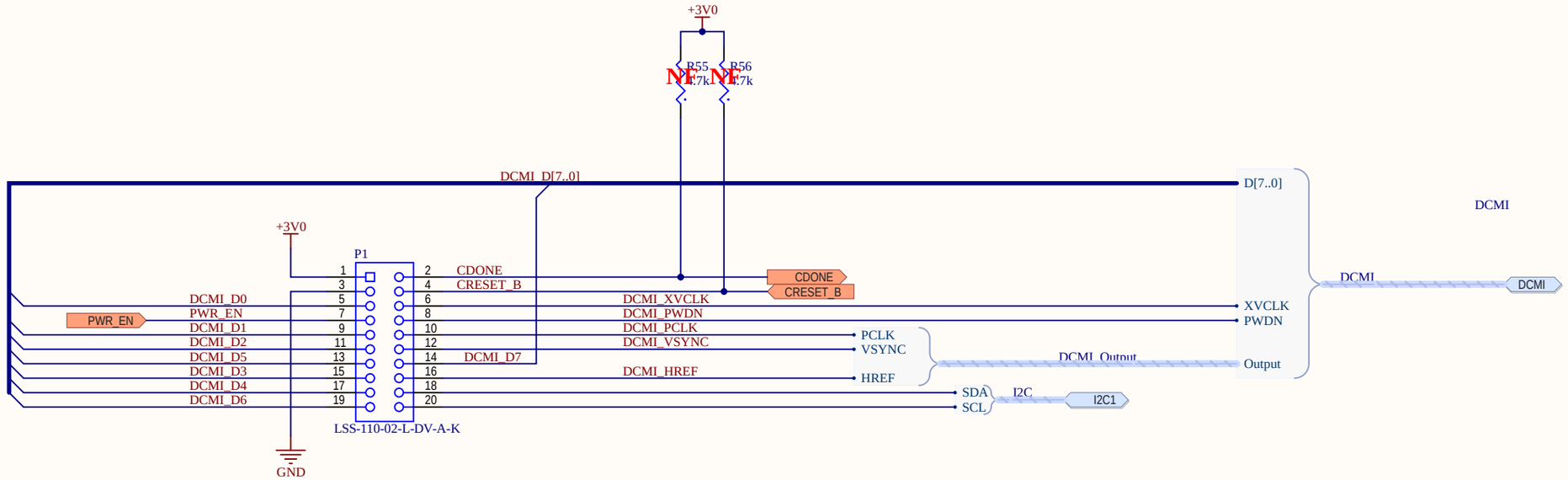
Camera Connector



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Drawing Title: FD-JUL-MB.PrjPcb			
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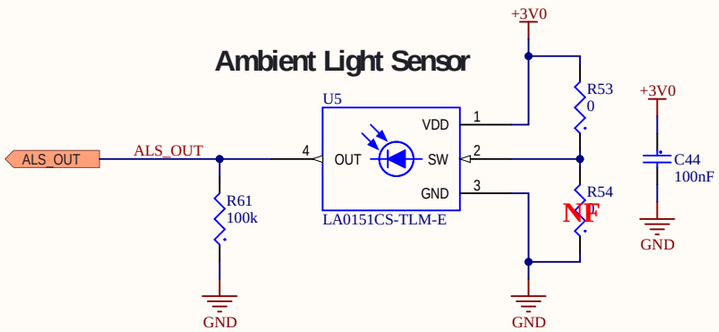
LCD, MEMORY

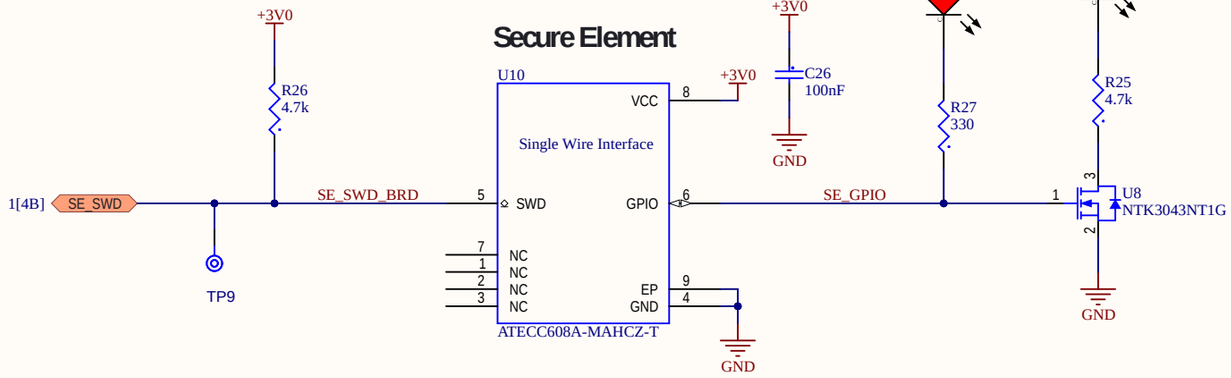
Design Note:
Signal Vih: 2.7V < Vih < 3.3V.
Applies to SCLK, SI, SCS, DISP, EXTCOMIN

Design Note:
Supply EXTCOMIN with a 1HZ pulse to maintain current display.

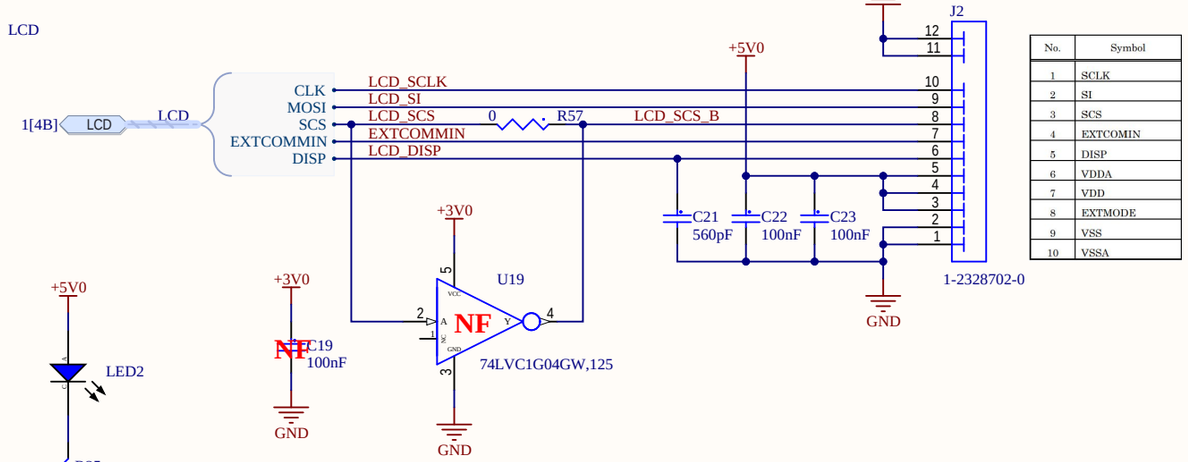
Ambient Light Sensor



Secure Element

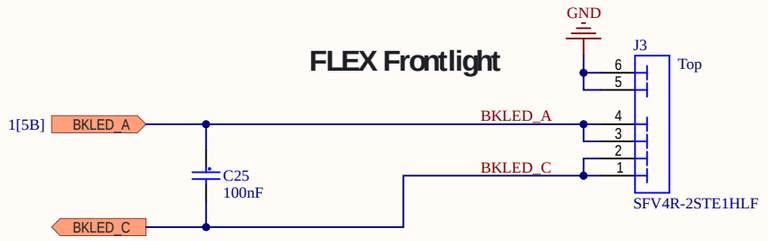


SHARP LCD

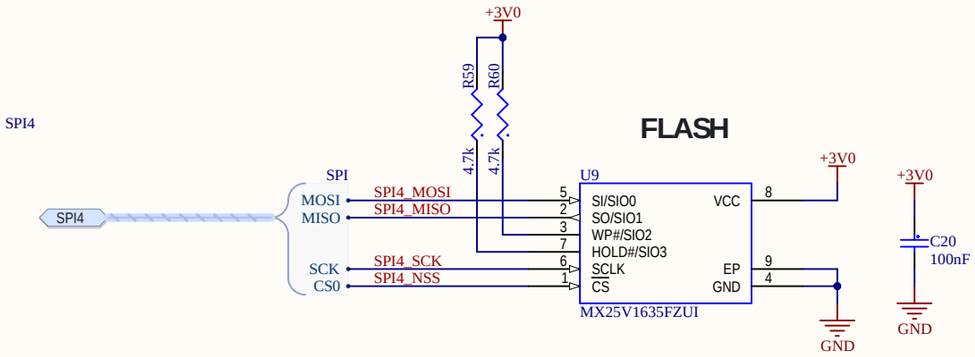


No.	Symbol
1	SCLK
2	SI
3	SCS
4	EXTCOMIN
5	DISP
6	VDDA
7	VDD
8	EXTMODE
9	VSS
10	VSSA

FLEX Frontlight



FLASH



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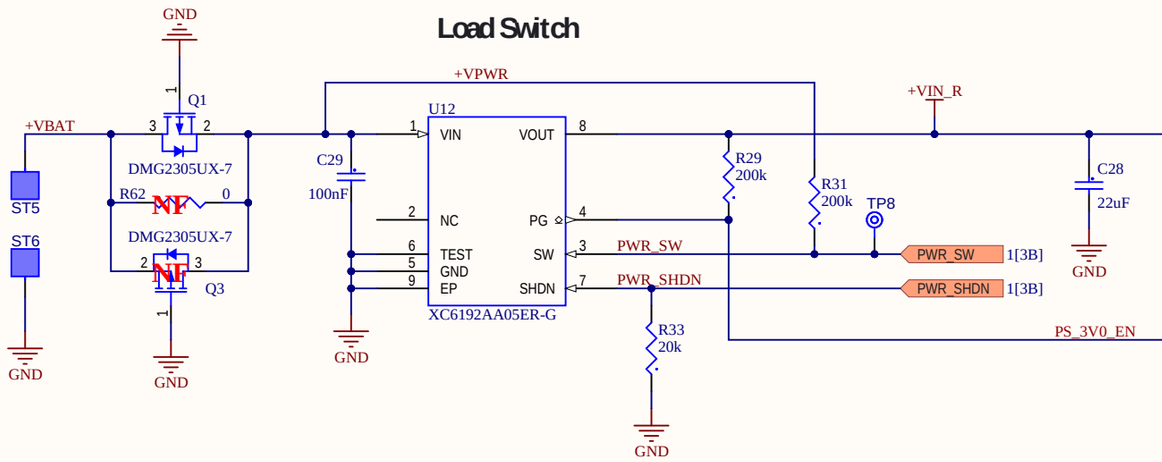
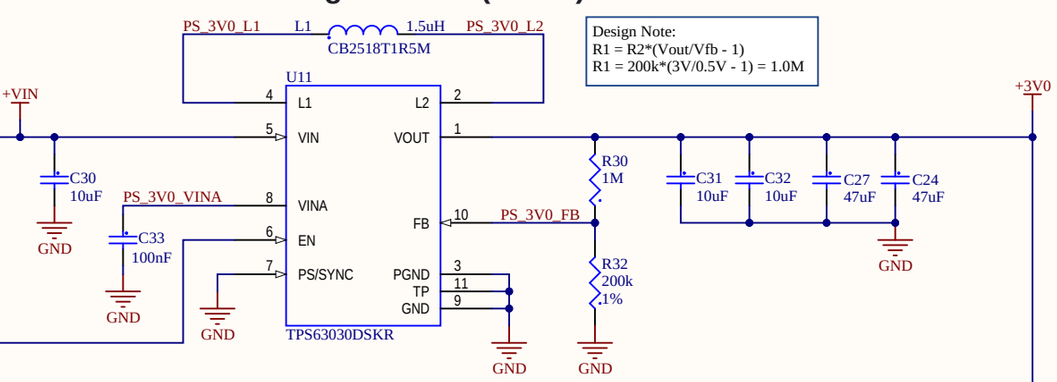
Power Regulators

Reverse Current Protection

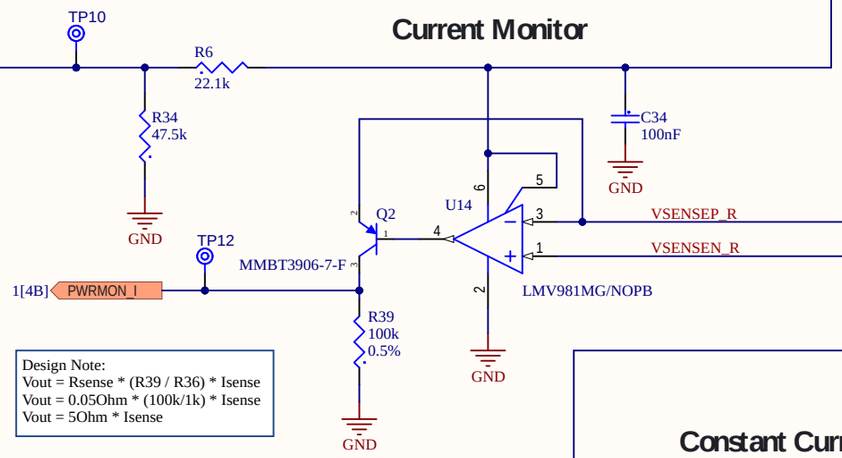
Load Switch



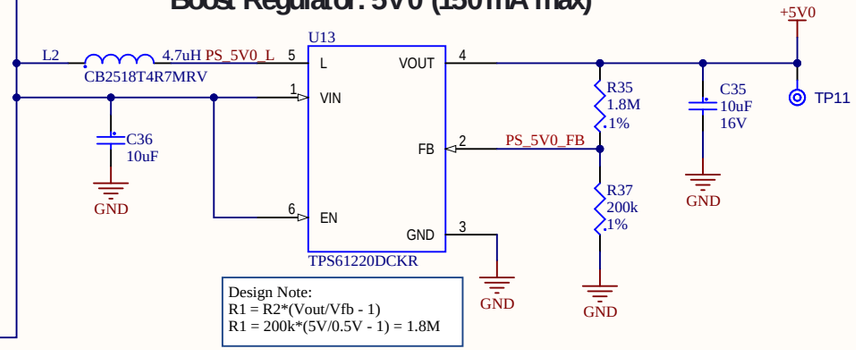
Boost-Buck Regulator: 3V0 (1A max)



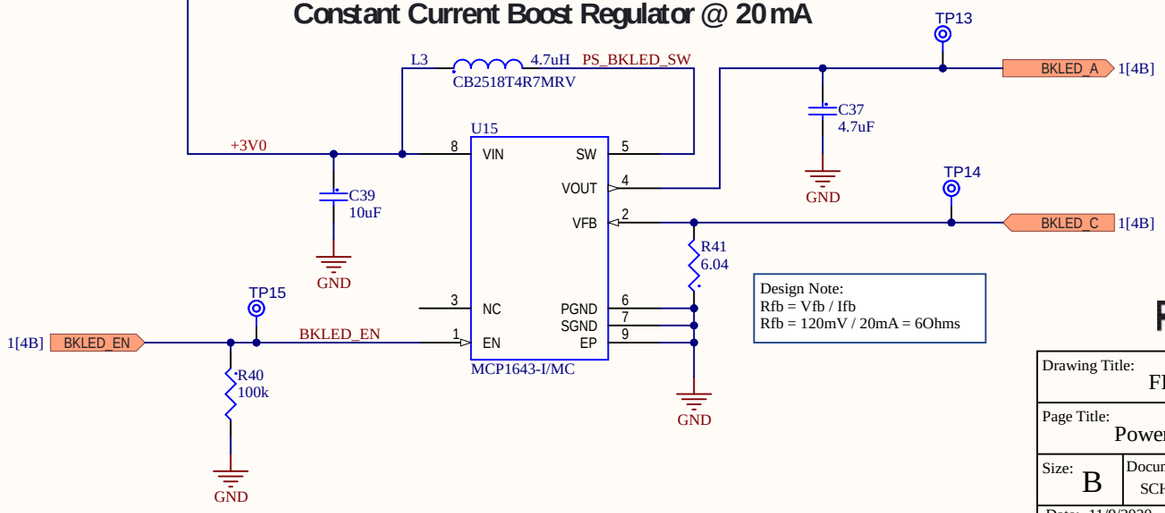
Current Monitor



Boost Regulator: 5V0 (150 mA max)



Constant Current Boost Regulator @ 20 mA



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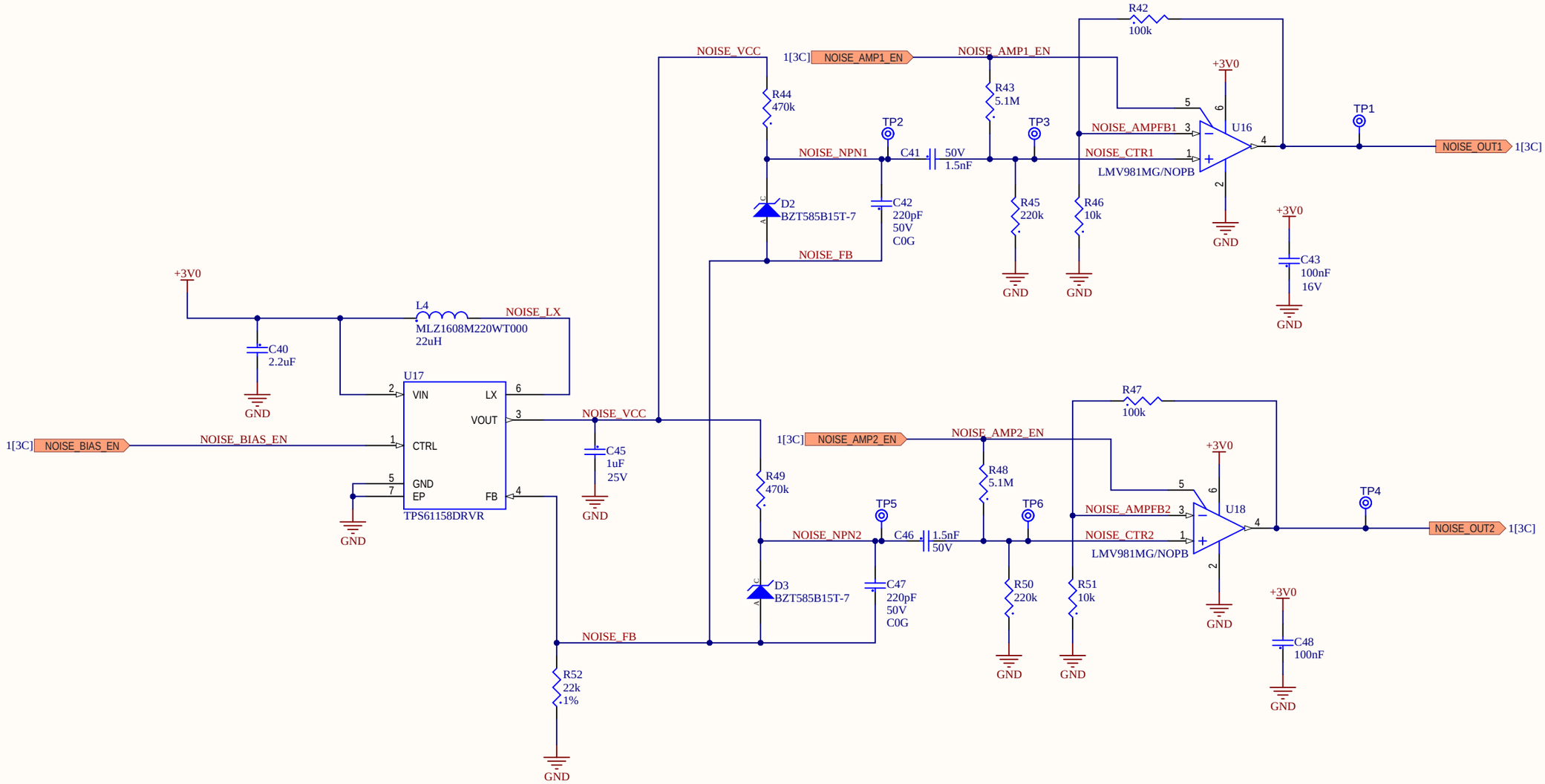
Avalanche Breakdown Noise Source



Circuit designed by:

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FOUNDATION

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