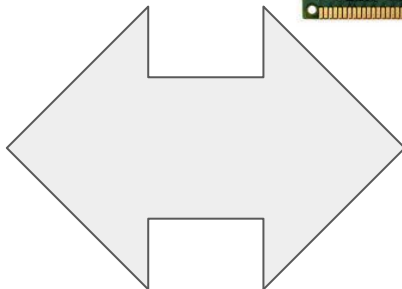
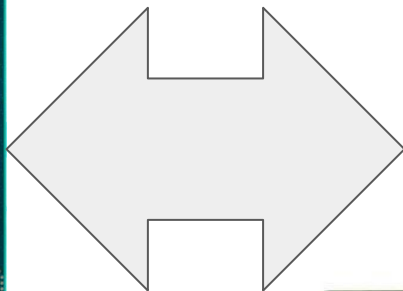
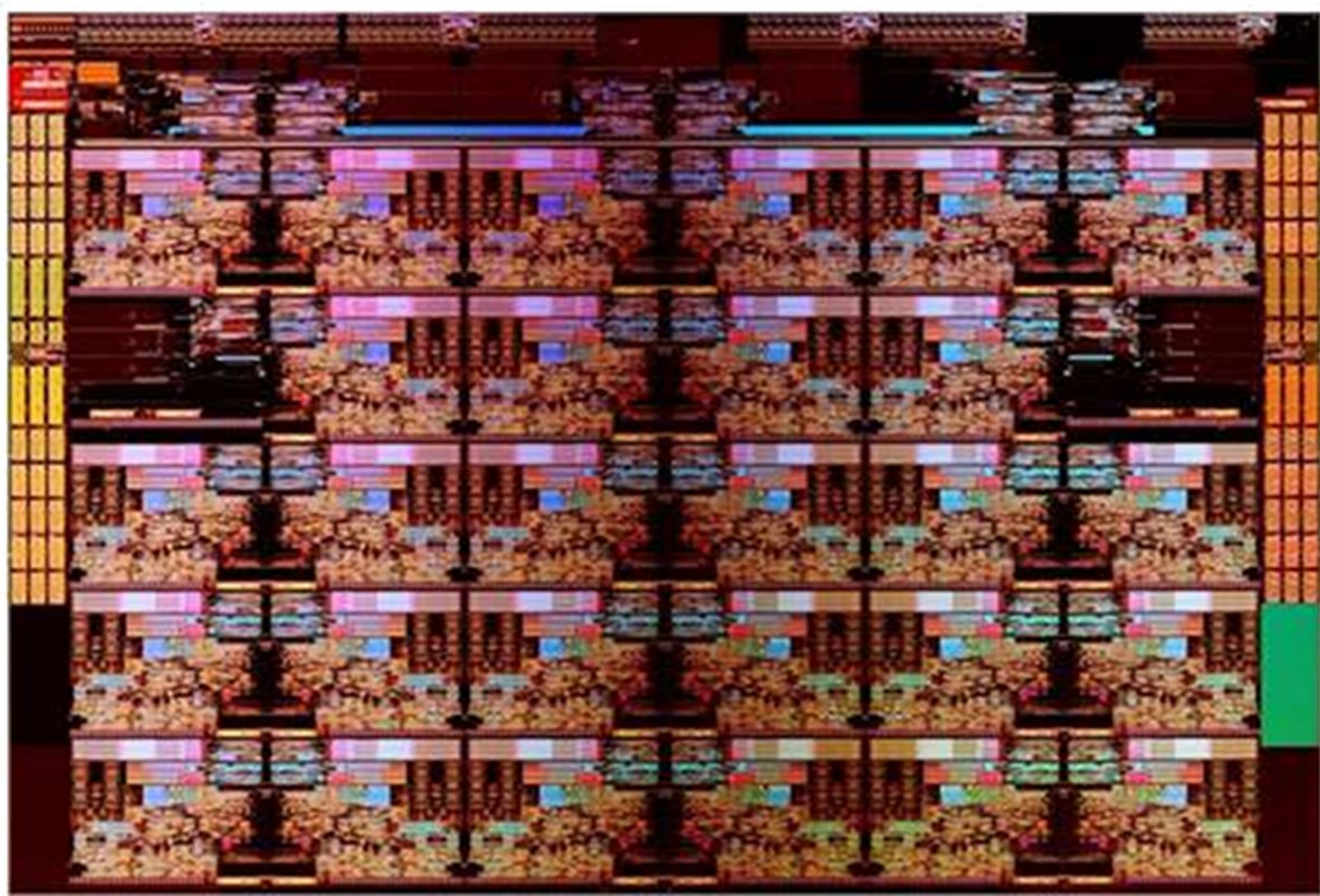
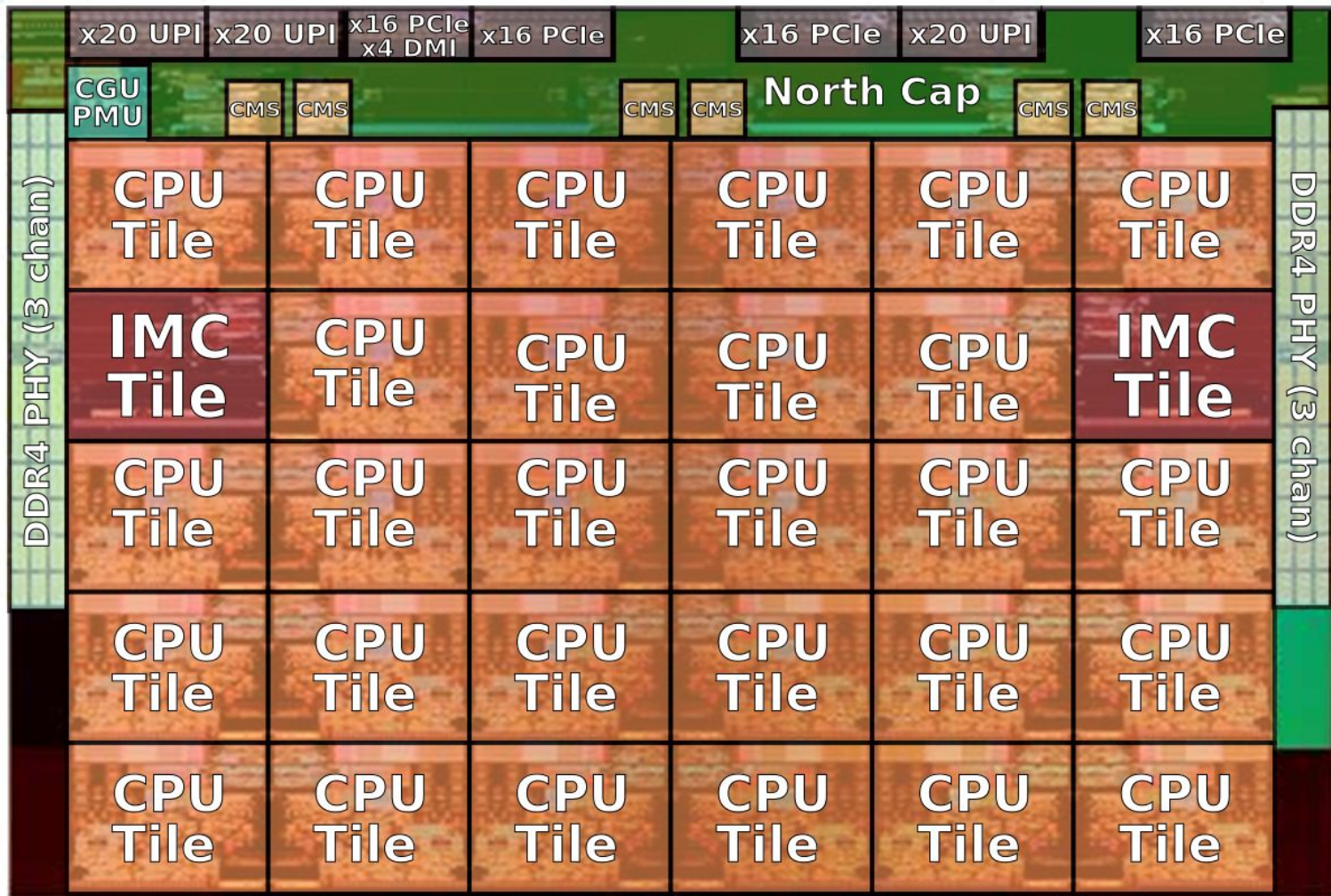
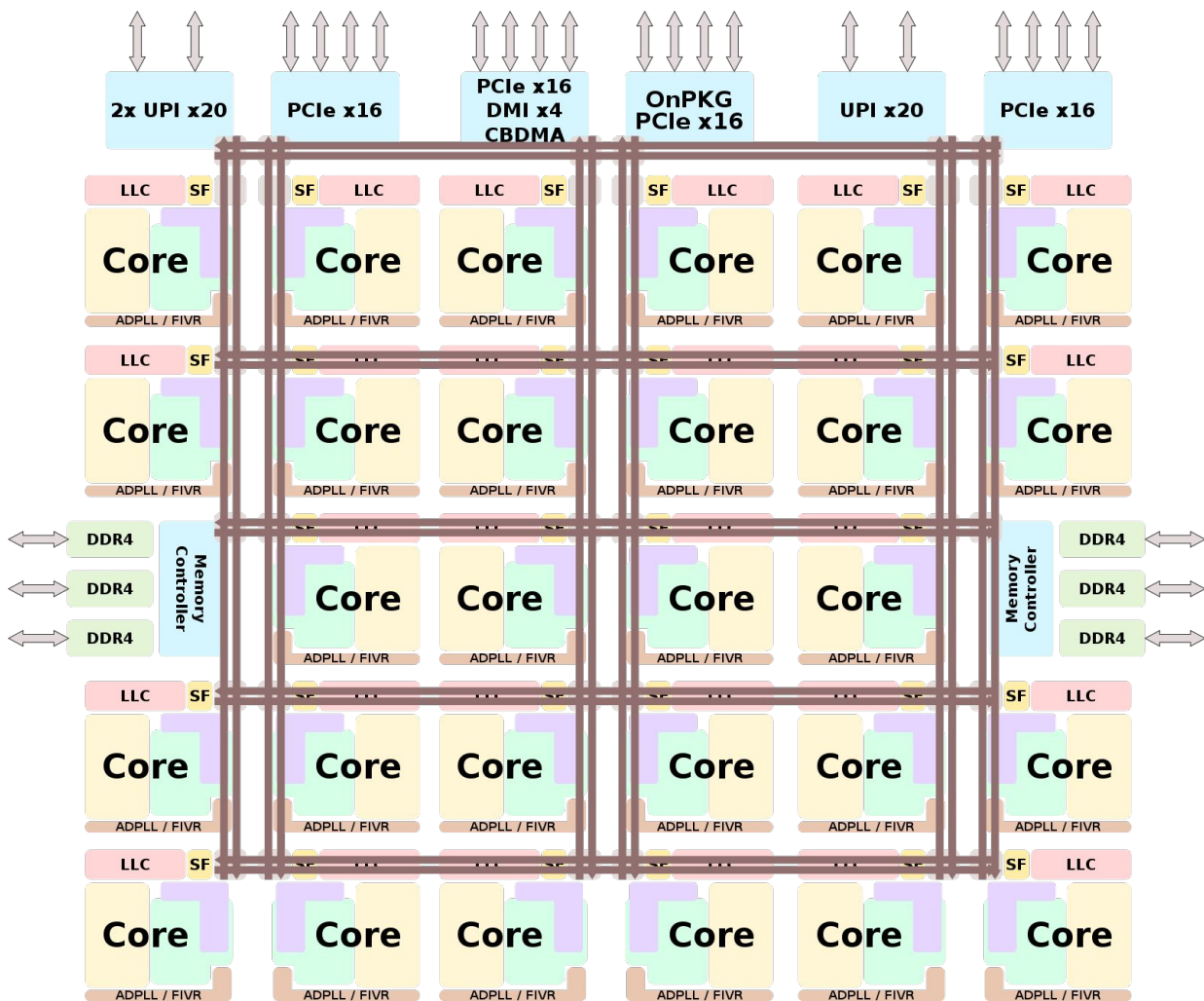


INTEL









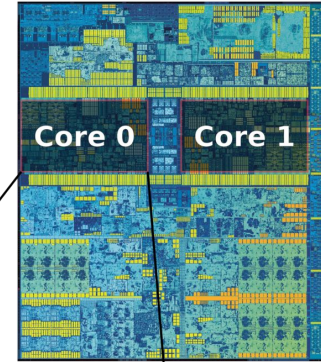
Server Arch

A Xenon

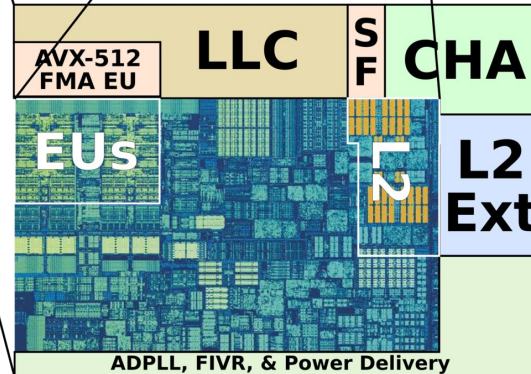


Client Arch

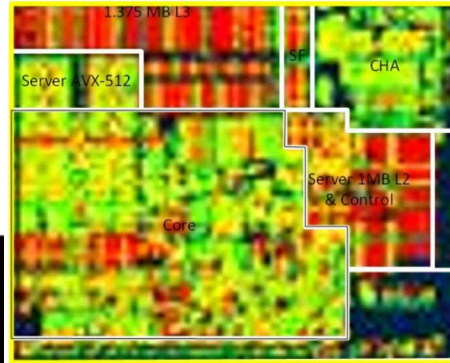
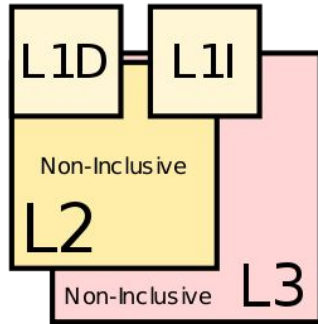
Your regular i3 processor



Extra parts are added.



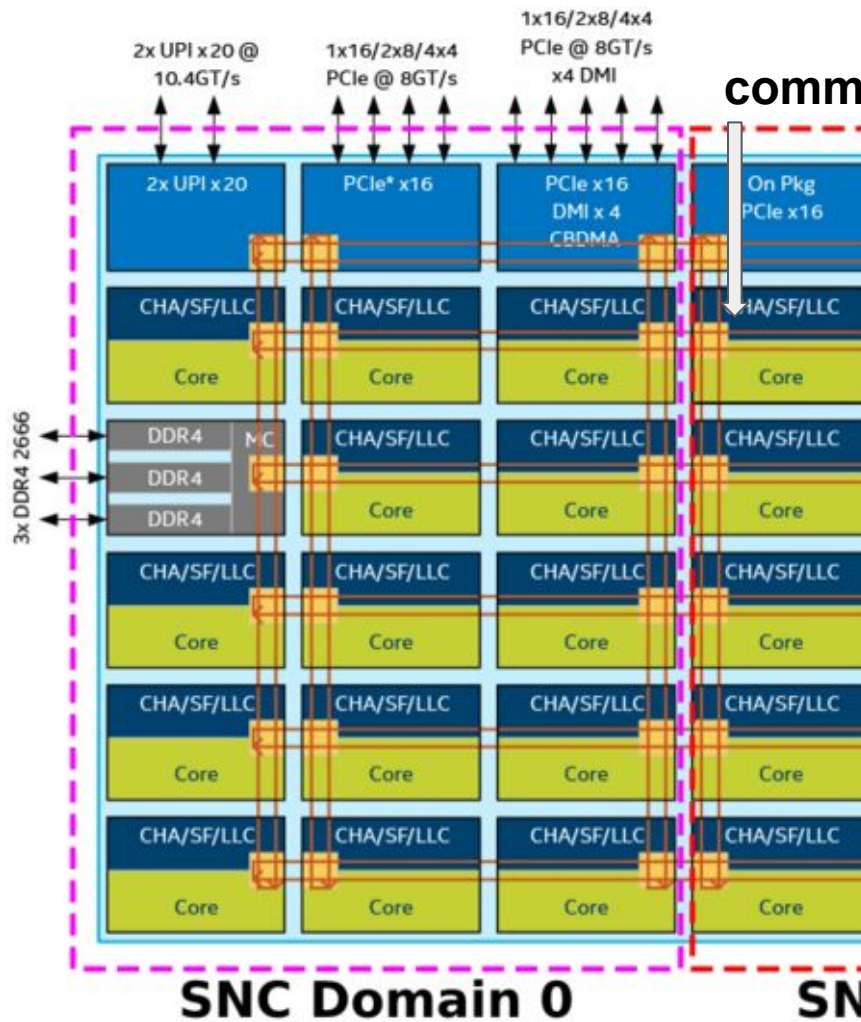
Skylake (SP/X)



LLC:= last level cache (L3)

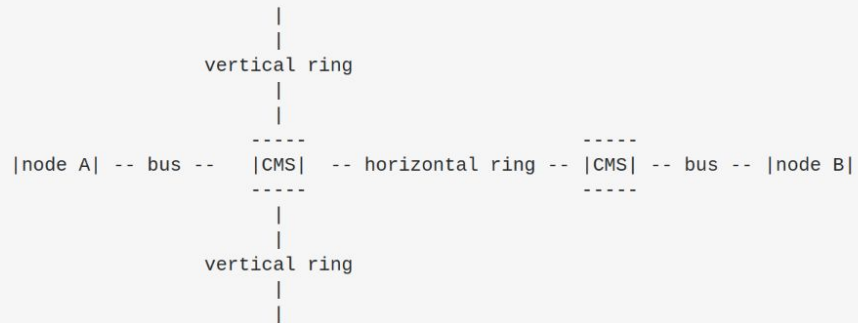
SF := snoop filter

CHA:= cache-home agent

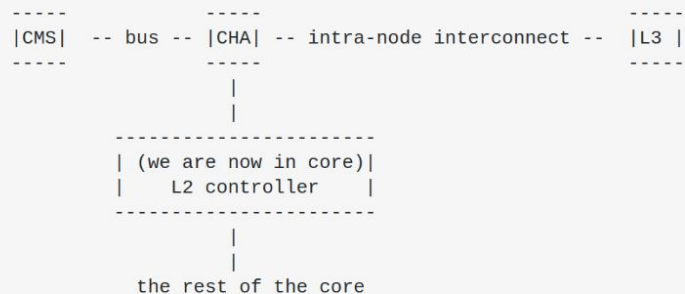


common mesh stop

The interconnect looks something like this:



Each node looks something like this:



Intel Ultra Path Interconnect

operational speed of up to 10.4 GT/s,

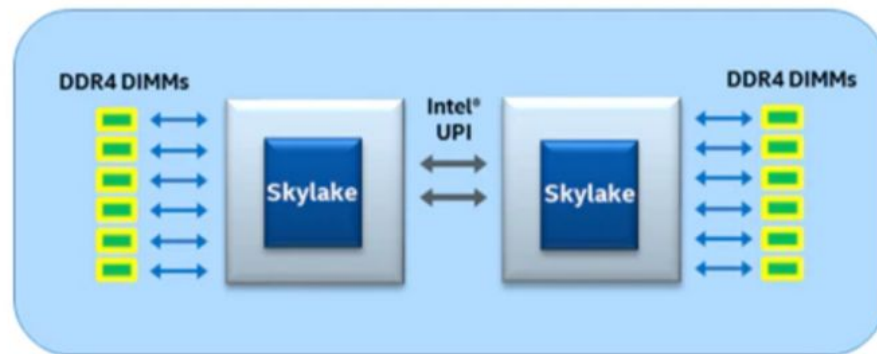
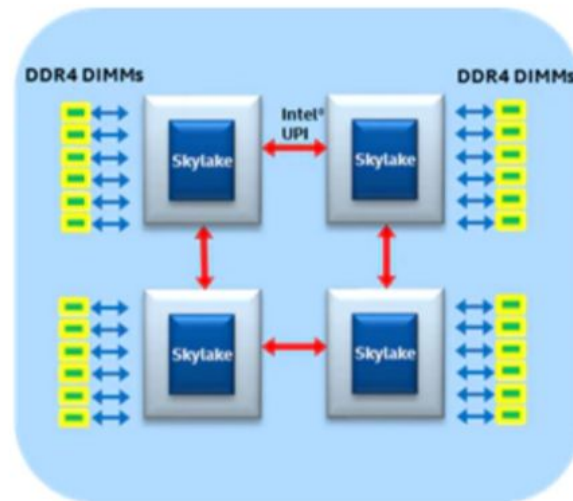
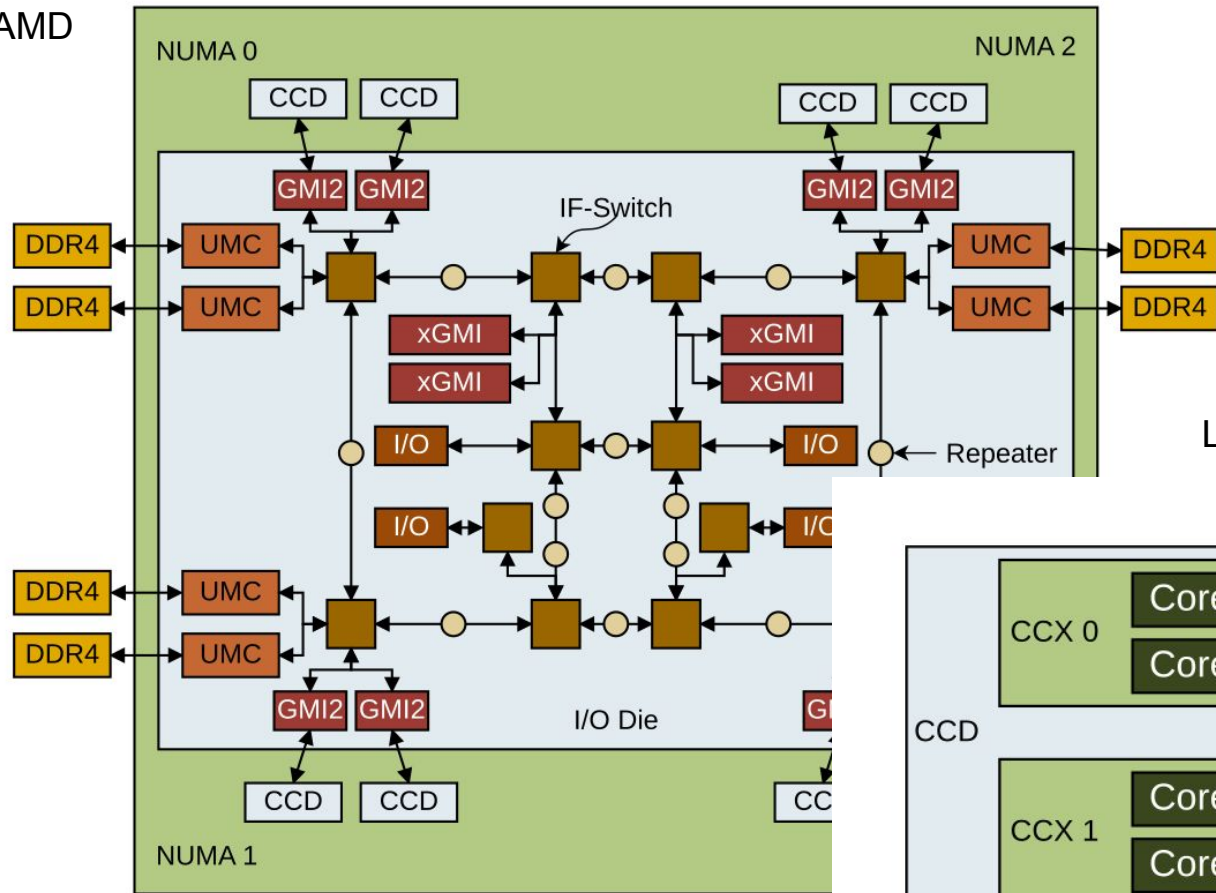


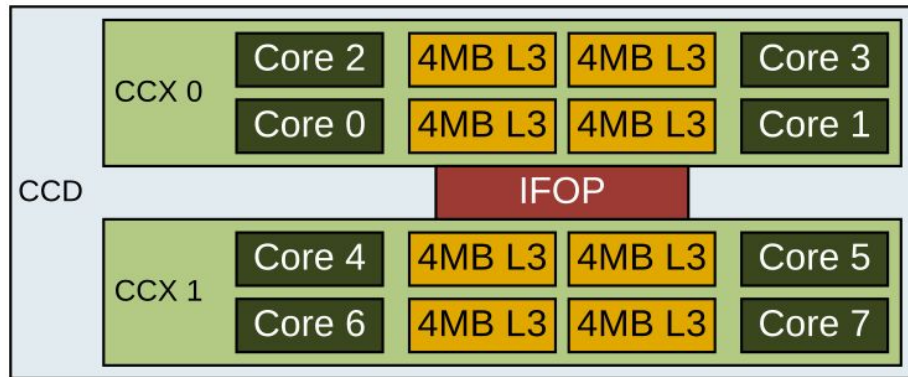
Figure 6. Typical two- socket configuration.



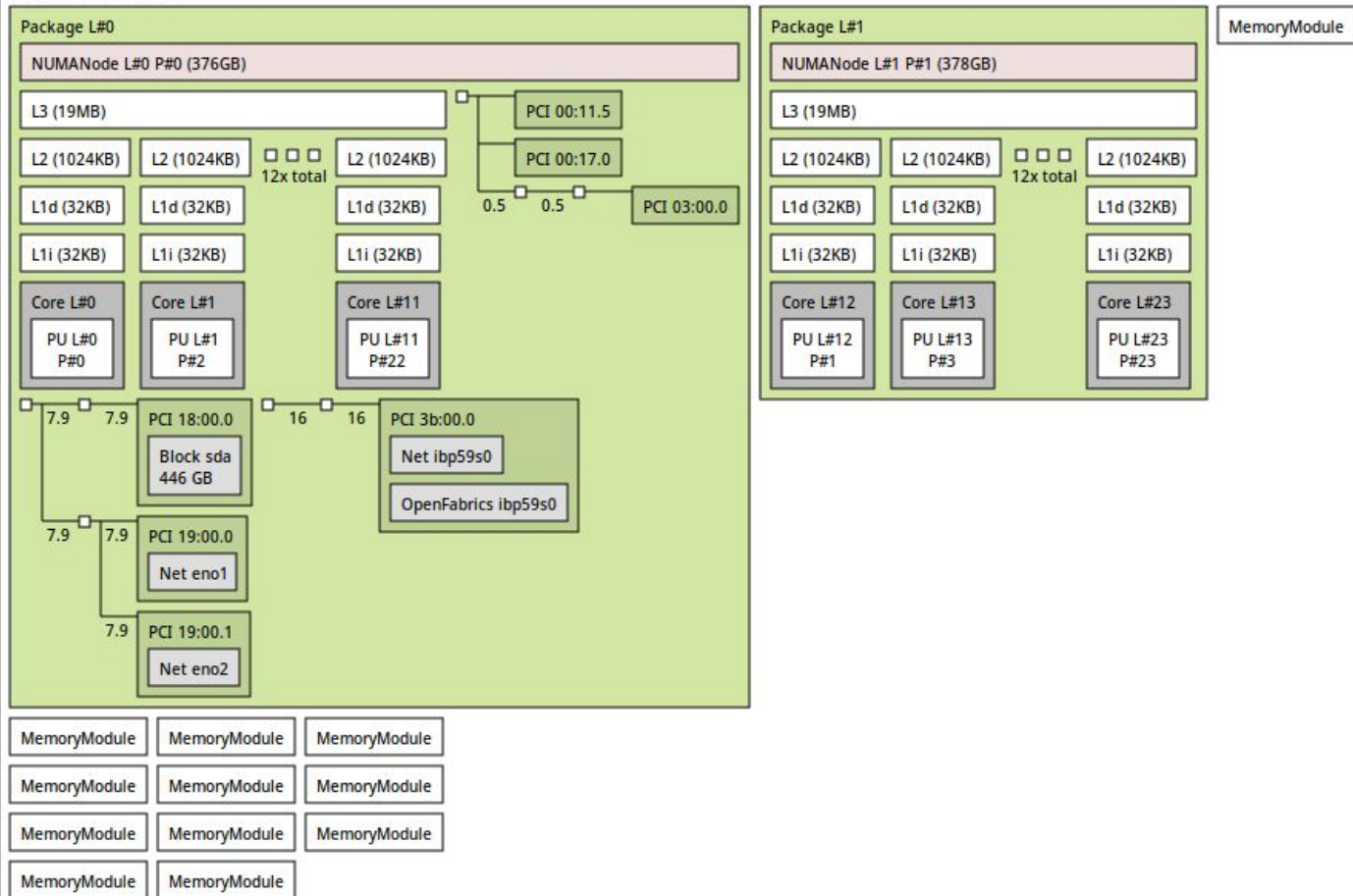
AMD



L3 is shared among 4 cores



Machine (754GB total)



Host: thin007

Date: Sun 04 Dec 2022 05:43:12 PM CET



MemoryModule	MemoryModule
MemoryModule	MemoryModule
MemoryModule	MemoryModule
MemoryModule	MemoryModule
MemoryModule	MemoryModule
MemoryModule	MemoryModule
MemoryModule	MemoryModule
MemoryModule	MemoryModule



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- [A] [AMD](#)
- [B] [CMS - skylake and newer ring bus](#)
- [C] [xeon technical overview](#)
- [C] [on inclusivity](#)