Connectors, IO

File: target.kicad_sch

Power

File: power.kicad_sch

FPGA Programming

File: fpgaprog.kicad_sch

FPGA 1

File: fpga 1.kicad_sch

User Button and IO

File: User Button and IO.kicad_sch

FPGA 2

File: FPGA 2.kicad_sch

FPGA Power

File: fpgapower.kicad_sch

H1 MountingHole

H2 MountingHole

H3 MountingHole

H4 MountingHole

cerg:cerg

CERG-Logo

Project: FOBOS Artix-7 a12t DUT

Author: Jens-Peter Kaps, Eddie Ferrufino

Cryptographic Engineering Research Group

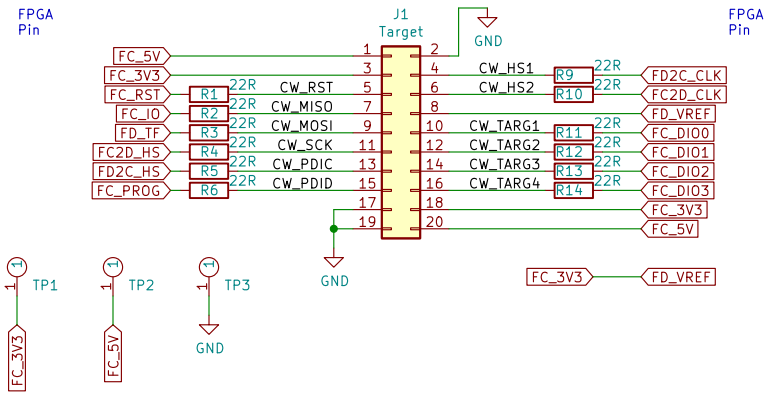
Sheet: /

File: dut-artix7-a12t.kicad_sch

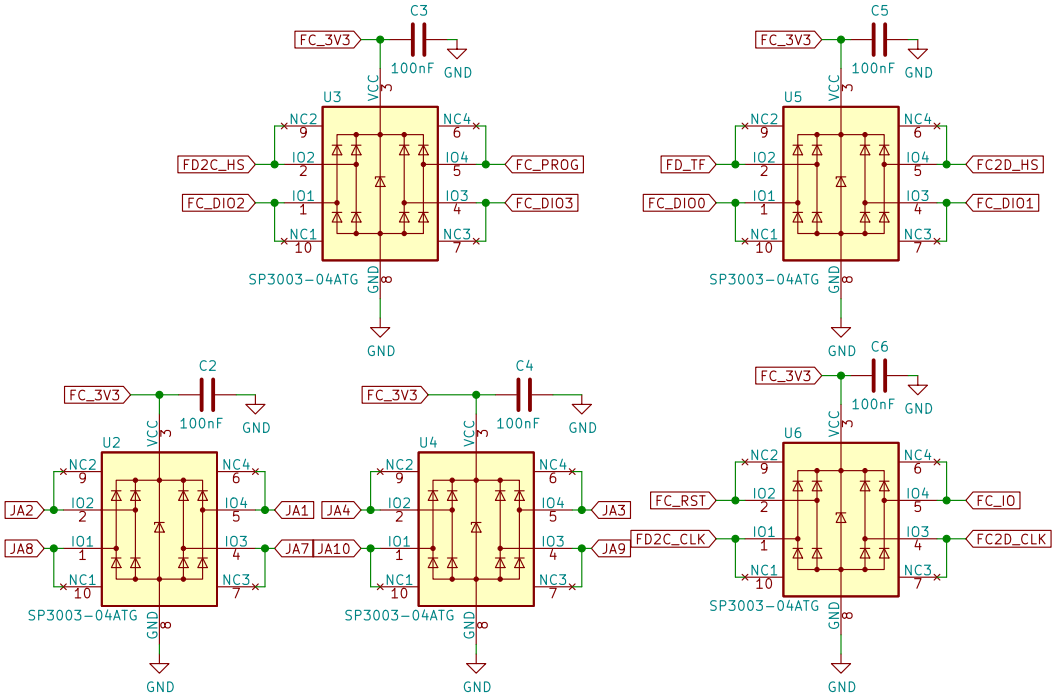
Title: FOBOS Artix-7 a12t DUT

Size: USLetter	Date: 2020-07-28	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.4)		Id: 1/8

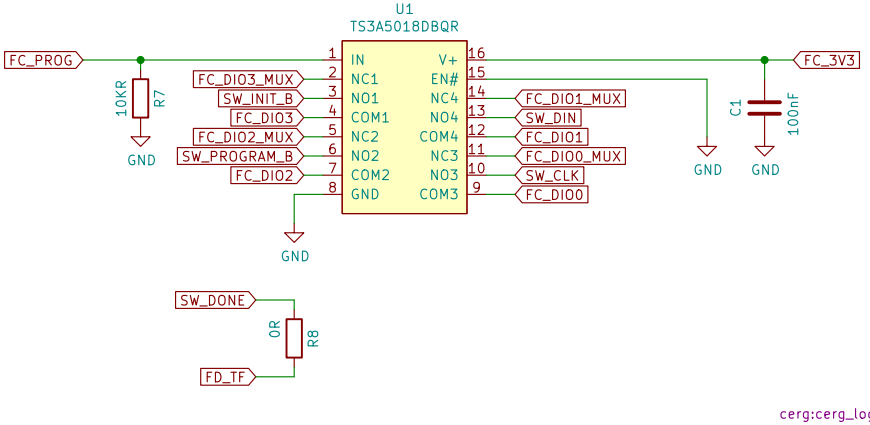
FOBOS Target Connector



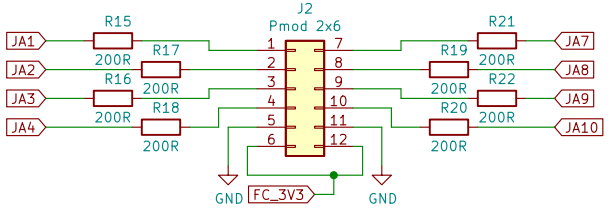
ESD Protection



Programming/DUT Communication Switches



PMOD Connector



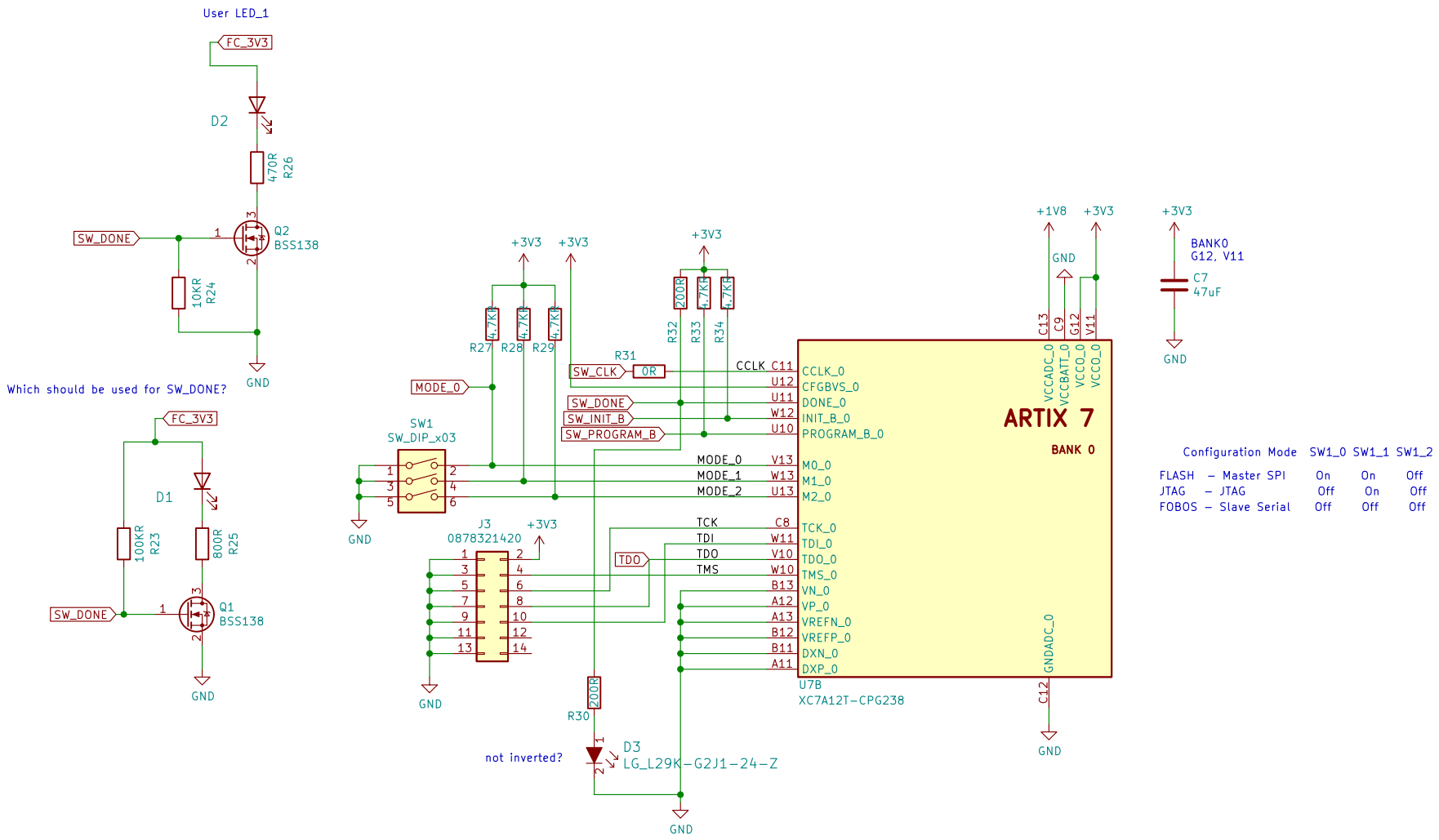
cerg:cerg_logo
CERG-Logo

Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino

Cryptographic Engineering Research Group
Sheet: /Connectors, IO/
File: target.kicad_sch

Title: FOBOS Artix-7 a12t DUT - Connectors, IO

Size: USLetter	Date: 2020-07-28	**Rev: 1.1**
KiCad E.D.A. kicad (6.0.4)		Id: 2/8

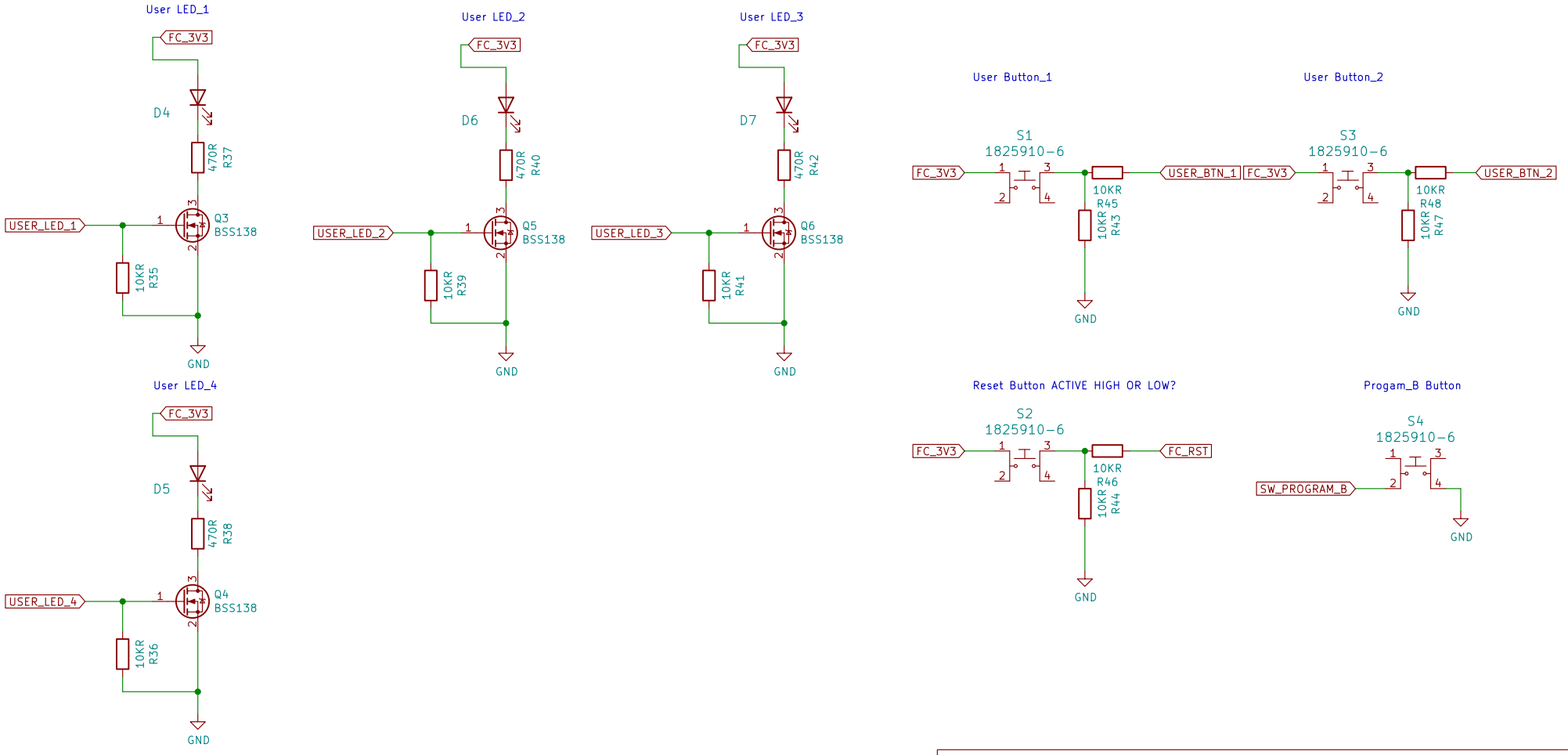


Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino

Cryptographic Engineering Research Group
Sheet: /FPGA Programming/
File: fpgaprog.kicad_sch

Title: FOBOS ARTIX7-A12T-CPG238 DUT – FPGA Programming

Size: USLetter	Date: 2020-07-28	**Rev: 1.1**
KiCad E.D.A. kicad (6.0.4)		Id: 3/8



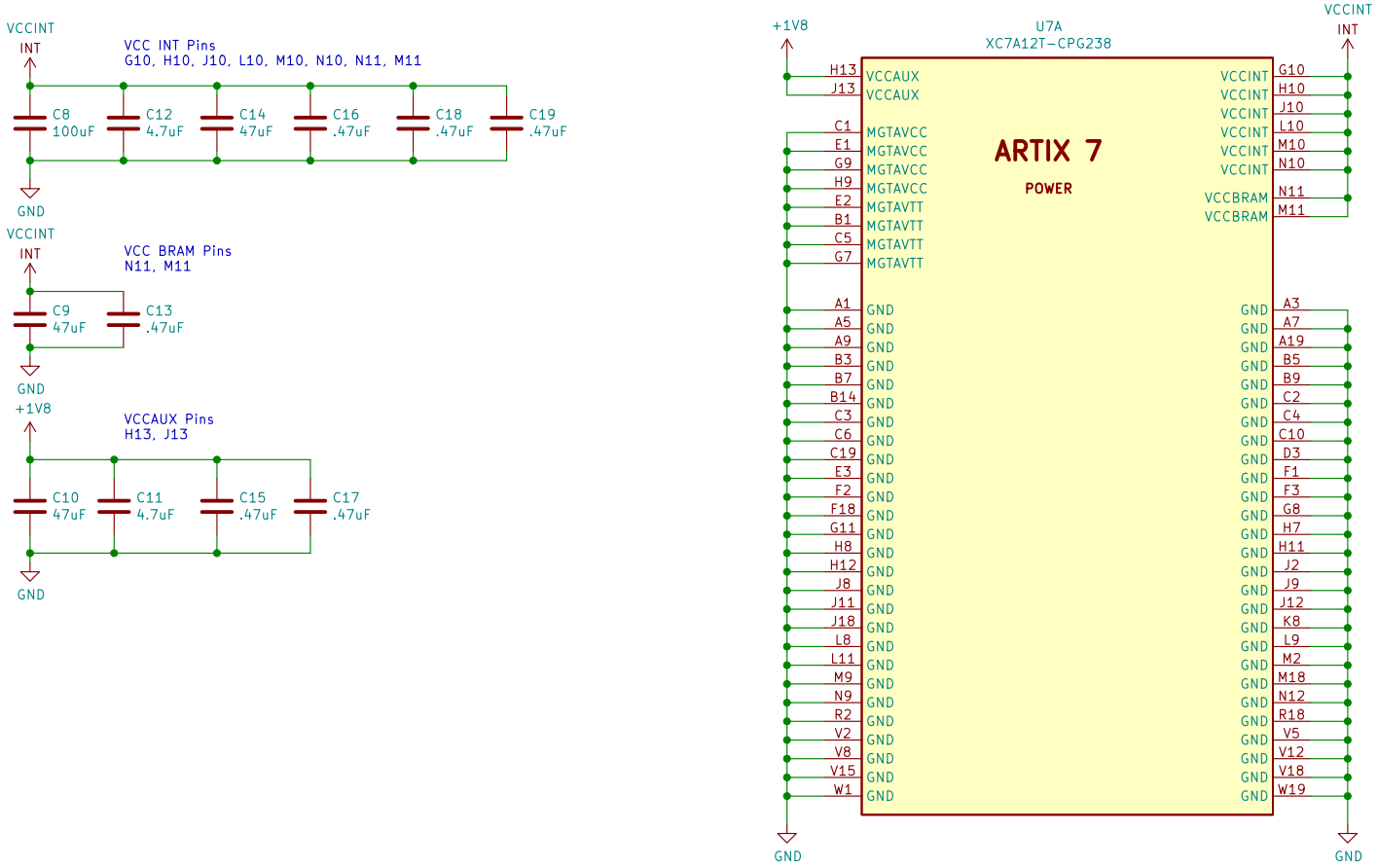
Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino

Cryptographic Engineering Research Group

Sheet: /User Button and IO/
File: User Button and IO.kicad_sch

Title: FOBOS Artix-7 a12t DUT - User Buttons and I/O

Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.4)		Id: 4/8



Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino

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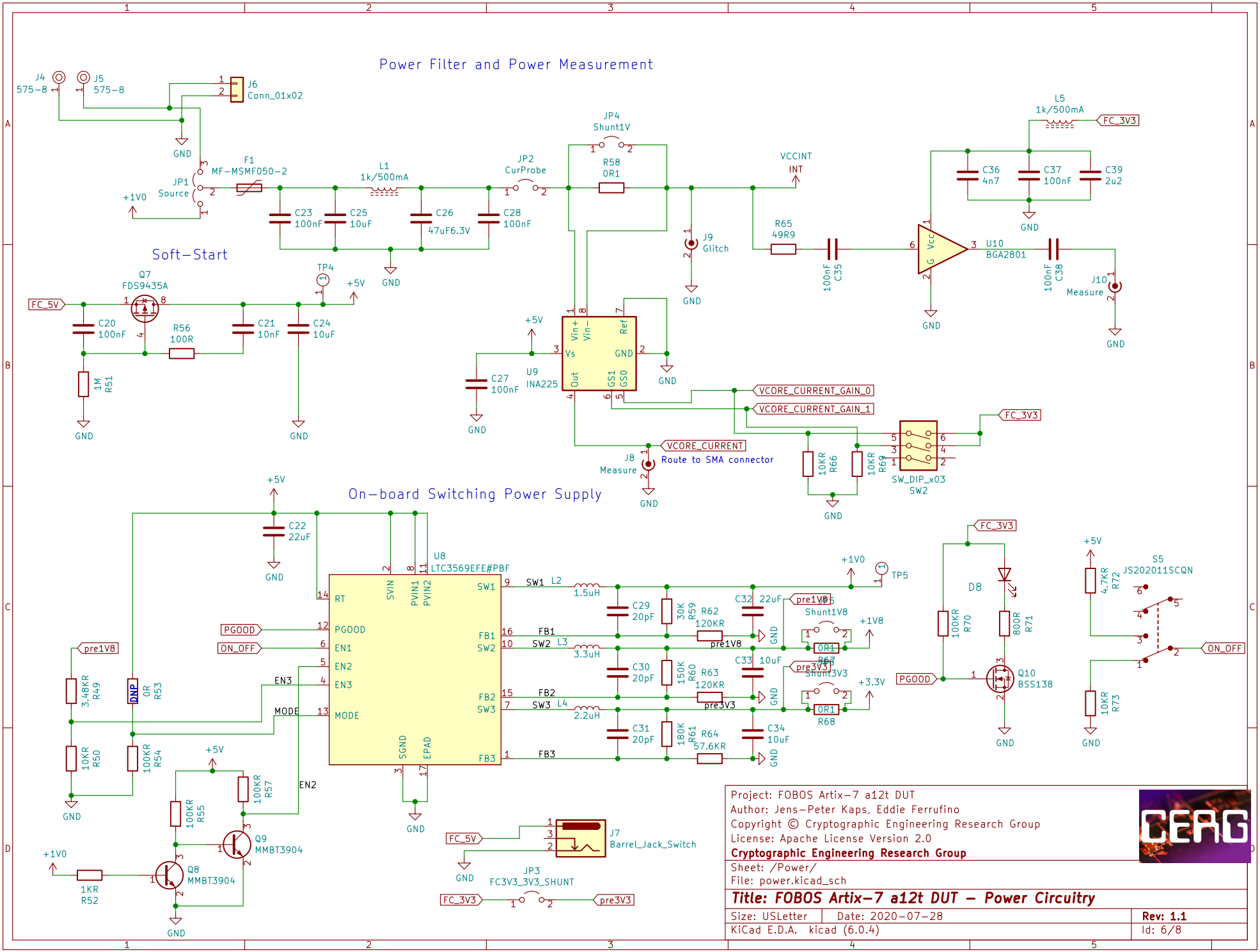
Sheet: /FPGA Power/
File: fpgapower.kicad_sch

Title: FOBOS Artix-7 a12t DUT - FPGA Power

Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.4)		Id: 5/8


Power Filter and Power Measurement
Soft-Start
On-board Switching Power Supply
J4 575-8
J5 575-8
J6 Conn_01x02
GND
F1 MF-MSMF050-2
JP1 Source
+1V0
L1 1k/500mA
C23 100nF
C25 10uF
C26 47uF6.3V
C28 100nF
JP2 CurProbe
JP4 Shunt1V
R58 0R1
VCCINT
INT
J9 Glitch
R65 49R9
100nF C35
U10 BGA2801
L5 1k/500mA
FC_3V3
C36 4n7
C37 100nF
C39 2u2
100nF C38
J10 Measure
Q7 FDS9435A
FC_5V
C20 100nF
R56 100R
C21 10nF
C24 10uF
TP4
+5V
1M R51
U9 INA225
C27 100nF
VCORE_CURRENT_GAIN_0
VCORE_CURRENT_GAIN_1
VCORE_CURRENT
J8 Measure
Route to SMA connector
10KR R66
10KR R69
SW_DIP_x03 SW2
C22 22uF
U8 LTC3569EFE#PBF
PGOOD
ON_OFF
EN1
EN2
EN3
MODE
RT
SVIN
PVIN1
PVIN2
SW1
FB1
SW2
FB2
SW3
FB3
SGND
EPAD
L2 1.5uH
L3 3.3uH
L4 2.2uH
C29 20pF
C30 20pF
C31 20pF
30K R59
150K R60
180K R61
R62 120KR
R63 120KR
R64 57.6KR
C32 22uF
C33 10uF
C34 10uF
pre1V8
pre3V3
Shunt1V8
Shunt3V3
0R1 R67
0R1 R68
+1V8
+3.3V
TP5
3.48KR R49
DNP
0R R53
10KR R50
100KR R54
100KR R55
100KR R57
Q8 MMBT3904
Q9 MMBT3904
1KR R52
D8
100KR R70
800R R71
Q10 BSS138
S5 JS202011SCQN
4.7KR R72
10KR R73
J7 Barrel_Jack_Switch
JP3 FC3V3_3V3_SHUNT
Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino
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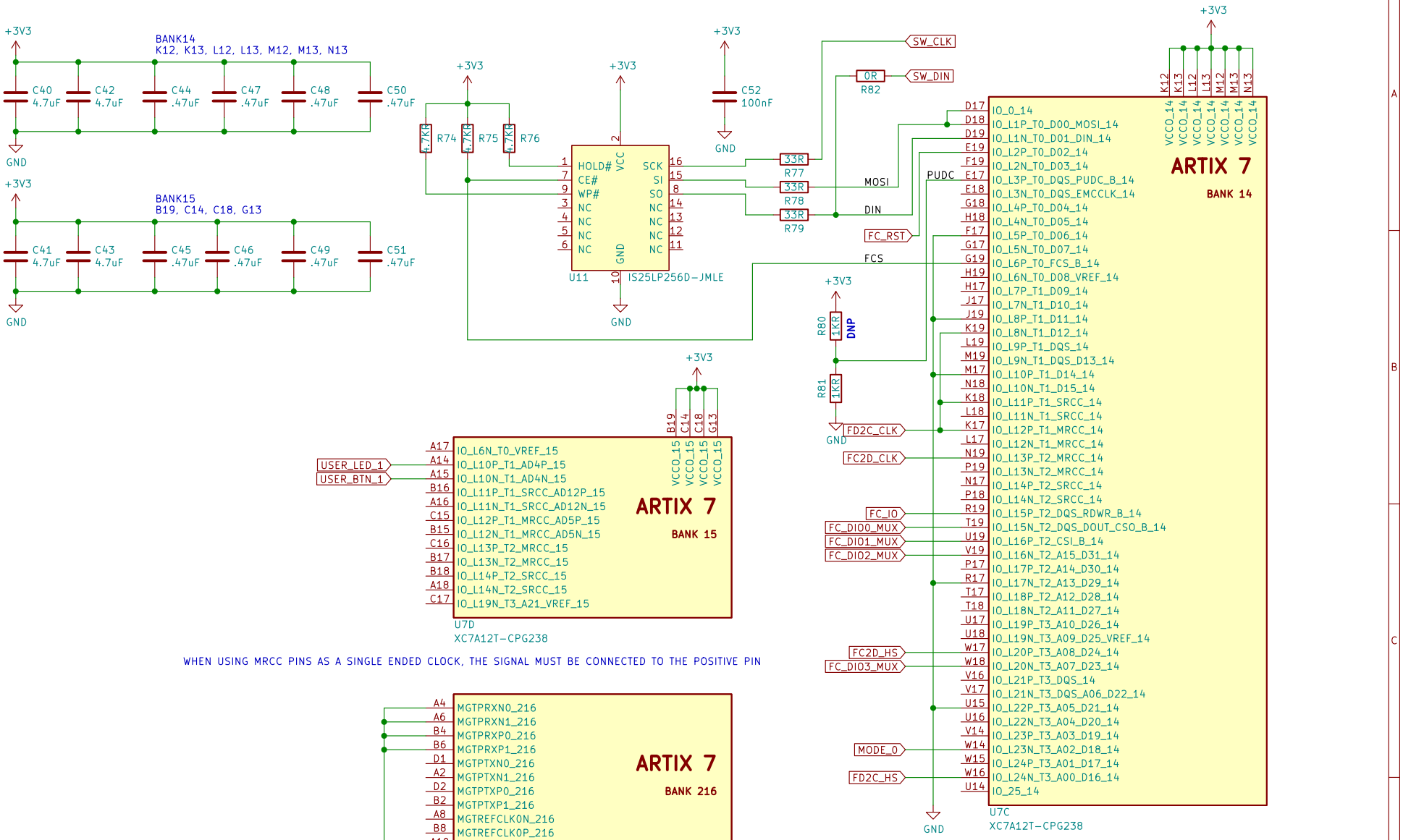
Sheet: /Power/
File: power.kicad_sch
Title: FOBOS Artix-7 a12t DUT - Power Circuitry
Size: USLetter
Date: 2020-07-28
Rev: 1.1
KiCad E.D.A. kicad (6.0.4)
Id: 6/8



Project: FOBOS Artix-7 a12t DUT
Author: Jens-Peter Kaps, Eddie Ferrufino

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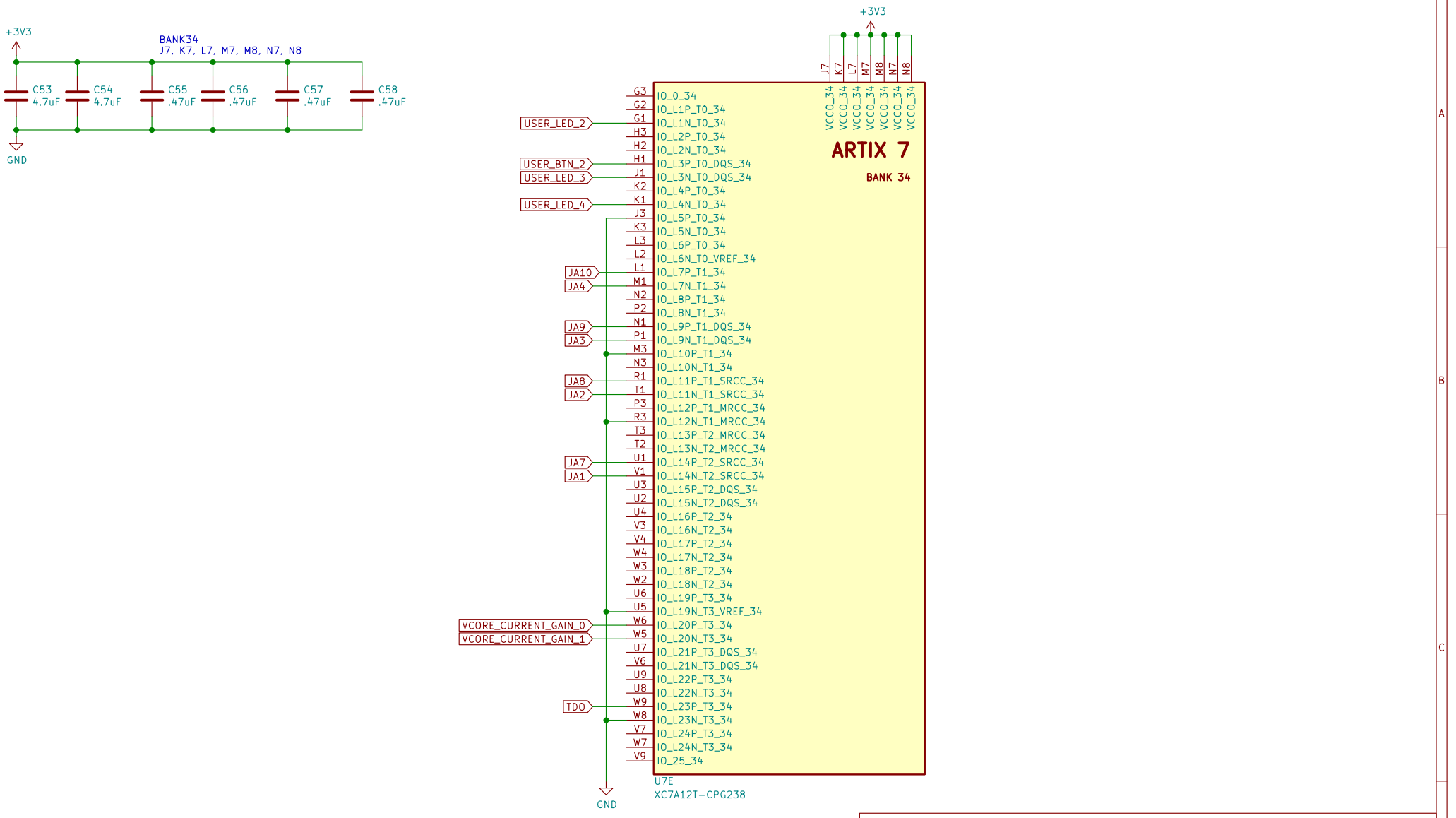
Sheet: /FPGA 1/
File: fpga 1.kicad_sch

Title: FOBOS Artix-7 a12t DUT - FPGA

Size: USLetter	Date: 2020-07-28	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.4)		Id: 7/8



WHEN USING MRCC PINS AS A SINGLE ENDED CLOCK, THE SIGNAL MUST BE CONNECTED TO THE POSITIVE PIN

Sheet: /FPGA 2/
File: FPGA 2.kicad_sch

Title: FOBOS Artix-7 a12t DUT - FPGA Part 2

Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.4)		Id: 8/8