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A Litrature Review on Golay Code Encoder and Decoder in Digital Communication

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ABSTRACT

In this survey paper shows the literature review of golay code in digital communication. A bird eye review for Golay code is presented in this research work. A Golay code is presented addressing the error correcting phenomena. This is used in field programmable gate array (FPGA). There are various researchers presents there techniques for correcting the error check. This research work reviews that work.

Keywords— Architecture, decoder, encoder, field programmable gate array (FPGA), Golay code

I. INTRODUCTION

The Golay code was presented in [2] to address error correcting phenomena. The binary Golay code (G23) is represented as (23, 12, 7), while the extended binary Golay code (G24) is as (24, 12, 8). The extended Golay code has been used extensively in deep space network of JPL-NASA as well as in the Voyager imaging system [6]. In addition, Golay code plays a vital role in different applications like coded excitation for a laser [7] and ultrasound imaging due to the complete sidelobe nullification property of complementary Golay pair. All these applications need generation of Golay sequence, which is fed as trigger to the laser modules. However, for generating Golay code an automatic pattern generator is used, which is of very high cost. To combat this problem, a hardware module programmed to yield a Golay encoded codeword may be used. Golay decoder is used extensively in communication links for forward error correction. Therefore, a high speed and high throughput hardware for decoder could be useful in communication links for forward error correction.

There are two closely related binary Golay codes. The **extended binary Golay code**, G_{24} (sometimes just called the "Golay code" in finite group theory) encodes 12 bits of data in a 24-bit word in such a way that any 3-bit errors can be corrected or any 7-bit errors can be detected. The other, the **perfect binary Golay code**, G_{23}, has codewords of length 23 and is obtained from the extended binary Golay code by deleting one coordinate position (conversely, the extended binary Golay code is obtained from the perfect binary Golay code by adding a parity bit). In standard code notation the codes have parameters [24, 12, 8] and [23, 12, 7], corresponding to the length of the codewords, the dimension of the code, and the minimum Hamming distance between two codewords, respectively.

In mathematical terms, the extended binary Golay code G_{24} consists of a 12-dimensional linear subspace W of the space $V=\mathbf{F}_2^{24}$ of 24-bit words such that any two distinct elements of W differ in at least 8 coordinates. W is called a linear code because it is a vector space. In all, W comprises $4096 = 2^{12}$ elements.

The elements of W are called *code words*. They can also be described as subsets of a set of 24 elements, where addition is defined as taking the symmetric difference of the subsets.

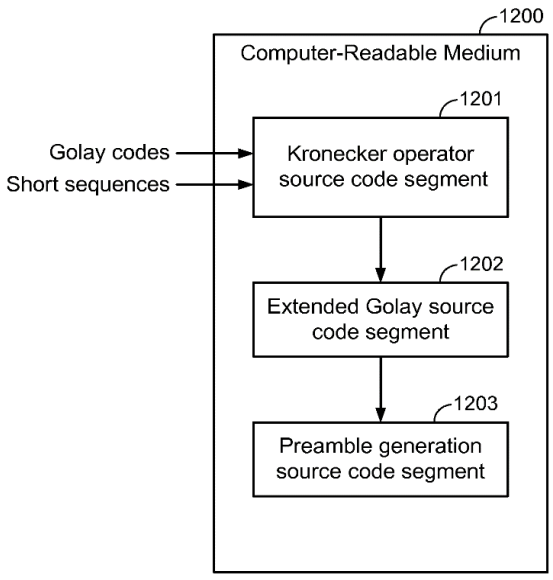

Fig.1 Shiows the Golay Codes Applying Phenomena

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- In the extended binary Golay code, all code words have Hamming weights of 0, 8, 12, 16, or 24. Code words of weight 8 are called **octads** and code words of weight 12 are called **dodecads**.
- Octads of the code G_{24} are elements of the S(5,8,24) Steiner system. There are 759 = 3*11*23 octads and 759 complements thereof. It follows that there are $2576 = 2^4*7*23$ dodecads.
- Two octads intersect (have 1's in common) in 0, 2, or 4 coordinates in the binary vector representation (these are the possible intersection sizes in the subset representation). An octad and a dodecad intersect at 2, 4, or 6 coordinates.
- Up to relabeling coordinates, W is unique.

The binary Golay code, G_{23} is a perfect code. That is, the spheres of radius three around code words form a partition of the vector space. G_{23} is a 12-dimensional subspace of the space $\mathbf{F}_2^{23}$.

II. LITERATURE SURVEY

A. Satyabrata Sarangi, Swapna Banerjee, "Efficient Hardware Implementation of Encoder and Decoder for Golay Code", 2015

This scheme provides a cyclic redundancy check-based encoding scheme and provides an efficient implementation of the coding algorithm in the FPGA prototype for both the binary Golay code (G23) and the extended binary Golay code (G24). High-Speed With low-latency architecture was developed and implemented in Virtex-4 FPGA for Golay encoders without incorporating linear feedback shift registers. This letter also provides an optimized and decompressed decoding architecture for extended binary Golay code (24, 12, 8) based on an incomplete maximum likelihood decoding scheme. The proposed architecture for decoders occupies less space and has a lesser latency than some of the recent works published in this area. The encoding module runs at 238.575 MHz, while the proposed architecture for the decoder has an operating clock frequency of 195.028 MHz. The proposed hardware modules may be a good candidate for forward error correction in the communication link, which requires a high speed system.

B. Xiao-Hong Peng, Member, Paddy G. Farrell, "On Construction of the (24, 12, 8) Golay Codes"

Two product array codes are used to construct the (24, 12, 8) binary Golay code by the direct sum operation. This design provides a systematic way to find correct (8, 4, 4) linear block component codes for generating the Golay code, and it creates and expands existing procedures using a similar construction framework. The generated code is easy to decode.

There are several ways to decode the (24, 12, 8) Golay code, such as the decoders based on the hexadecond constructions for arbitration decision and single decode decoding. For the construction based on (6), a regular grating can be produced using various techniques. This trellis has three sections of length 8 and 64 states at each section boundary. It consists essentially of eight structurally identical sub-trellisms and thus enables a simple and fast maximum likelihood decoding since these sub-trellis can be processed in parallel. Trellises with such a structure are desirable since this can significantly reduce the connections within the IC and the chip size, which is of great importance in the implementation of trellis decoding using DSP and VLSI technologies. The decoding complexity can be further reduced by simplifying the sub-trellisings by initial decoding on the component code C1.

C. Michael Sprachmann, "Automatic Generation of Parallel CRC Circuits"

A parallel CRC circuit simultaneously processes multiple data bits. A generic VHDL description of parallel CRC circuits allows designers to synthesize CRC circuits for each generator polynomial or the required parallelism.

A generic VHDL description of a general parallel CRC circuit is presented. The underlying method is based on the basic LFSR cascading. The VHDL description hides algebraic transformations and allows the designer to easily explore constructional alternatives.

The synthesis tool automatically generates the final feedback network of the CRC circuit. Particularly in reusable embodiments, a generic description of the fault monitoring circuit is very attractive because the generator polynomial is usually dependent on the application domain. In this case, the feedback network is generated individually during logic synthesis.

The area and speed of the circuit show a linear dependence on the parallelism quantity. A hardware increase of 5 to 10% can be estimated per bit in parallel processes. Provided that the feedback network does not contribute to the critical path of the entire design, the parallel solution can result in an acceleration proportional to the parallelism involved.

D. Giuseppe Campobello, Giuseppe Patane,Marco Russo, "Parallel CRC Realization"

This paper presents a theoretical result in connection with the realization of high-speed hardware for parallel CRC checksums. Starting from the serial implementation widely used in the literature, we have identified a recursive formula from which our parallel implementation is derived. Compared to earlier work, the new system is faster and more compact and independent of the technology used. In our solution, the number of bits processed in parallel can be different from the degree of the polynomial generator. Finally, we have also developed high-level parametric codes that are capable of generating the circuits autonomously, if only the polyonomy is given.

E. Ayyoob D. Abbaszadeh, Craig K. Rushforth, VLSI Implementation of a Maximum-Likelihood Decoder for the Golay (24, 12) Code

Conway and Sloane recently introduced a new algorithm for the exact maximum-likelihood decoding of the Golay code (24,12) in the additive white Gaussian noise channel, which requires significantly fewer calculations than previous algorithms. In this work we describe an efficient hit-serial VLSI implementation of this algorithm. Our design consists of two chips that have been developed using path-programmable logic (PPL) and a related system of automated design tools for 3 pm NMOS technology. We estimate that this decoder will produce an information bit every 1.6-2.4 ps. Higher speeds can be

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achieved by using a faster technology or by replicating the chips to perform more operations in parallel.

F. Shyue-Win We1, Che-Ho Wei, "On High-speed Decoding of the (23,12,7) Golay Code"

An algebraic decoding method for triple-error-correcting binary BCH codes applicable upon complete decoding of the (23, 12, 7) Golay code has recently been demonstrated. A modified step-by-step complete decoding algorithm of this Golay code is introduced that requires less relocation operations than the kasami error trapping decoder. Based on the algorithm, a high speed hardware decoder of this code is proposed.

Kasamis error trapping decoder is one of the most popular decoders for decoding the (23, 12, 7) Golay code. In the Kasami decoder, 46 shift operations are required to decode a completed received word, while the new step-by-step method requires only 35 shift operations when the code word is in a systematic form. Thus, this new step-by-step decoder is faster than the Kasami decoder with the same clock rate. Consequently, this new decoding algorithm is suitable for hardware implementation and a high-speed decoder of this code is illustrated. This decoder also needs 35 clock cycles to decode a word and can operate at a data rate up to 2 Mb / s. When the Chien search method is used, it requires two circuits to calculate the syndrome values and the coefficients of the error location polynomial. The complexity of these circuits is comparable to the syndrome calculation circuit and the comparison circuitry of the new step-by-step decoder. However, the Chien search method still requires a complex circuit for finding or solving the roots of the fault location polynomial [5, 10]. Therefore, the new step-by decoder is less complex than the Chien's search method implemented by hardware circuits.

III. CONCLUSION

This paper presents a review on Golay code. A binary Golay code is a type of linear error-correcting code used in digital communications. The binary Golay code, along with the ternary Golay code, has a particularly deep and interesting connection to the theory of finite sporadic groups in mathematics. There are various methods for representing Golay code which are defined by numerous researchers are present in this paper.

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