	Chisel_P3 Spec	Status/Errata
Instruction set	RV64IMAFDC	✓
Privilege levels	machine, user, supervisor (SV39)	✓
Memory management	Yes	✓
Physical memory prot	Yes	✓
Compliance tests	https://github.com/riscv/riscv-tests	✓
	rv64u{i,m,a,f,d,c}-{p,v}, rv64{m,s}i-{p,v}	225 PASS, 1 FAIL - see list below
Operating system	Linux kernel	✓
Default GFE clock MHz	25	✓
Superscalar	Yes – dual issue	✓
Out-of-order	Yes	✓
ICache/DCache	32 KB	✓
Multiply-Divide unit	Yes	✓
Single/double FPU unit	Yes	✓
RISC-V debug module	RISC-V External Debug Support v0.13 system bus	✓
Interrupts (PLIC)	Chapter 8, SiFive U54-MC-RVCoreIP v1p0 16 interrupts	✓ Linux driver currently requires workaround
Timer (CLINT)	Chapter 9, SiFive U54-MC-RVCoreIP v1p0	✓ no known issues
System bus	64-bit AXI4	✓ no known issues
Implementation language	Chisel	✓

Issues	Diagnosis
rv64mi-p-csr Failing	Error in Boom processor. Does not seem to have an impact in functionality for Linux
Tandem Verification	Currently the Chisel P3 does not include tandem verification support.
Ethernet causes kernel panic	Trying to send packets over Ethernet will cause a kernel panic. These panics may be related to bugs in the Boom processor due to compressed instructions near page boundaries. We are continuing to investigate the issue.
PLIC Driver requires workaround	The SiFive Linux PLIC driver required a modification to double “claim” the first interrupt seen. Without this addition, the Linux kernel will become stuck in a loop trying to claim a phantom interrupt. We are investigating the issue and hope to have a hardware fix soon. In the meantime, no ill-effects were noticed with the software work around. The workaround is included in the current master release of the GFE