	Chisel_P2 Spec	Status/Errata
Instruction set	RV64IMAFDC	✓
Privilege levels	machine, user, supervisor (SV39)	✓
Memory management	Yes	✓
Physical memory prot	No	✓
Compliance tests	https://github.com/riscv/riscv-tests	✓
	rv64u{i,m,a,f,d,c}-{p,v}, rv64{m,s}i-{p,v}	✓ no failures
Operating system	Linux kernel	✓
Pipeline stages	5	✓
Default GFE clock MHz	50	✓
Max GFE clock MHz	150	✓
Superscalar	No	✓
Out-of-order	No	✓
ICache/DCache	8 KB	✓
Multiply-Divide unit	Yes	✓
Single/double FPU unit	Yes	✓
RISC-V debug module	RISC-V External Debug Support v0.13 system bus	✓
Interrupts (PLIC)	Chapter 8, SiFive U54-MC-RVCoreIP v1p0 16 interrupts	✓
Timer (CLINT)	Chapter 9, SiFive U54-MC-RVCoreIP v1p0	✓
System bus	64-bit AXI4	✓
Implementation language	Chisel	✓