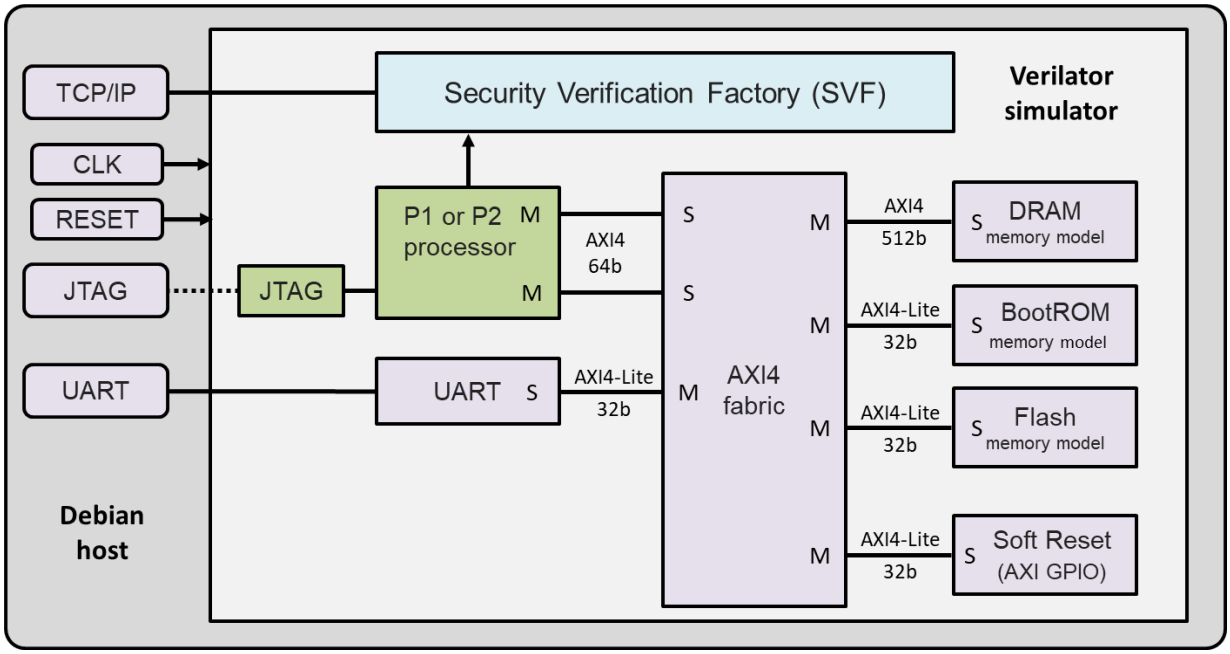
System description for standalone processor simulation



	Processor simulation	VCU118 GFE
Objective	unit-level processor debug	system-level high speed execution
Simulator	Verilator	not supported
gdb	same host software is used	
console		
Tandem verifier		
Ethernet controller	not modeled	Xilinx IP
DMA controller		
DRAM controller		
Flash controller		
UART1, SPI1, IIC0, GPIO1		
DRAM memory	Bluespec AXI4 memory models	VCU118 components
Flash memory		
Boot ROM	Bluespec compiled Verilog	Xilinx IP
AXI4 fabric		
UART		
JTAG		
Soft reset		
SVF block	Bluespec compiled Verilog	