

	Bluespec_P3 Spec	Status/Errata
Instruction set	RV64IMAFDC	✓
Privilege levels	machine, user, supervisor (SV39)	✓
Memory management	Yes	✓
Physical memory prot	No	✓
Compliance tests	<a href="https://github.com/riscv/riscv-tests">https://github.com/riscv/riscv-tests</a>	✓
	rv64u{i,m,a,f,d,c}-{p,v}, rv64{m,s}i-{p,v}	202 PASS, 27 FAIL - see list below
Operating system	Linux kernel	testing
Pipeline stages	5	✓
Default GFE clock MHz	24	✓
Max GFE clock MHz	24	no plan to attempt optimization
Superscalar	Yes – dual issue	✓
Out-of-order	Yes	✓
ICache/DCache	16 KB	✓
Multiply-Divide unit	Yes	✓
Single/double FPU unit	Yes	✓
RISC-V debug module	RISC-V External Debug Support v0.13 system bus	debugging minimal gdb functionality future: brk-pts and single-step errata: can't boot from Flash yet
Interrupts (PLIC)	Chapter 8, SiFive U54-MC-RVCoreIP v1p0 16 interrupts	✓ no known issues
Timer (CLINT)	Chapter 9, SiFive U54-MC-RVCoreIP v1p0	✓ no known issues
System bus	64-bit AXI4	✓ no known issues
Implementation language	BSV	✓

Failing ISA test	Diagnosis
System instructions: rv64mi-p-csr rv64si-p-dirty rv64mi-p-illegal	No accurate diagnoses yet, although some symptoms look similar to what we saw with earlier processors (these test various corner-cases of system instructions).  Target date for fix: 2019-Apr-15
'F' and 'D' instructions rv64uf-{p,v}-add rv64uf-{p,v}-fcmp rv64uf-{p,v}-fdiv rv64uf-{p,v}-fmin rv64ud-{p,v}-add rv64ud-{p,v}-fcmp rv64ud-{p,v}-fdiv rv64ud-{p,v}-fmadd rv64ud-{p,v}-fmin rv64ud-{p,v}-ldst rv64ud-{p,v}-move	These are simulation-only errors. Simulation uses some quick-and-dirty floating-point "model" modules written by the MIT authors, which are not accurate. All the errors seem to be regarding incomplete treatment of NaNs in the models. These errors should not happen in FPGA since those use Xilinx IP modules instead. MIT has been booting Linux with the Xilinx IP modules, lending more confidence in the FPGA version.  The actual number of root-cause failures is likely to be smaller than the list. For example, the 'fadd' test has four variants: {uf/ud} x {-p/-v-}; they all likely need common fix.  Target date: 2019-Apr-30