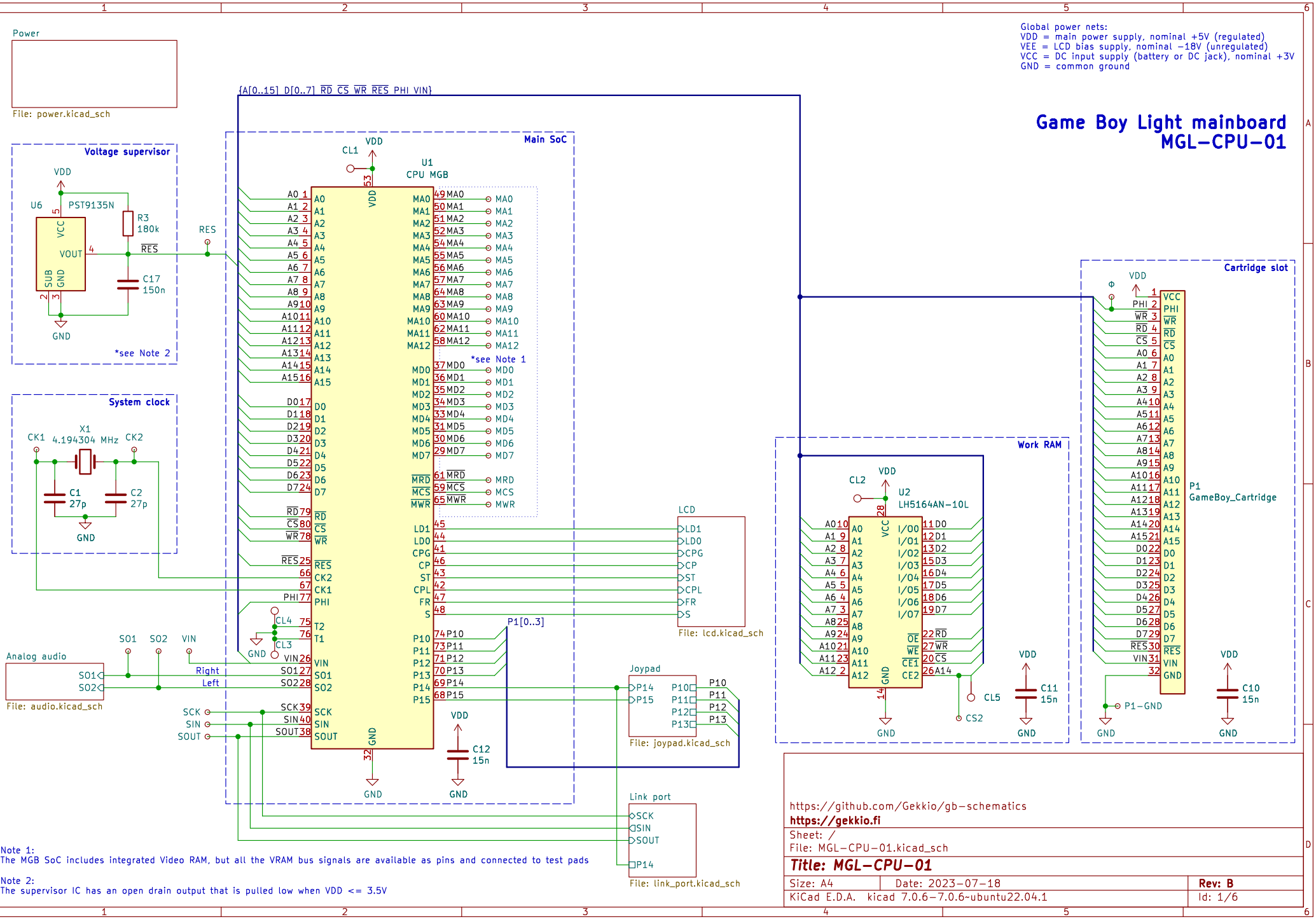
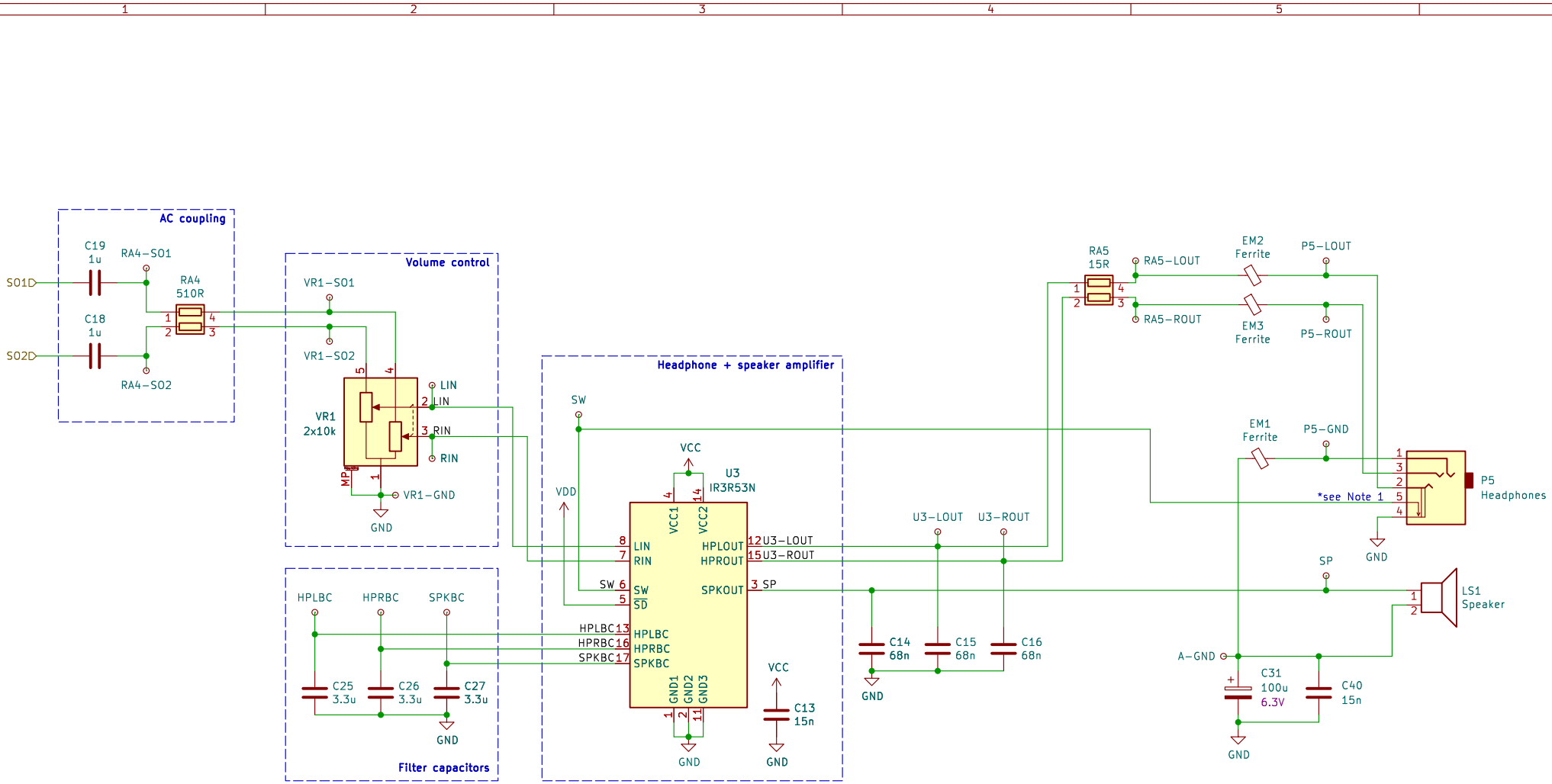

Power
File: power.kicad_sch
Global power nets:
VDD = main power supply, nominal +5V (regulated)
VEE = LCD bias supply, nominal −18V (unregulated)
VCC = DC input supply (battery or DC jack), nominal +3V
GND = common ground
{A[0..15] D[0..7] RD CS WR RES PHI VIN}
Game Boy Light mainboard
MGL−CPU−01
Voltage supervisor
U6
PST9135N
R3
180k
C17
150n
RES
*see Note 2
System clock
X1
4.194304 MHz
CK1
CK2
C1
27p
C2
27p
Main SoC
U1
CPU MGB
CL1
*see Note 1
P1[0..3]
LCD
File: lcd.kicad_sch
Work RAM
U2
LH5164AN−10L
CL2
CS2
C11
15n
Cartridge slot
P1
GameBoy_Cartridge
P1−GND
C10
15n
Analog audio
File: audio.kicad_sch
Right
Left
SCK
SIN
SOUT
C12
15n
Joypad
File: joypad.kicad_sch
Link port
File: link_port.kicad_sch
Note 1:
The MGB SoC includes integrated Video RAM, but all the VRAM bus signals are available as pins and connected to test pads
Note 2:
The supervisor IC has an open drain output that is pulled low when VDD <= 3.5V
https://github.com/Gekkio/gb−schematics
https://gekkio.fi
Sheet: /
File: MGL−CPU−01.kicad_sch
Title: MGL−CPU−01
Size: A4
Date: 2023−07−18
Rev: B
KiCad E.D.A. kicad 7.0.6−7.0.6~ubuntu22.04.1
Id: 1/6



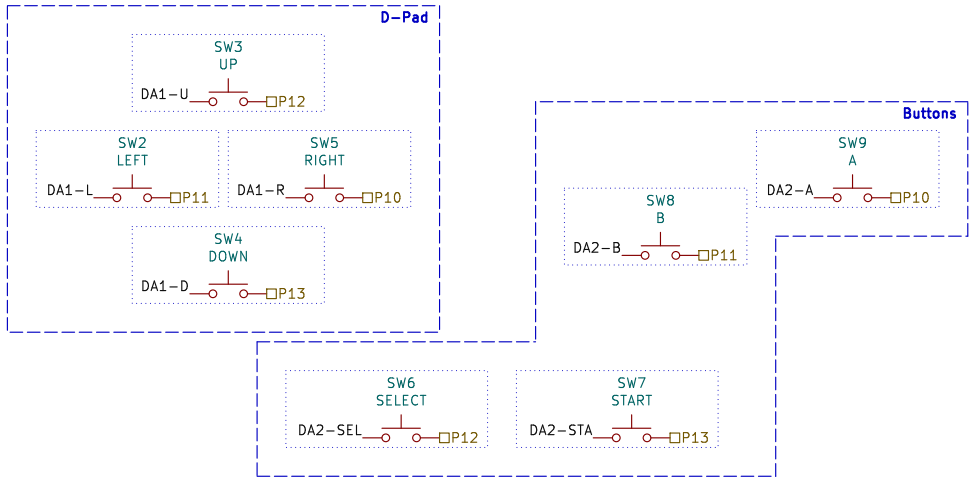

Note 1:
Pins 4 (GND) and 5 (SW) are normally connected, and inserting a plug disconnects SW from GND.

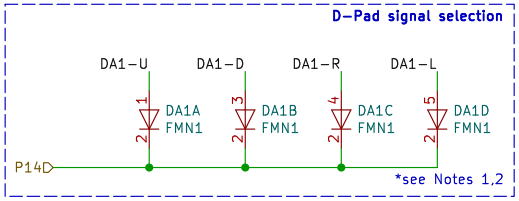
https://github.com/Gekkio/gb-schematics
**https://gekkio.fi**

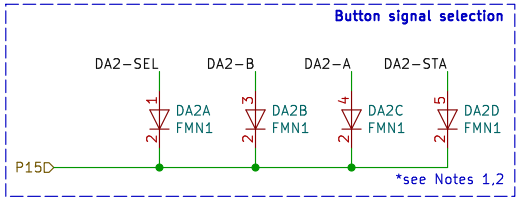
Sheet: /Analog audio/
File: audio.kicad_sch

***Title: MGL-CPU-01***

| Size: A4 | Date: 2023-07-18 | **Rev: B** |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-7.0.6~ubuntu22.04.1 | | Id: 2/6 |




Note 1:
Some boards use Panasonic MA6X124 (SOT-23-6 footprint) instead of Rohm FMN1 (SOT-23-5 footprint)
The SOT-23-6 footprint on the board is compatible with both

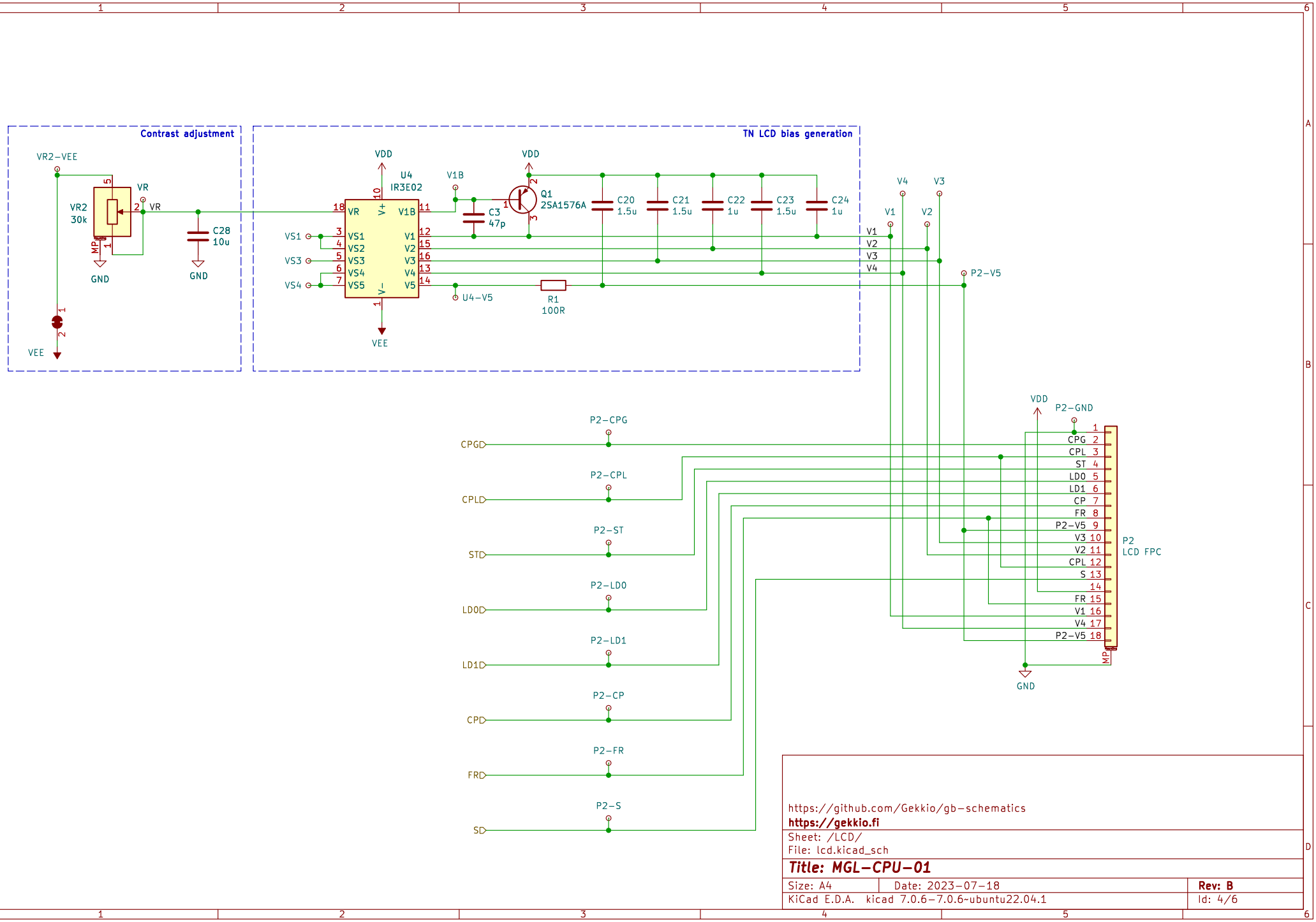
Note 2:
Warning: MA6X124 and FMN1 datasheets use non-standard pin numbering!
This schematic uses standard SOT-23-5/SOT-23-6 numbering

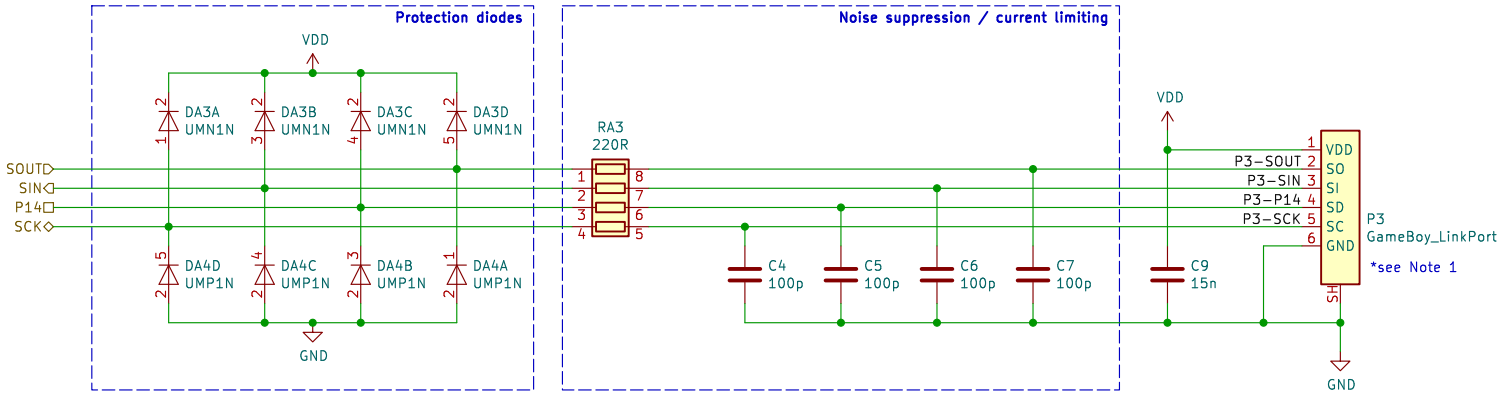
https://github.com/Gekkio/gb-schematics
**https://gekkio.fi**

Sheet: /Joypad/
File: joypad.kicad_sch

***Title: MGL-CPU-01***

| Size: A4 | Date: 2023-07-18 | **Rev: B** |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-7.0.6~ubuntu22.04.1 | | Id: 3/6 |


Contrast adjustment
VR2-VEE
VR2
30k
VR
C28
10u
GND
VEE
TN LCD bias generation
VDD
U4
IR3E02
V1B
C3
47p
Q1
2SA1576A
C20
1.5u
C21
1.5u
C22
1u
C23
1.5u
C24
1u
VS1
VS2
VS3
VS4
VS5
V1
V2
V3
V4
V5
U4-V5
R1
100R
P2-V5
P2-CPG
P2-CPL
P2-ST
P2-LD0
P2-LD1
P2-CP
P2-FR
P2-S
P2-GND
CPG
CPL
ST
LD0
LD1
CP
FR
S
P2
LCD FPC
https://github.com/Gekkio/gb-schematics
https://gekkio.fi
Sheet: /LCD/
File: lcd.kicad_sch
Title: MGL-CPU-01
Size: A4
Date: 2023-07-18
Rev: B
KiCad E.D.A. kicad 7.0.6-7.0.6~ubuntu22.04.1
Id: 4/6



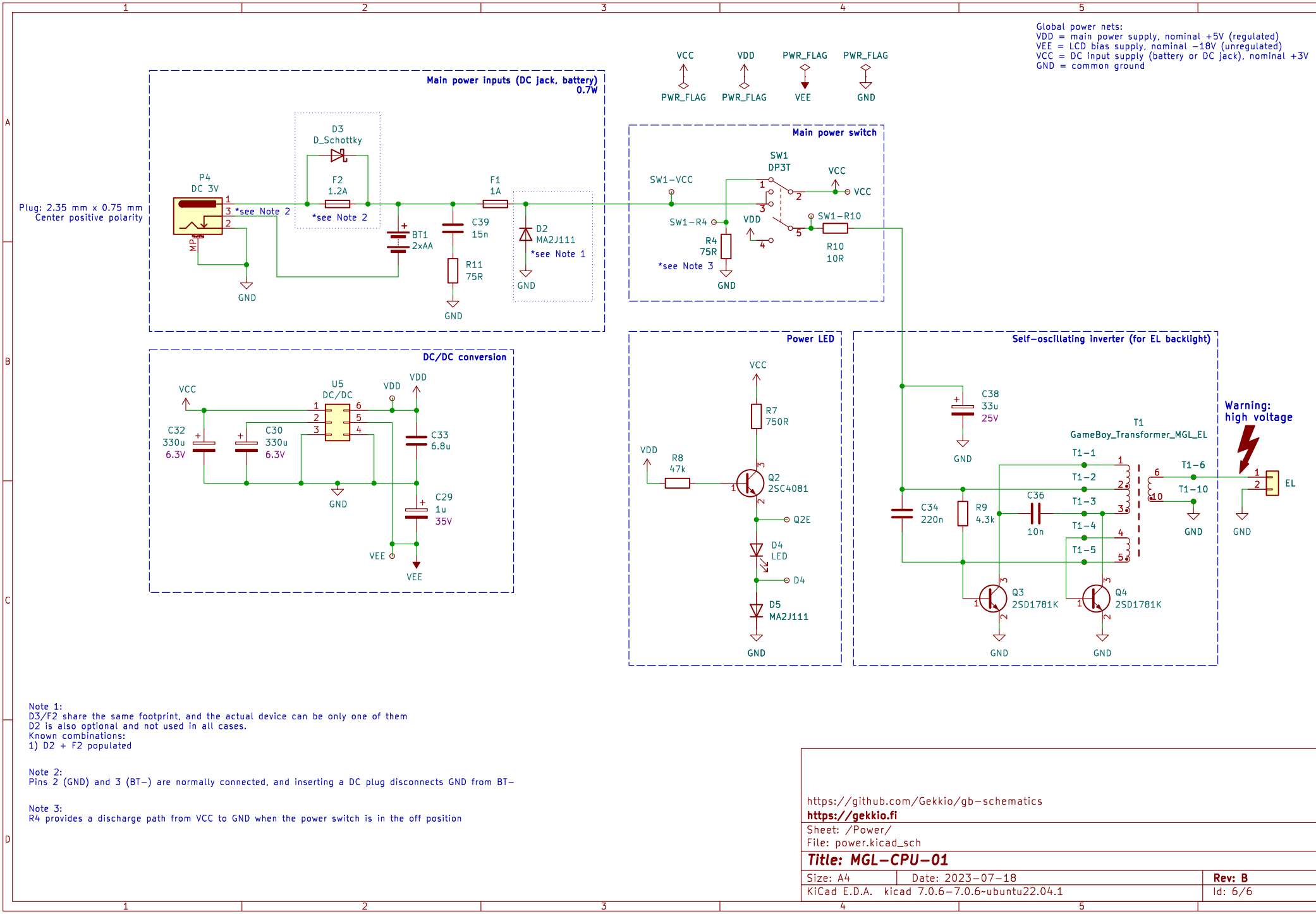

Note 1:
Official link cables omit pin 1 (VDD) and pin 4 (P14/SD), but unofficial cables usually have all 6 signals with VDD/SD crossed

https://github.com/Gekkio/gb-schematics
**https://gekkio.fi**

Sheet: /Link port/
File: link_port.kicad_sch

**Title: MGL-CPU-01**

| Size: A4 | Date: 2023-07-18 | **Rev: B** |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-7.0.6~ubuntu22.04.1 | | Id: 5/6 |




Note 1:
D3/F2 share the same footprint, and the actual device can be only one of them
D2 is also optional and not used in all cases.
Known combinations:
1) D2 + F2 populated

Note 2:
Pins 2 (GND) and 3 (BT−) are normally connected, and inserting a DC plug disconnects GND from BT−

Note 3:
R4 provides a discharge path from VCC to GND when the power switch is in the off position

https://github.com/Gekkio/gb−schematics
**https://gekkio.fi**

Sheet: /Power/
File: power.kicad_sch

***Title: MGL−CPU−01***

| Size: A4 | Date: 2023−07−18 | **Rev: B** |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6−7.0.6~ubuntu22.04.1 | | Id: 6/6 |