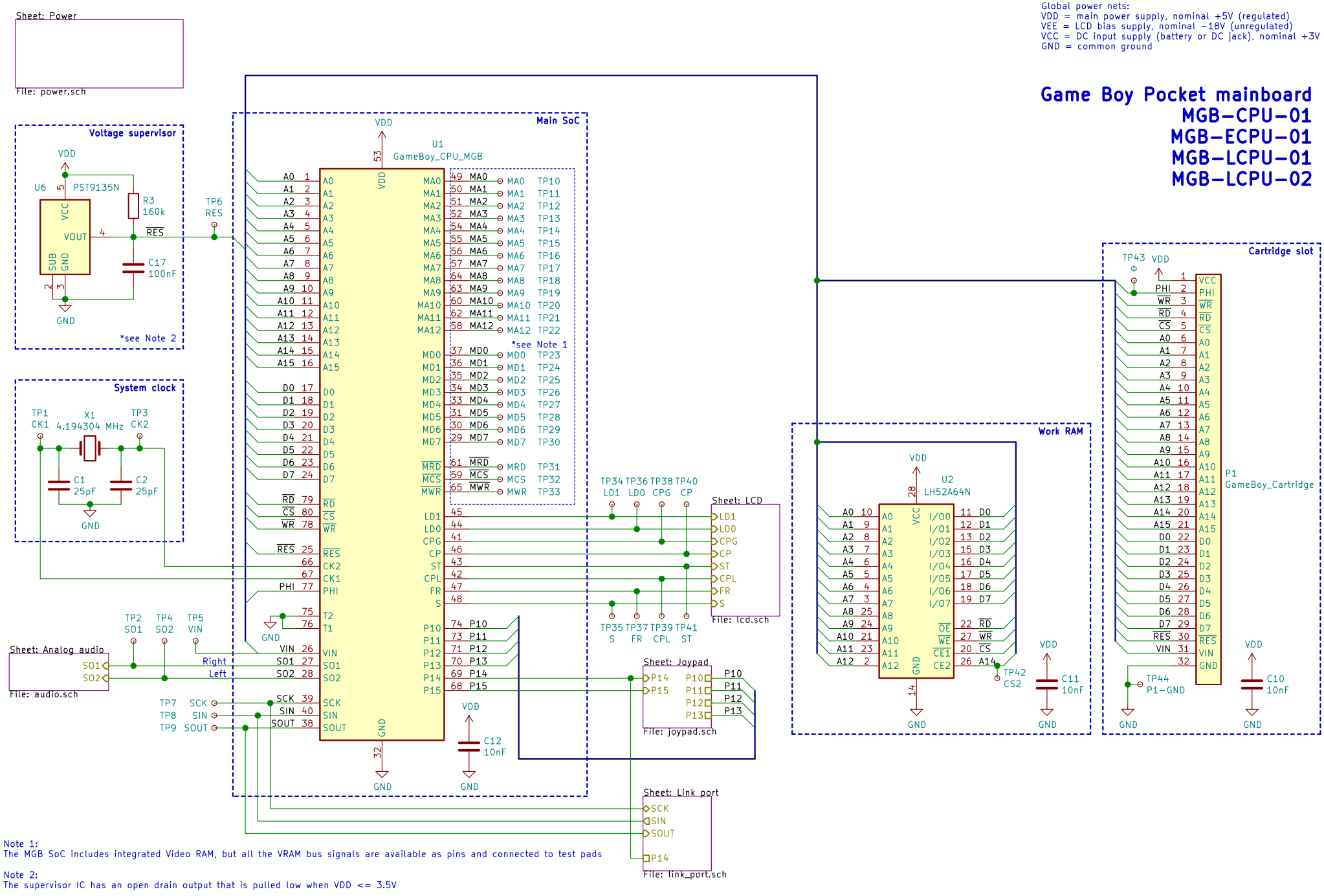
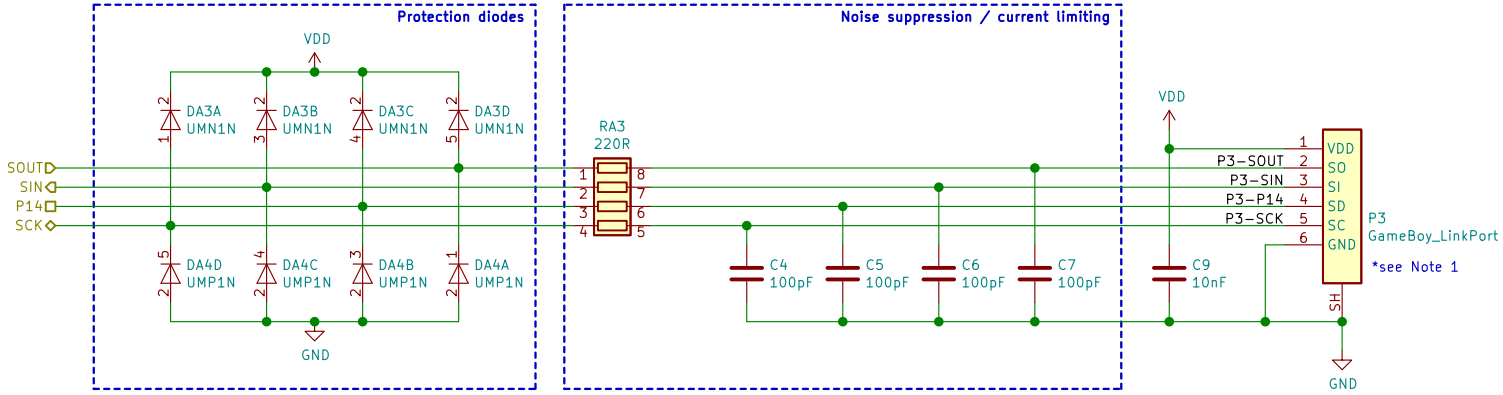
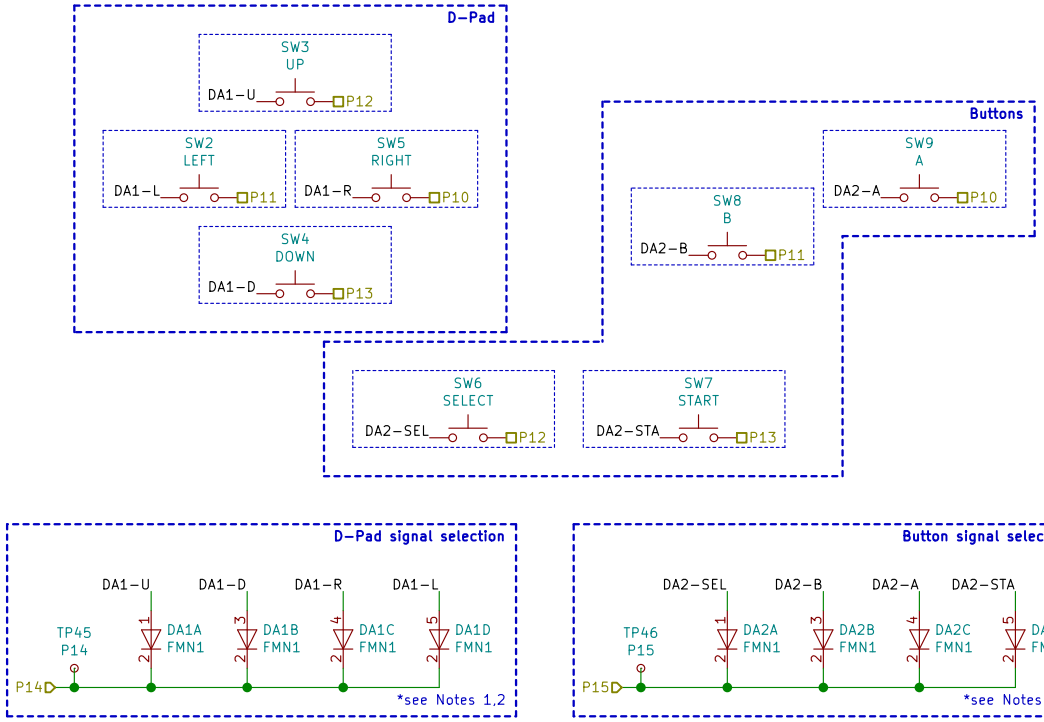

Global power nets:
VDD = main power supply, nominal +5V (regulated)
VEE = LCD bias supply, nominal −18V (unregulated)
VCC = DC input supply (battery or DC jack), nominal +3V
GND = common ground
Game Boy Pocket mainboard
MGB−CPU−01
MGB−ECPU−01
MGB−LCPU−01
MGB−LCPU−02
Sheet: Power
File: power.sch
Voltage supervisor
U6 PST9135N
R3 160k
C17 100nF
*see Note 2
TP6 RES
System clock
X1 4.194304 MHz
C1 25pF
C2 25pF
TP1 CK1
TP3 CK2
Main SoC
U1 GameBoy_CPU_MGB
*see Note 1
Work RAM
U2 LH52A64N
C11 10nF
TP42 CS2
Cartridge slot
P1 GameBoy_Cartridge
TP43 Φ
TP44 P1−GND
C10 10nF
Sheet: LCD
File: lcd.sch
Sheet: Joypad
File: joypad.sch
Sheet: Analog audio
File: audio.sch
Sheet: Link port
File: link_port.sch
C12 10nF
Note 1:
The MGB SoC includes integrated Video RAM, but all the VRAM bus signals are available as pins and connected to test pads
Note 2:
The supervisor IC has an open drain output that is pulled low when VDD <= 3.5V

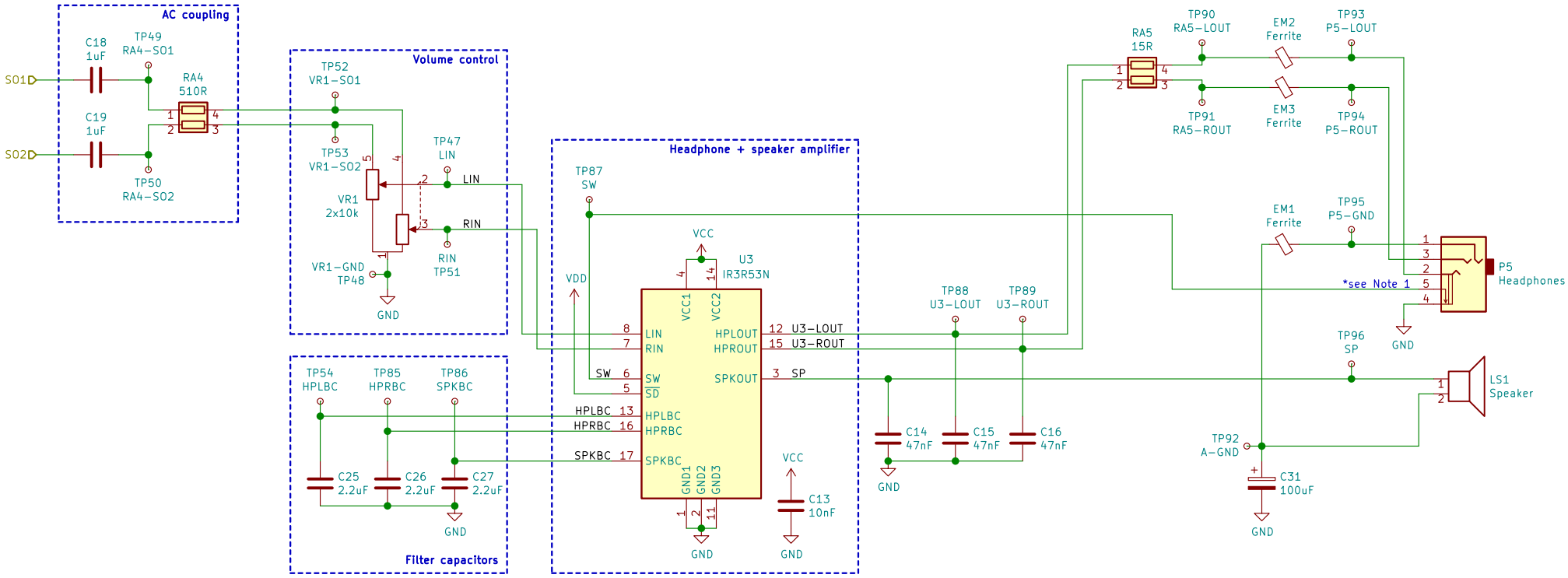


Note 1:
Official link cables omit pin 1 (VDD) and pin 4 (P14/SD), but unofficial cables usually have all 6 signals with VDD/SD crossed



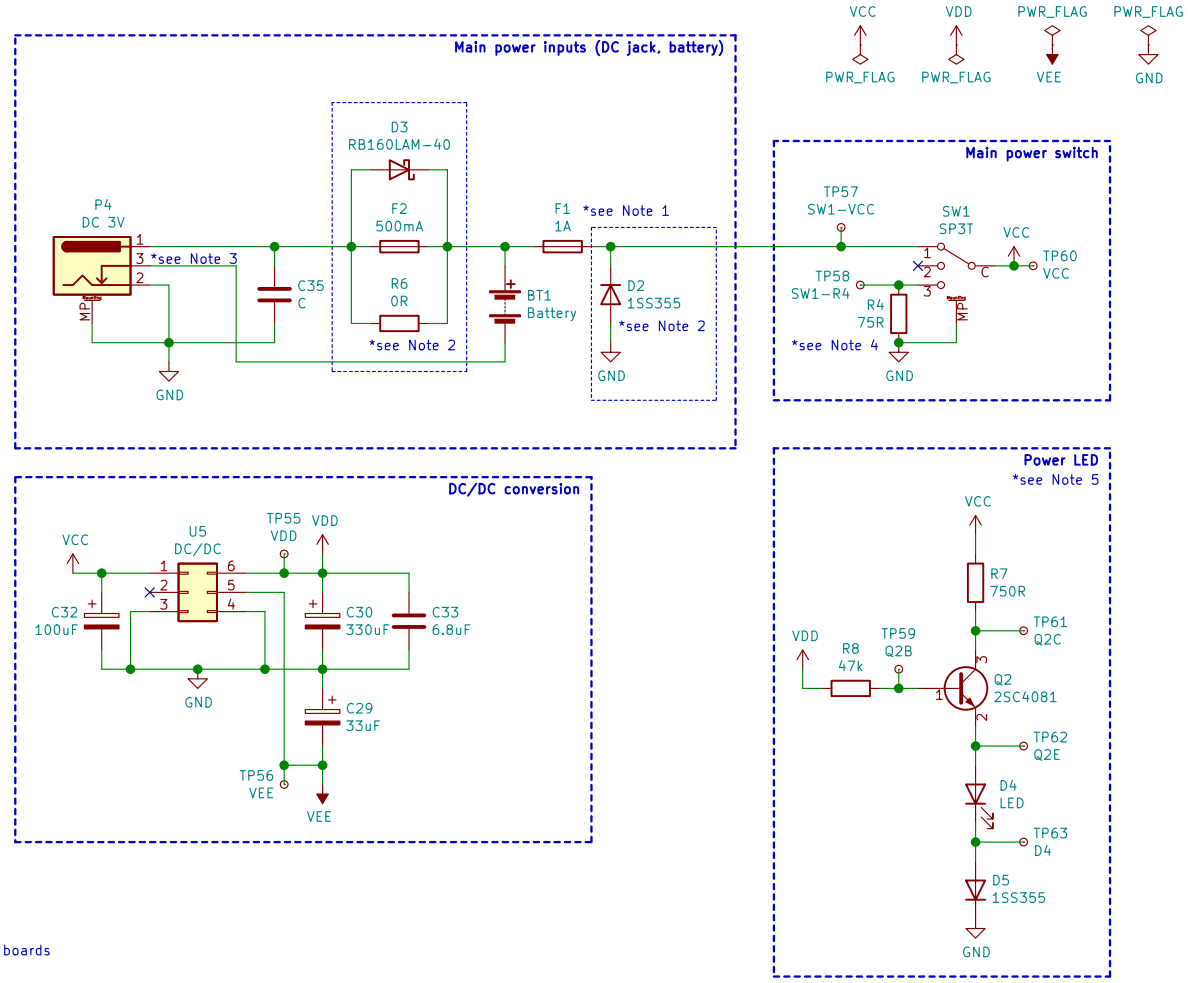
Note 1:
Earlier boards use Panasonic MA6X124 (SOT-23-6 footprint) instead of Rohm FMN1 (SOT-23-5 footprint)
The SOT-23-6 footprint on the board is compatible with both

Note 2:
Warning: MA6X124 and FMN1 datasheets use non-standard pin numbering!
This schematic uses standard SOT-23-5/SOT-23-6 numbering



Note 1:
Pins 4 (GND) and 5 (SW) are normally connected, and inserting a plug disconnects SW from GND.

Global power nets:
VDD = main power supply, nominal +5V (regulated)
VEE = LCD bias supply, nominal −18V (unregulated)
VCC = DC input supply (battery or DC jack), nominal +3V
GND = common ground



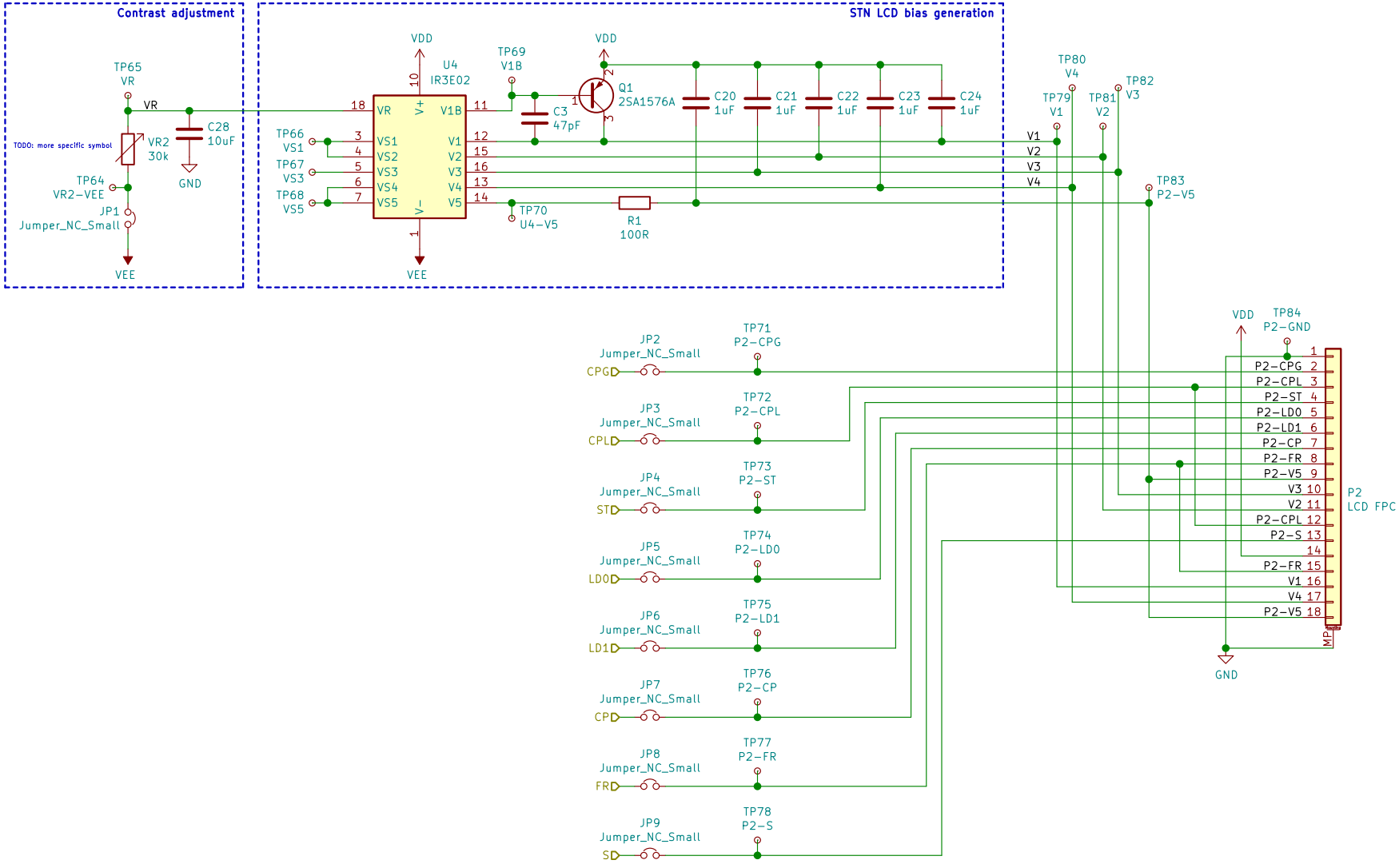
Note 1:
F1 is 600mA on earlier boards

Note 2:
D3/F2/R6 share the same footprint, and the actual device can be only one of them
D2 is also optional and not used in all cases.
Known combinations:
1) only D2 populated, no D3/F2/R6
2) D2 + R6 populated
3) D2 + F2 populated
4) only D3 populated, no D2

Note 3:
Pins 2 (GND) and 3 (BT−) are normally connected, and inserting a DC plug disconnects GND from BT−

Note 4:
R4 provides a discharge path from VCC to GND when the power switch is in the off position

Note 5:
Power LED circuit is not present on early MGB−CPU−01 boards


Contrast adjustment
TP65
VR
VR
C28
10uF
TODO: more specific symbol
VR2
30k
GND
TP64
VR2-VEE
JP1
Jumper_NC_Small
VEE
STN LCD bias generation
VDD
U4
IR3E02
TP69
V1B
VDD
Q1
2SA1576A
C20
1uF
C21
1uF
C22
1uF
C23
1uF
C24
1uF
TP80
V4
TP79
V1
TP81
V2
TP82
V3
TP66
VS1
TP67
VS3
TP68
VS5
18 VR
3 VS1
4 VS2
5 VS3
6 VS4
7 VS5
10 V+
1 V-
11 V1B
12 V1
15 V2
16 V3
13 V4
14 V5
C3
47pF
TP70
U4-V5
R1
100R
V1
V2
V3
V4
TP83
P2-V5
JP2
Jumper_NC_Small
CPG
TP71
P2-CPG
JP3
Jumper_NC_Small
CPL
TP72
P2-CPL
JP4
Jumper_NC_Small
ST
TP73
P2-ST
JP5
Jumper_NC_Small
LD0
TP74
P2-LD0
JP6
Jumper_NC_Small
LD1
TP75
P2-LD1
JP7
Jumper_NC_Small
CP
TP76
P2-CP
JP8
Jumper_NC_Small
FR
TP77
P2-FR
JP9
Jumper_NC_Small
S
TP78
P2-S
VDD
TP84
P2-GND
1
P2-CPG 2
P2-CPL 3
P2-ST 4
P2-LD0 5
P2-LD1 6
P2-CP 7
P2-FR 8
P2-V5 9
V3 10
V2 11
P2-CPL 12
P2-S 13
14
P2-FR 15
V1 16
V4 17
P2-V5 18
MP
P2
LCD FPC
GND