Logic Design & Computer Organization Lab

Assignment 1 - IC Testing

Name : Gopal Saraf

Class : SE 09

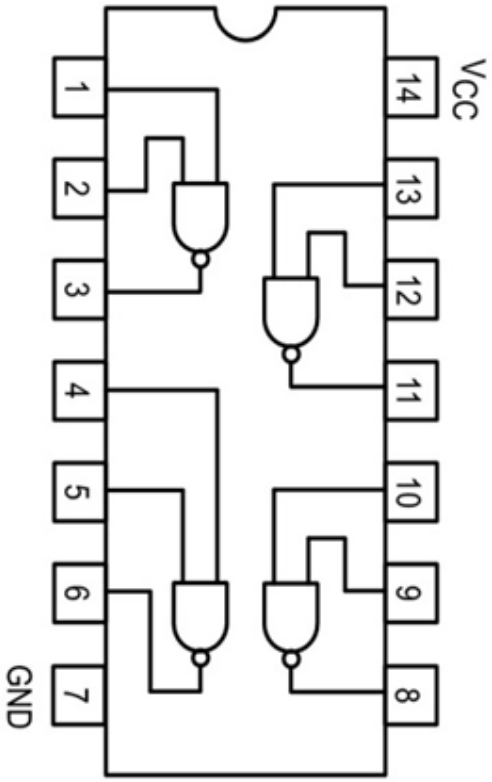
Batch : H9

Roll No : 23168

74HC00

NAND GATE

Pin Assignments



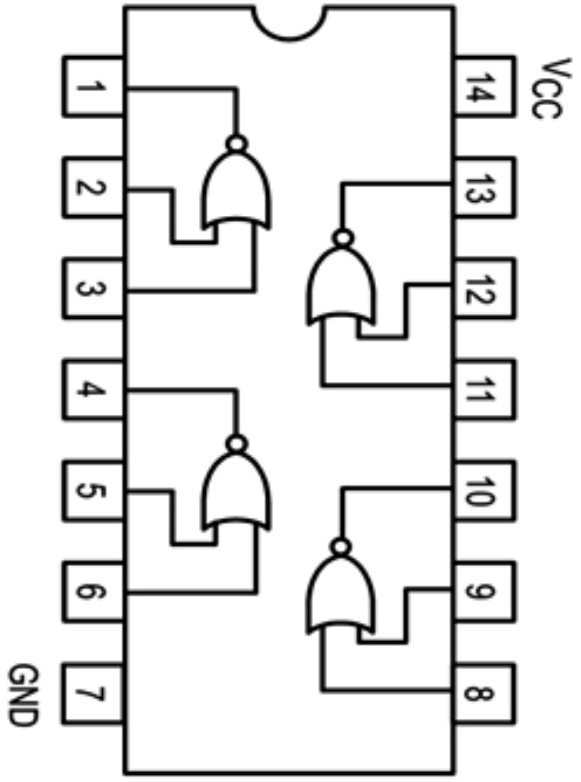
Truth Table

Input		Output
A	B	Y= $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

74HC02

NOR GATE

Pin Assignments



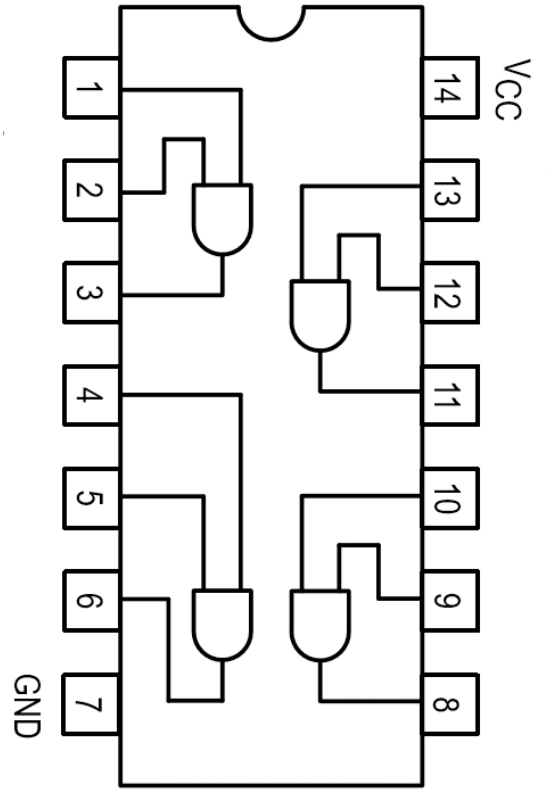
Truth Table

Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

74HC08

AND GATE

Pin Assignments



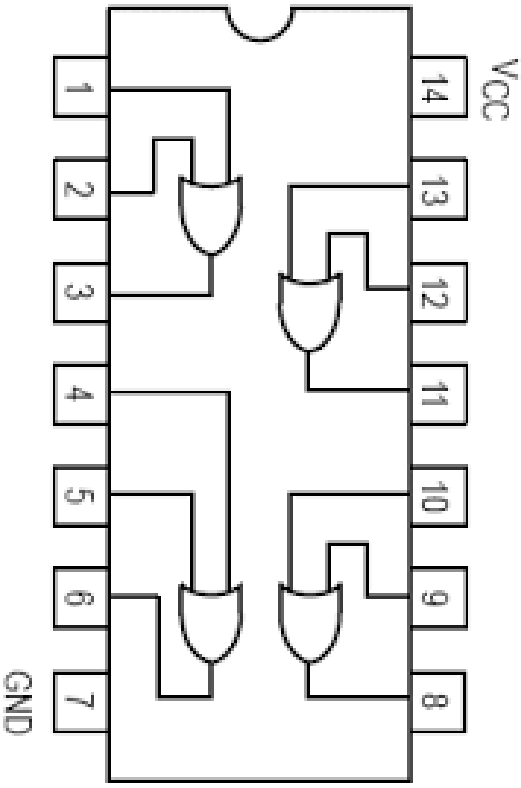
Truth Table

Input		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

74HC32

OR GATE

Pin Assignments



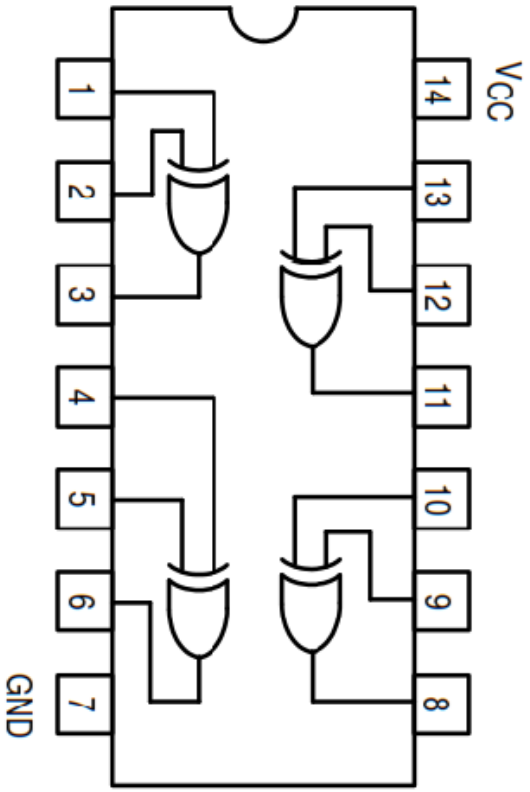
Truth Table

Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

74HC86

XOR GATE

Pin Assignments



Truth Table

INPUTS		OUTPUT
a	b	A XOR B
0	0	0
1	0	1
0	1	1
1	1	0

Tinkercad Circuit :