QN902x Hardware Application Note

Version 0.8

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1. Introduction

QN902x is an ultra low power, high performance and highly integrated Bluetooth Low Energy (BLE) SOC with few external components.

1.1 Purpose

This document is the application note for hardware design with QN902x.

2. Hardware design

2.1 Power supply

The QN902x has integrated a voltage regulator. So there are two typical solutions for QN902x power supply connection.

2.1.1 Using external power supply directly

If using external power supply directly, all the QN902x power pins should be connected to the external power supply source. Please refer to schematic in figure10 or figure12. And the voltage range should be between 2.4V~3.6V. To keep the best performance the 100nF decupling capacitors should be connected to the power supply pins and suggested a 10uF capacitor to be connected to pin1 of QN9020 to filter ripple of power supply pin.

2.1.2 Using internal DC-DC converter

Using internal integrated DC-DC converter can be utilized to further reduce the current consumption. The DC-DC converter generates the internal required voltage from VCC (pin1 in QN902x) and output the voltage at the DCC pin (pin48 in QN9020 or pin32 in QN9021). The DCC pin connects the DC–DC converter circuit to supply the voltage for QN9020 three power pins (VDD1、VDD2、VDD3). The figure1 shows the DCC pin (pin48 in QN9020 or pin32 in QN9021) connection in schematic.

The DCC pin needs a 10uH inductor and a 15nH inductor in series then a 1uF decupling capacitor in parallel. The 15nH inductor and the 1uF decupling capacitor are used to filtering the noise from DC-DC converter. All the three components should place close to the DCC pin.

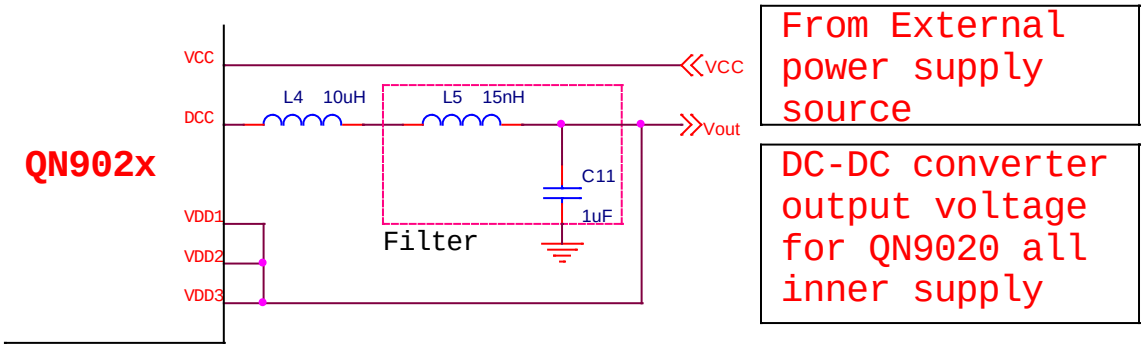

Figure 1 Using internal integrated DC-DC converter reference schematic

2.2 Clocks

Two clocks are required by the QN902x, there are the 16/32 MHz high frequency clock and 32.768 KHz low frequency clock (RTC).

2.2.1 High frequency clock

A high frequency crystal is utilized to provide the system clock, which accepts16/32-MHz external crystal with ±50ppm accuracy. Higher accuracy can easier successfully to send or receive packets. If possible, suggested using the 20ppm accuracy crystal. The QN902x has integrated crystal load capacitances. The parameters for selecting the crystals show in the table below.

Table 1 High Frequency Crystal Selection

Frequency	Accuracy	Load capacitance	Equivalent Series Resistance max(Ω)
16/32MHz	<±50ppm	8pF	50

QN902x also accepts external clock inputs.

- Square clock. For Square wave as clock input, the voltage range is between 0~VCC.
- Sin wave. For sin wave as clock input, the voltage should be larger than 350mVpeak and it should be AC coupling.

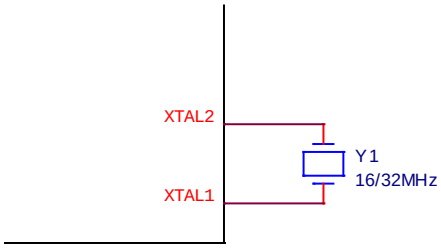

Figure 2 Crystal input interface with no external load capacitance

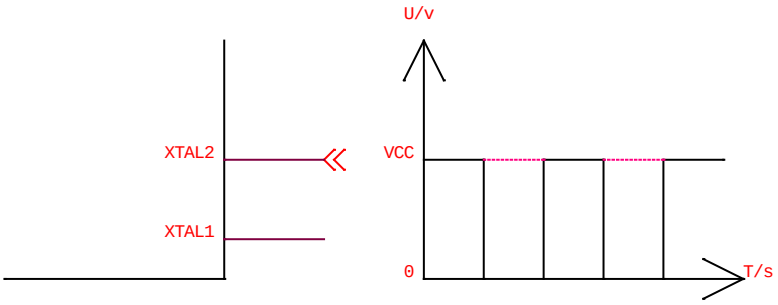

Figure 3 External square wave clock input interface

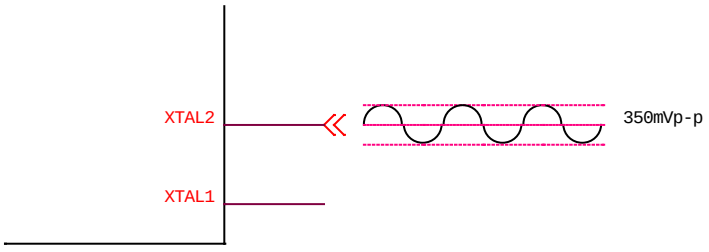

Figure 4 External sin wave clock input interface

2.2.2 Low frequency clock

- The external 32.768-kHz crystal is used when the accurate timing is needed.
- The 32-kHz internal RC oscillator can be used in order to reduce the cost and the power consumption in case it needn't the accurate timing.

The parameters for selecting external 32.768 KHz crystal are shown in follows table2. The recommend accuracy is 20ppm.

Table 2 Low Frequency Crystal Selection

Frequency	Accuracy
32.768KHz	<±100ppm

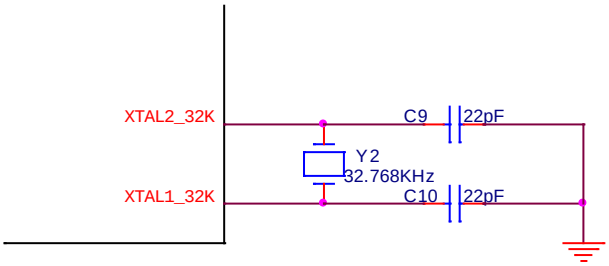

Figure 5 32.768 KHz crystal circuit

2.3 Reset circuit

The reset pin of QN902x is RSTN. It is logic low for reset, for normal using it should be connected to logic high. This pin is suggested to connect with an RC reset circuit for power on reset. The recommended values for the resistor(Rres) and the capacitor(Cres) should be 100kΩ and 1uF.

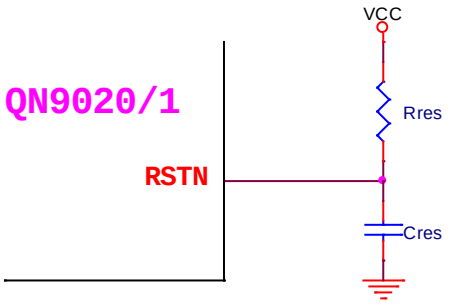

Figure 6 RC reset circuit

2.4 GPIO's define

Pin_ctrl	0	1	2	3	pin num
[1:0]	GPIO0	UART0_TXD	SPI0_DAT	RSVD	P0_0
[3:2]	GPIO1	RSVD	SPI0_CS0	UART0_CTSn	P0_1
[5:4]	GPIO2	I2C_SDA	SPI0_CLK	UART0_RTSn	P0_2
[7:6]	GPIO3	RSVD	CLKOUT0	TIMER0_eclk	P0_3
[9:8]	GPIO4	RSVD	CLKOUT1	RSVD	P0_4
[11:10]	GPIO5	I2C_SCL	ADC Trig	ACMP1_out	P0_5
[13:12]	SW_DAT	GPIO6	AIN2	ACMP1-	P0_6
[15:14]	SW_CLK	GPIO7	AIN3	ACMP1+	P0_7
[17:16]	GPIO8	SPI1_DIN	UART1_RXD	TIMER2_eclk	P1_0
[19:18]	GPIO9	SPI1_DAT	UART1_TXD	TIMER1_0_out	P1_1
[21:20]	GPIO10	SPI1_CS0	UART1_CTSn	ADC Trig	P1_2
[23:22]	GPIO11	SPI1_CLK	UART1_RTSn	CLKOUT1	P1_3
[25:24]	GPIO12	RSVD	RSVD	TIMER1_3	P1_4
[27:26]	GPIO13	RSVD	PWM1	TIMER1_2	P1_5
[29:28]	GPIO14	SPI0_CS1	PWM0	TIMER0_3	P1_6
[31:30]	GPIO15	UART0_RXD	SPI0_DIN	TIMER0_0	P1_7
[33:32]	GPIO16	SPI1_DIN	UART1_RXD	TIMER3_2	P2_0
[35:34]	GPIO17	SPI1_DAT	UART1_TXD	TIMER3_1	P2_1
[37:36]	GPIO18	SPI1_CLK	UART1_RTSn	TIMER2_3	P2_2
[39:35]	GPIO19	I2C_SDA	ACMP0_out	TIMER3_0	P2_3
[41:40]	GPIO20	I2C_SCL	PWM1	TIMER3_eclk	P2_4
[43:42]	GPIO21	SPI1_CS1	RSVD	TIMER2_2	P2_5
[44:43]	GPIO22	RSVD	PWM1	TIMER2_0	P2_6
[46:45]	GPIO23	ACMP1	PWM0	TIMER1_eclk	P2_7
[48:47]	GPIO24	TIMER2_1	AIN0	ACMP0-	P3_0
[50:49]	GPIO25	TIMER0_2	AIN1	ACMP0+	P3_1
[52:51]	GPIO26	SPI0_DIN	RSVD	ACMP0_out	P3_2
[54:53]	GPIO27	SPI0_DAT	CLKOUT0	RSVD	P3_3
[56:55]	GPIO28	SPI0_CLK	RSVD	RSVD	P3_4
[58:57]	GPIO29	SPI0_CS0	RSVD	TIMER0_0	P3_5
[60:59]	GPIO30	SPI1_CS0	UART1_CTSn	RSVD	P3_6

Most of the GPIOs have four defined function and swap using register's control.
Only P0_0 to P1_7 can be used as wakeup source.
From the table it can see only the red part are shared with QN9021 QFN5x5 package.

2.5 RF matching circuit

The QN902x radio transceiver requires a matching network to match the 50 ohm impedance. The structure of the matching network shows as figure 7 and figure 8. All the values on the matching network, please follows the BOM list Table 3 and Table 4.

The components of the matching network should place to the pins as close as possible.

The 50ohm RF trace between the antennas or SMA connectors and matching circuit should be as short as possible

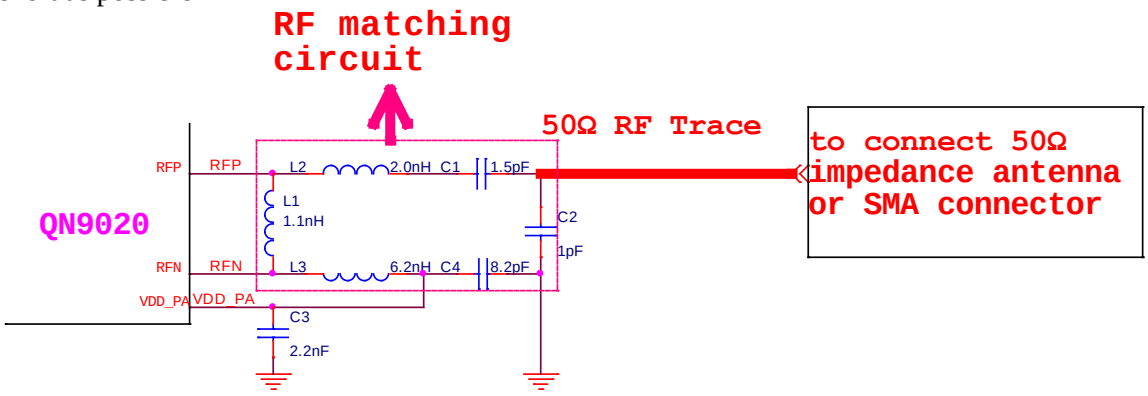

Figure 7 QN9020 RF matching circuit

Table 3 QN9020 RF matching components value

Part name	Part number	Value	Size
Inductor L1	LQP15MN1N1B02	1.1nH	0402
Inductor L2	LQP15MN2N0B02	2.0nH	0402
Inductor L3	LQP15MN6N2B02	6.2nH	0402
Capacitor C1	GRM1555C1H1R5CA01	1.5pF	0402
Capacitor C2	GRM1555C1H1R0CA01	1.0pF	0402
Capacitor C4	GRM1555C1H8R2DA01	8.2pF	0402
Capacitor C3	GRM155R71H222KA01	2.2nF	0402

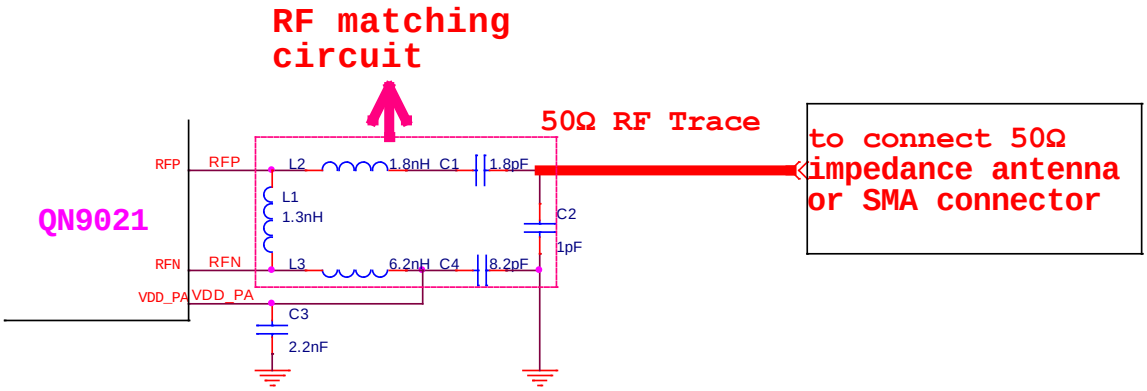

Figure 8 QN9021 RF matching circuit

Table 4 QN9021 RF matching components value

Part name	Part number	Value	Size
Inductor L1	LQP15MN1N3B02	1.3nH	0402
Inductor L2	LQP15MN1N8B02	1.8nH	0402
Inductor L3	LQP15MN6N2B02	6.2nH	0402
Capacitor C1	GRM1555C1H1R8CA01	1.8pF	0402
Capacitor C2	GRM1555C1H1R0CA01	1.0pF	0402
Capacitor C4	GRM1555C1H8R2DA01	8.2pF	0402
Capacitor C3	GRM155R71H222KA01	2.2nF	0402

2.6 AN Hardware reference design

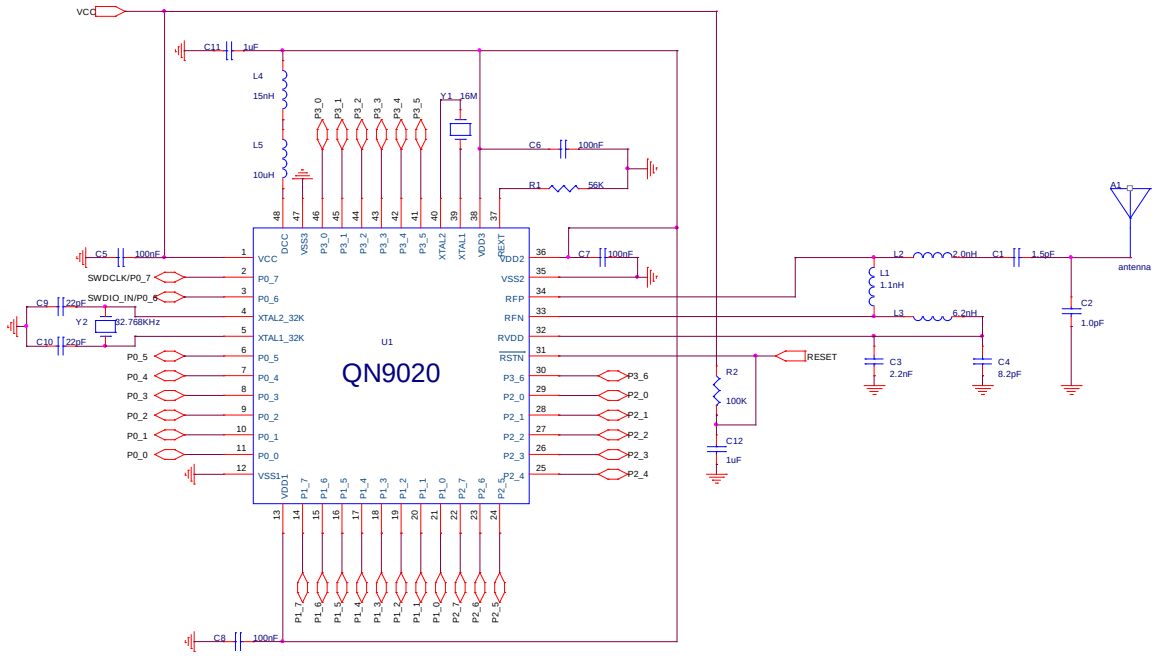

Figure 9 QN9020 with DC-DC converter reference design schematic

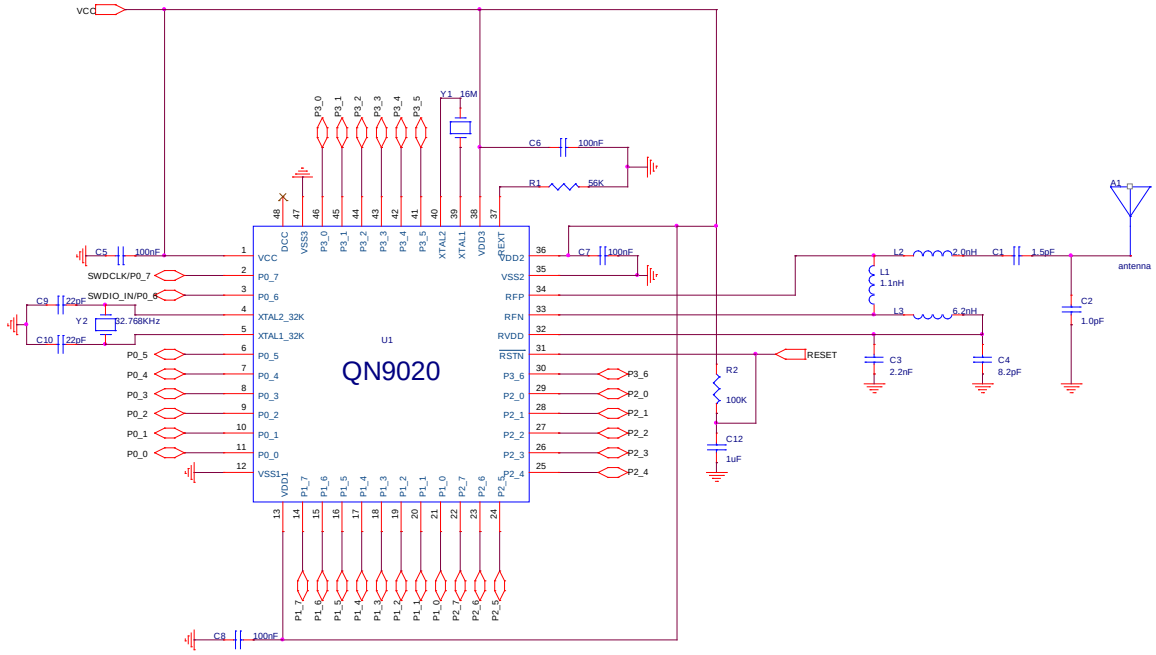

Figure 10 QN9020 without DC-DC converter reference design schematic

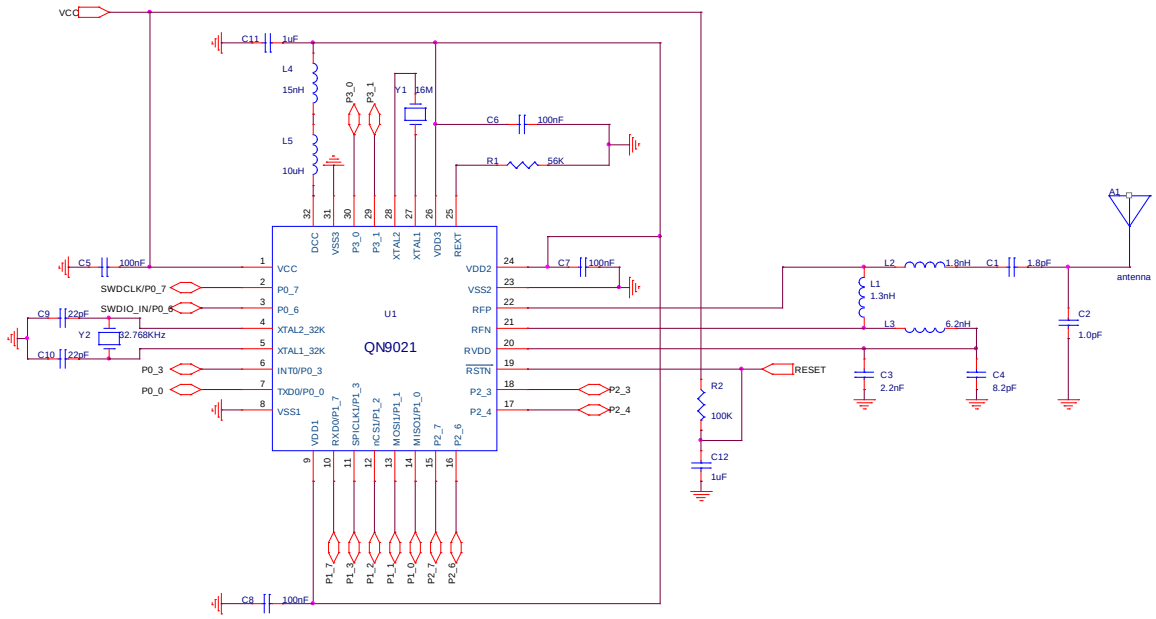

Figure 11 QN9021 with DC-DC converter reference design schematic

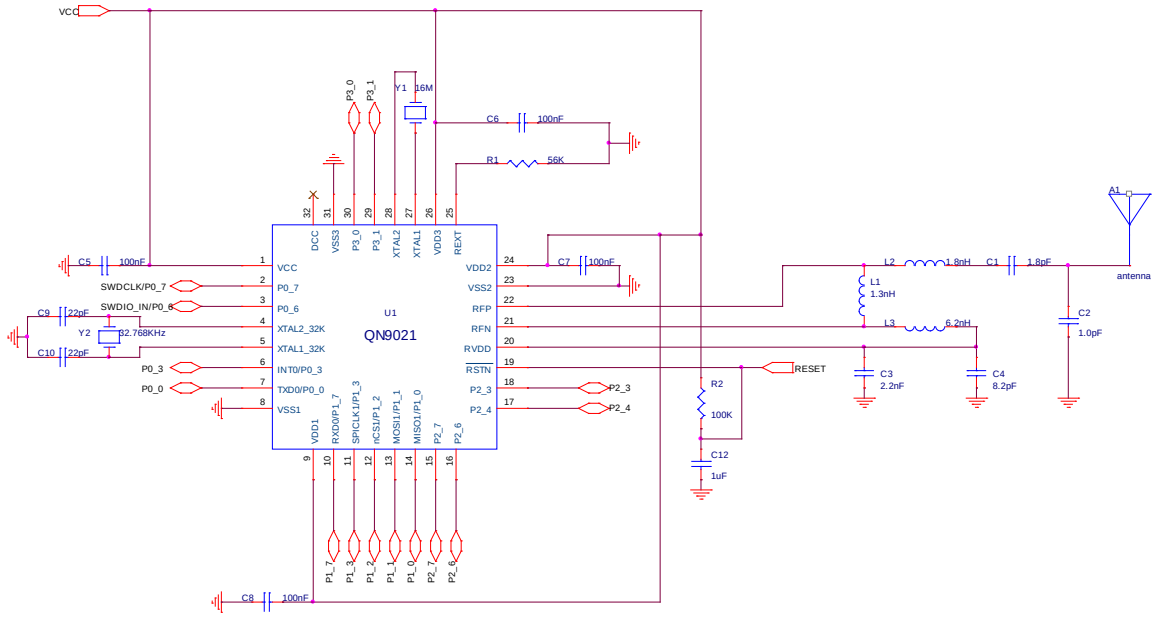

Figure 12 QN9021 without DC-DC converter reference design schematic

2.7 QN9020 typical application design schematic

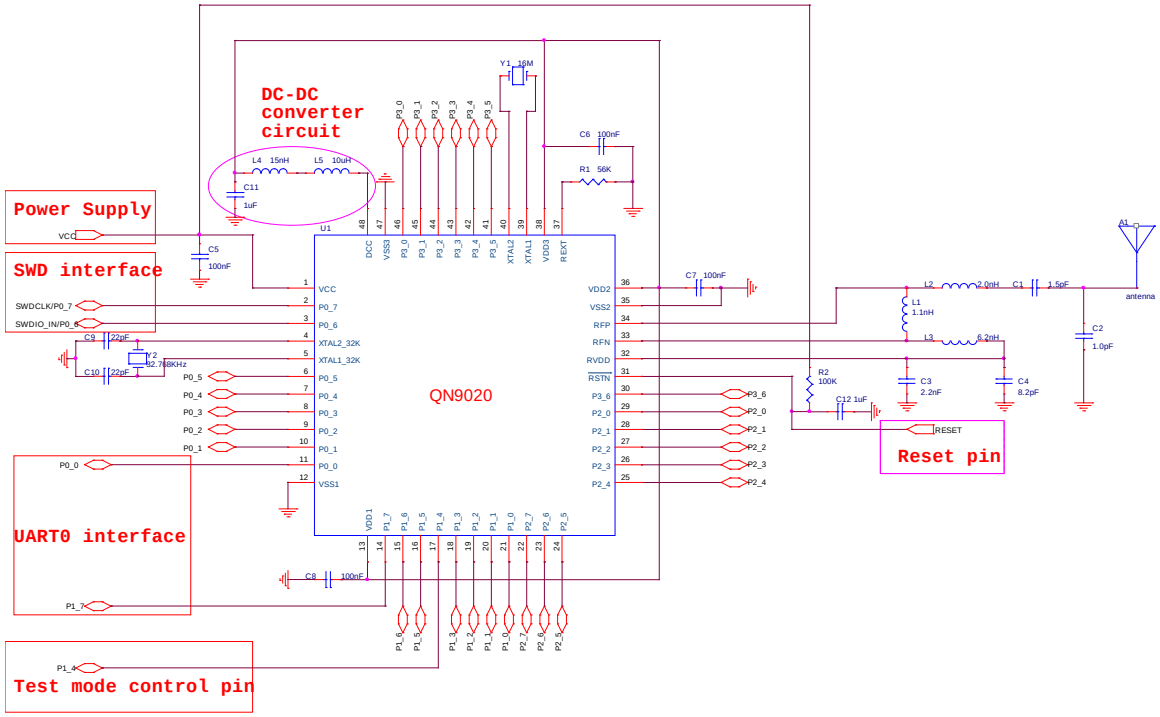

Figure 13 QN9020 Typical application design schematic

Note:

- VCC (pin1) must connect external power supply source.
- Reset pin (pin21) as an input pin used for QN9020 hardware reset. When it inputs logical low can force Qn9020 to reset.
- When GPIO P1.4 (pin17) is configured as an input and inputs logical low, it can force QN9020 enter into test mode.
- UART0 or SWD interface together with Reset used for Qn9020 to download program.

Please make sure you connect these pins out to interface pads for your production testing and debug purpose.

2.8 Bill of material

Table 5 Bill of materials for QN9020 with DCDC converter reference design

QN9020_48 with DC converter Reference Design Bom					
Item	**Part Description**	**Footprint**	**Reference**	**Qty**	**part No.**
Capacitor					
1	C_SMD, 100nF, X7R, ±10%, 16V, 0402	0402	C5,C6,C7,C8	4	GRM155R71C104KA88
2	C_SMD,1uF, X5R, ±10%, 6.3V, 0402	0402	C11,C12	2	GRM155R60J105KE19
3	C_SMD, 22pF, NP0, 5%, 50V, 0402	0402	C9,C10	2	GRM1555C1H220JA01
Resistor					
4	R_SMD,56K, ±1%, 0402	0402	R1	1	
5	R_SMD,100K, ±5%, 0402	0402	R2	1	
Inductor					
6	L_SMD,15nH,5%,0402	0402	L4	1	LQG15HN15NJ02
7	L_SMD,10uH,5%,0603	0603	L5	1	LQM18FN100M00D
Oscillator					
8	Crystal, 16MHz, ±20ppm, 12pF, 2.5x2.0x0.55 mm	SMD_2520	Y1	1	FA-20H
9	Crystal, 32.768K, ±20ppm, 15pF, 2.0x1.2x0.6 mm	SMD_2012	Y2	1	FC-12M
IC					
10	IC, 2.4G SOC, 64KB system memory, QFN48,QN9020	QFN48	U1	1	QN9020
RF circuit					
11	L_SMD, 6.2nH, ±0.1nH,0402	0402	L3	1	LQP15MN6N2B02
12	L_SMD, 2.0nH, ±0.1nH,0402	0402	L2	1	LQP15MN2N0B02
13	L_SMD, 1.1nH, ±0.1nH,0402	0402	L1	1	LQP15MN1N1B02
14	C_SMD, 2.2nF, X7R, ±10%, 50V, 0402	0402	C3	1	GRM155R71H222KA01
15	C_SMD, 8.2pF, COG, ±0.5pF, 50V, 0402	0402	C4	1	GRM1555C1H8R2DA01
16	C_SMD, 1.5pF, COG, ±0.25pF, 50V, 0402	0402	C1	1	GRM1555C1H1R5CA01
17	C_SMD, 1.0pF, COG, ±0.25pF, 50V, 0402	0402	C2	1	GRM1555C1H1R0CA01
Others					
18	Antenna		A1	1	

Table 6 Bill of materials for QN9020 without DCDC converter reference design

QN9020_48 without DC converter Reference Design Bom					
Item	**Part Description**	**Footprint**	**Reference**	**Qty**	**part No.**
Capacitor					
1	C_SMD, 100nF, X7R, ±10%, 16V, 0402	0402	C5,C6,C7,C8	4	GRM155R71C104KA88
2	C_SMD,1uF, X5R, ±10%, 6.3V, 0402	0402	C11	1	GRM155R60J105KE19
3	C_SMD, 22pF, NP0, 5%, 50V, 0402	0402	C9,C10	2	GRM1555C1H220JA01
Resistor					
4	R_SMD,56K, ±1%, 0402	0402	R1	1	
5	R_SMD,100K, ±5%, 0402	0402	R2	1	
Oscillator					
6	Crystal, 16MHz, ±20ppm, 12pF, 2.5x2.0x0.55 mm	SMD_2520	Y1	1	FA-20H
7	Crystal, 32.768K, ±20ppm, 15pF, 2.0x1.2x0.6 mm	SMD_2012	Y2	1	FC-12M
IC					
8	IC, 2.4G SOC, 64KB system memory, QFN48,QN9020	QFN48	U1	1	QN9020
RF circuit					
9	L_SMD, 6.2nH, ±0.1nH,0402	0402	L3	1	LQP15MN6N2B02
10	L_SMD, 2.0nH, ±0.1nH,0402	0402	L2	1	LQP15MN2N0B02
11	L_SMD, 1.1nH, ±0.1nH,0402	0402	L1	1	LQP15MN1N1B02
12	C_SMD, 2.2nF, X7R, ±10%, 50V, 0402	0402	C3	1	GRM155R71H222KA01
13	C_SMD, 8.2pF, COG, ±0.5pF, 50V, 0402	0402	C4	1	GRM1555C1H8R2DA01
14	C_SMD, 1.5pF, COG, ±0.25pF, 50V, 0402	0402	C1	1	GRM1555C1H1R5CA01
15	C_SMD, 1.0pF, COG, ±0.25pF, 50V, 0402	0402	C2	1	GRM1555C1H1R0CA01
Others					
16	Antenna		A1	1	

Table 7 Bill of materials for QN9021 with DCDC converter reference design

QN9021_32 with DC converter Reference Design Bom					
Item	**Part Description**	**Footprint**	**Reference**	**Qty**	**part No.**
Capacitor					
1	C_SMD, 100nF, X7R, ±10%, 16V, 0402	0402	C5,C6,C7,C8	4	GRM155R71C104KA88
2	C_SMD,1uF, X5R, ±10%, 6.3V, 0402	0402	C11,C12	2	GRM155R60J105KE19
3	C_SMD, 22pF, NP0, 5%, 50V, 0402	0402	C9,C10	2	GRM1555C1H220JA01
Resistor					
4	R_SMD,56K, ±1%, 0402	0402	R1	1	
5	R_SMD,100K, ±5%, 0402	0402	R2	1	
Inductor					
6	L_SMD,15nH,5%,0402	0402	L4	1	LQG15HN15NJ02
7	L_SMD,10uH,5%,0603	0603	L5	1	LQM18FN100M00D
Oscillator					
8	Crystal, 16MHz, ±20ppm, 12pF, 2.5x2.0x0.55 mm	SMD_2520	Y1	1	FA-20H
9	Crystal, 32.768K, ±20ppm, 15pF, 2.0x1.2x0.6 mm	SMD_2012	Y2	1	FC-12M
IC					
10	IC, 2.4G SOC, 64KB system memory, QFN32,QN9021	QFN32	U1	1	QN9021
RF circuit					
11	L_SMD, 6.2nH, ±0.1nH,0402	0402	L3	1	LQP15MN6N2B02
12	L_SMD, 1.8nH, ±0.1nH,0402	0402	L2	1	LQP15MN1N8B02
13	L_SMD, 1.3nH, ±0.1nH,0402	0402	L1	1	LQP15MN1N3B02
14	C_SMD, 2.2nF, X7R, ±10%, 50V, 0402	0402	C3	1	GRM155R71H222KA01
15	C_SMD, 8.2pF, COG, ±0.5pF, 50V, 0402	0402	C4	1	GRM1555C1H8R2DA01
16	C_SMD, 1.8pF, COG, ±0.25pF, 50V, 0402	0402	C1	1	GRM1555C1H1R8CA01
17	C_SMD, 1.0pF, COG, ±0.25pF, 50V, 0402	0402	C2	1	GRM1555C1H1R0CA01
Others					
18	Antenna		A1	1	

Table 8 Bill of materials for QN9021 without DCDC converter reference design

QN9021_32 without DC converter Reference Design Bom					
Item	**Part Description**	**Footprint**	**Reference**	**Qty**	**part No.**
Capacitor					
1	C_SMD, 100nF, X7R, ±10%, 16V, 0402	0402	C5,C6,C7,C8	4	GRM155R71C104KA88
2	C_SMD,1uF, X5R, ±10%, 6.3V, 0402	0402	C11	1	GRM155R60J105KE19
3	C_SMD, 22pF, NP0, 5%, 50V, 0402	0402	C9,C10	2	GRM1555C1H220JA01
Resistor					
4	R_SMD,56K, ±1%, 0402	0402	R1	1	
5	R_SMD,100K, ±5%, 0402	0402	R2	1	
Oscillator					
6	Crystal, 16MHz, ±20ppm, 12pF, 2.5x2.0x0.55 mm	SMD_2520	Y1	1	FA-20H
7	Crystal, 32.768K, ±20ppm, 15pF, 2.0x1.2x0.6 mm	SMD_2012	Y2	1	FC-12M
IC					
8	IC, 2.4G SOC, 64KB system memory, QFN32,QN9021	QFN32	U1	1	QN9021
RF circuit					
9	L_SMD, 6.2nH, ±0.1nH,0402	0402	L3	1	LQP15MN6N2B02
10	L_SMD, 1.8nH, ±0.1nH,0402	0402	L2	1	LQP15MN1N8B02
11	L_SMD, 1.3nH, ±0.1nH,0402	0402	L1	1	LQP15MN1N3B02
12	C_SMD, 2.2nF, X7R, ±10%, 50V, 0402	0402	C3	1	GRM155R71H222KA01
13	C_SMD, 8.2pF, COG, ±0.5pF, 50V, 0402	0402	C4	1	GRM1555C1H8R2DA01
14	C_SMD, 1.8pF, COG, ±0.25pF, 50V, 0402	0402	C1	1	GRM1555C1H1R8CA01
15	C_SMD, 1.0pF, COG, ±0.25pF, 50V, 0402	0402	C2	1	GRM1555C1H1R0CA01
Others					
16	Antenna		A1	1	

3. PCB layout for QN902x

3.1 PCB Stack-up

The recommend PCB Stack-up for QN902x application shows as follows.

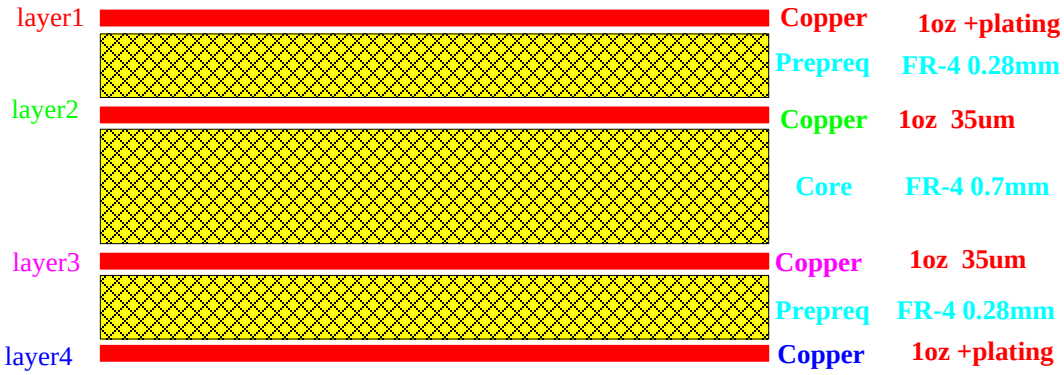

Figure 14 PCB stack up

The PCB board is 1.5 millimeter thick based on standard flame retardant (FR4) material.

3.2 RF interface

Since the QN902x works at 2.4GHz frequency, the parasitic parameters from printed circuit board (PCB) layout will affect the RF parameters and it is very sensitive. So we should pay attention to some details.

- Route the RF traces on the top layer and keep traces as short as possible no via is allowed on the trace.
- The impedance of the RF trace between matching network and antenna (or the SMA connector) must be 50-Ω. Under this RF trace there should be a large, unbroken solid ground. There should be via around the RF trace with high density.
- When the PCB is multi-layers (more than 2 layers) it should remove the ground plane on the internal layers under the RF components. Just keep the bottom layer's ground plane for shielding.
- On the top layer, it should make a distance between the components and the ground plane.
- Under the RF components and the RF traces no other signal trace is allowed.
- L1 should be placed as close as possible to QN902x RF port for reduce parasitic capacitance.

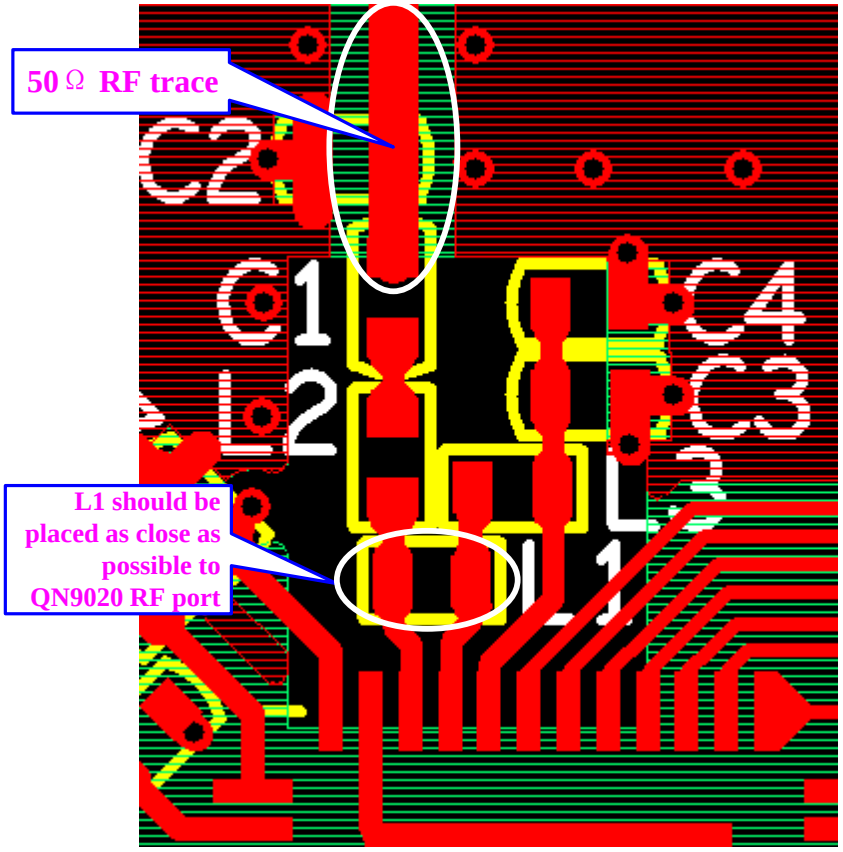

Figure 15 QN902x RF layout

3.3 Clock

If a crystal is used, the parasitic characteristics of the clock trace will influence the circuit. The trace must be kept as short as possible. Keep the ground plane under the crystal trace to improve the return path. We should avoid crossing the crystal trace between the layers.

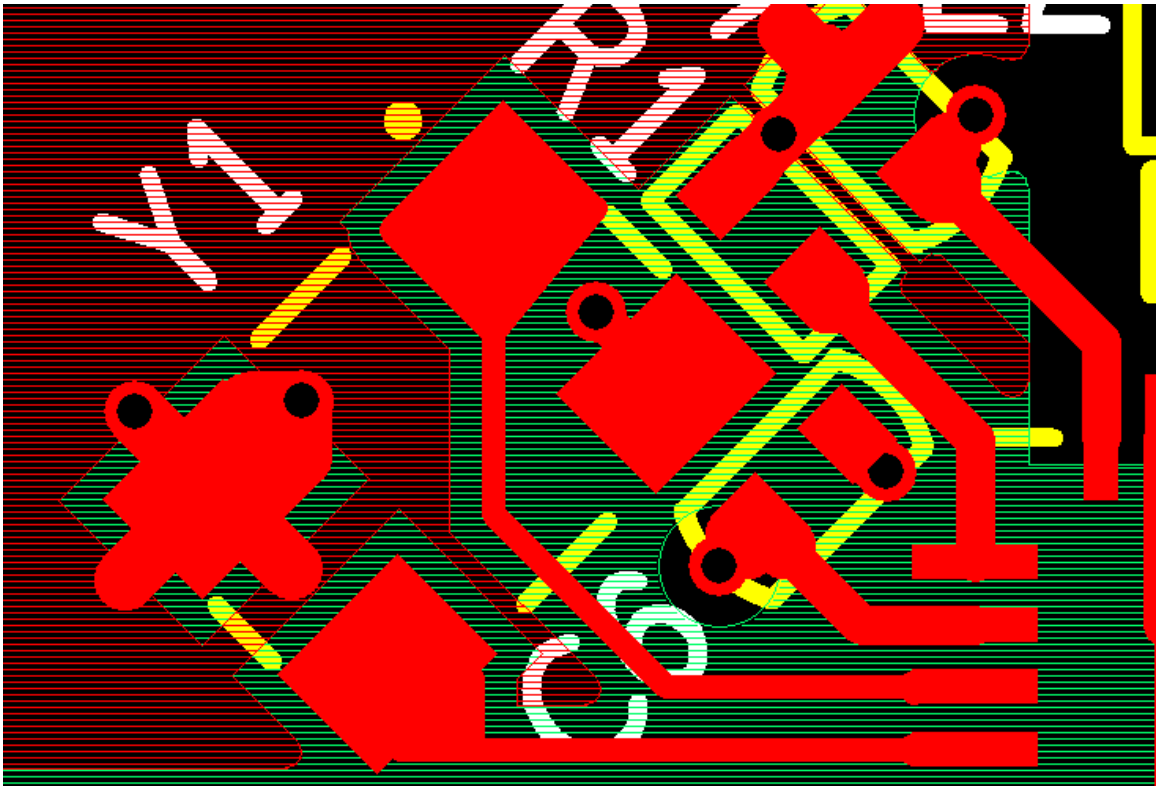

Figure 16 QN902x 16/32M clock layout

3.4 With DC-DC converter

The DC-DC converter will generate noise. It should place the DC-DC converter components to QN902x device as close as possible. Ensure the DC-DC converter output trace is wide enough. Trace must be kept as short as possible. Keep the useful signal trace far away from the DC-DC converter routing area.

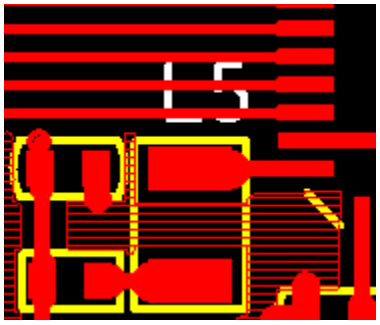

Figure 17 QN902x with DC-DC converter layout

3.5 AN Example of PCB layout

Qn9020 EVB layout

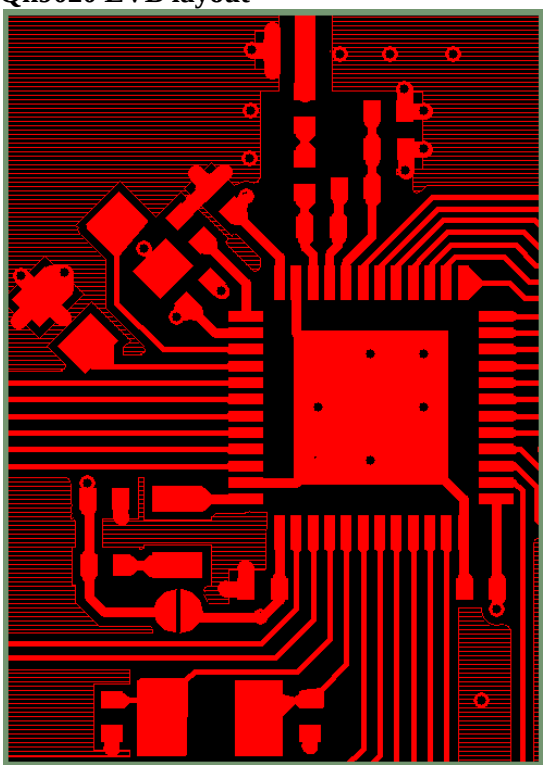

Figure 18 QN902x Layer1

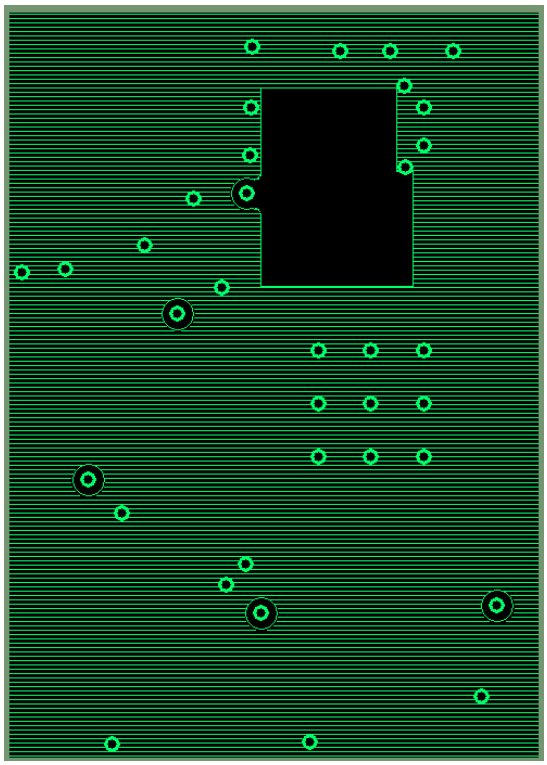

Figure 19 QN902x Layer2

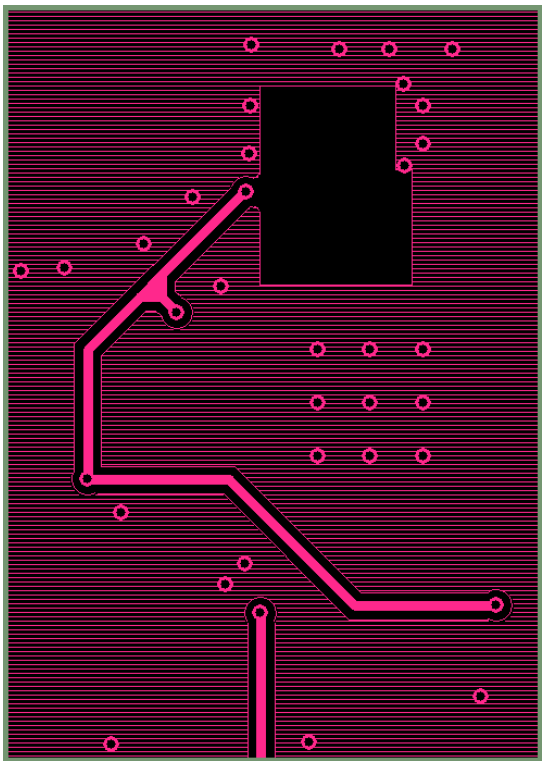

Figure 20 QN902x Layer3

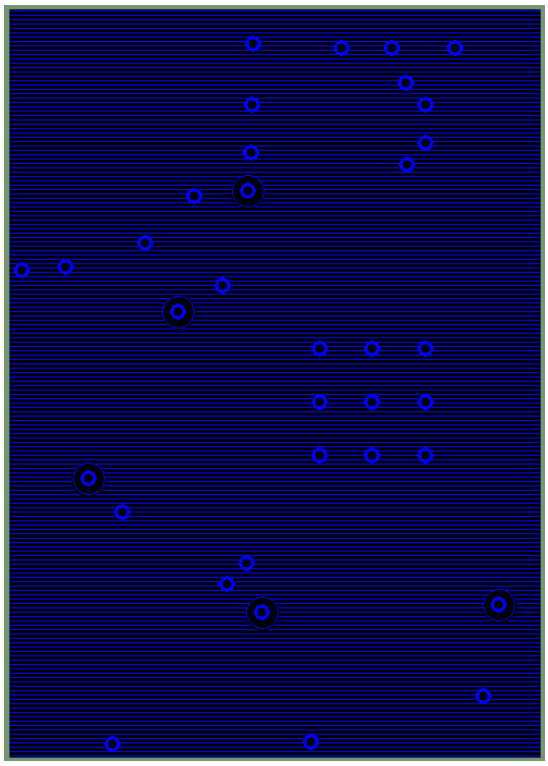

Figure 21 QN902x Layer4

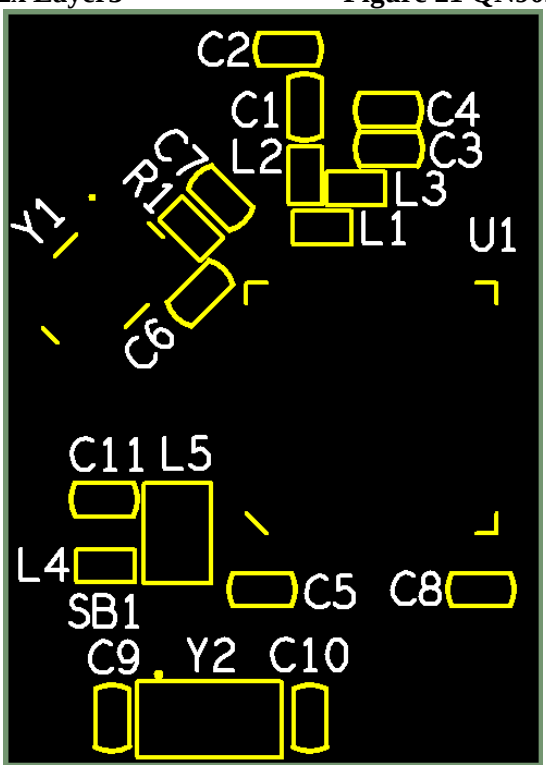

Figure22 QN902x SILK TOP

QN9021 EVB layout

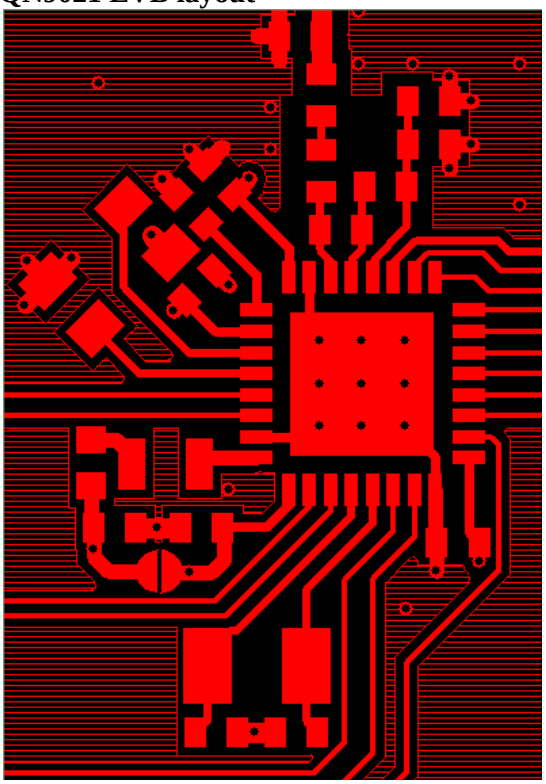

Figure23 QN9021 Layer1

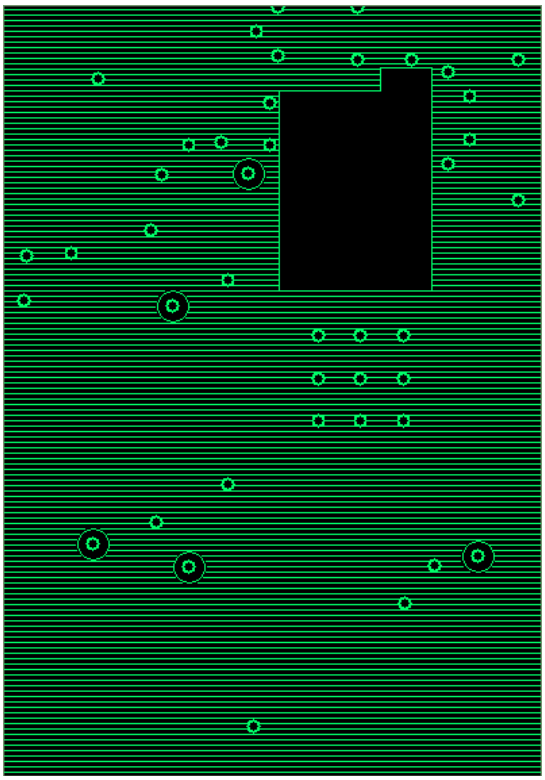

Figure24 QN9021 Layer2

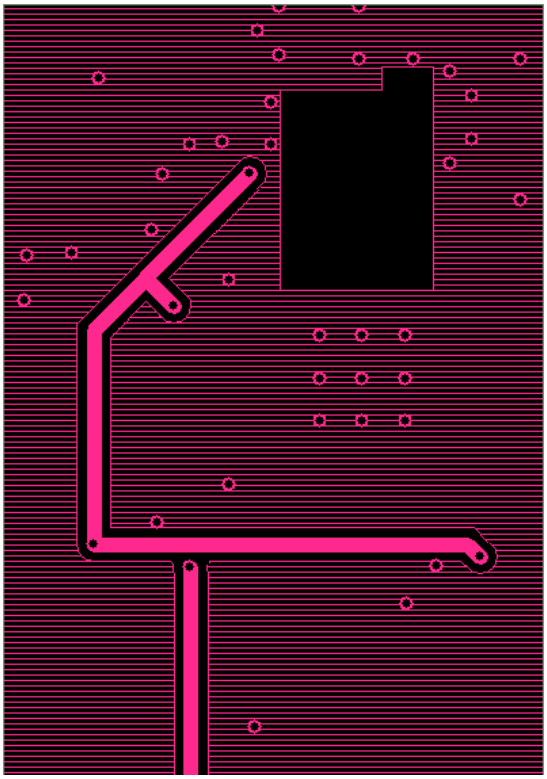

Figure25 QN9021 Layer3

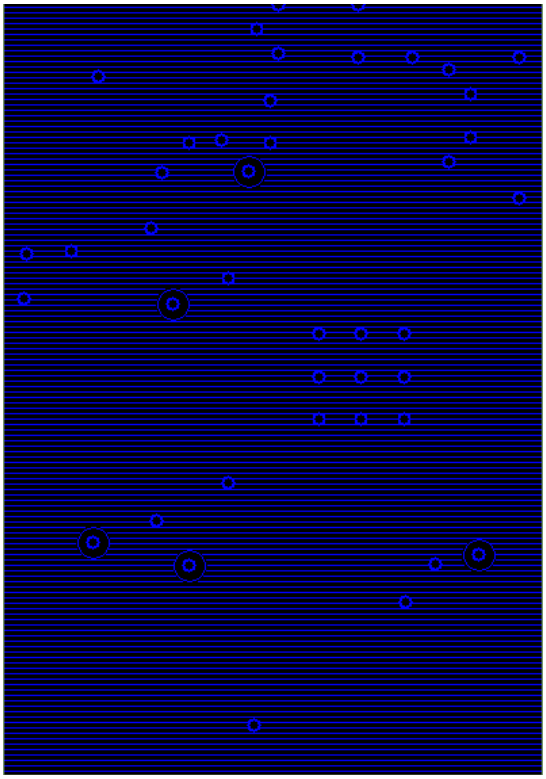

Figure26 QN9021 Layer4

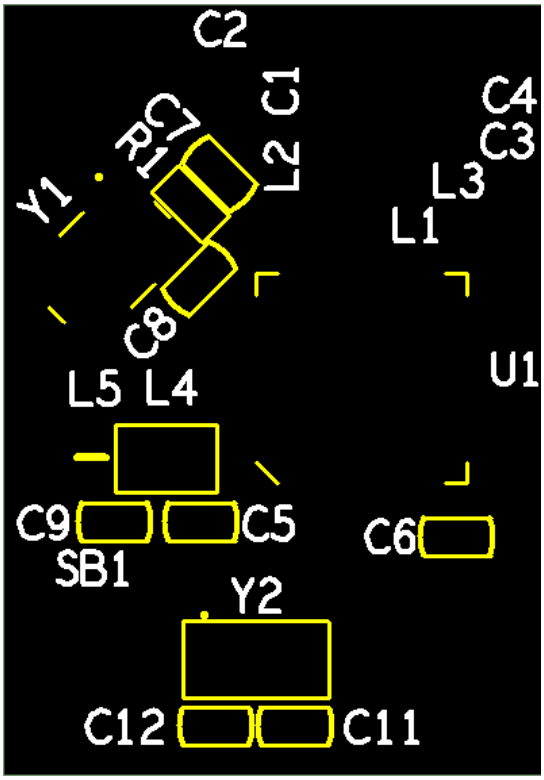

Figure27 QN9021 SILK TOP

Release History

REVISION	CHANGE DESCRIPTION	DATE
0.1	Initial release	2013-04-18
0.2	Add QN9021 reference design;	2013-05-22
0.3	Add QN9020 typical application design schematic	2013-06-06
0.4	Modify the pin name IDC to DCC in figure 9,10,11,12,13	2013-07-08
0.5	Update the RF matching net components value	2013-07-15
0.51	Update the parameter's with crystal Add GPIO description	2013-07-29
0.52	Update load capacitor value of 32.768 kHz crystal	2013-08-12
0.6	Update the Bill Of Material	2013-08-27
0.7	Suggest a 10uF capacitor to be connected to the pin1 of QN9020	2014-01-16
0.8	Swap the pins XTAL1 and XTAL2 in schematic Update the parameters for crystal's selection	2014-05-17

