Memory Technology

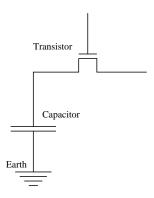
- All memory today is based on semi-conductor technology
- Previously magnetic core memory was used but replaced in 70s except for devices for use in nuclear facilities or space craft that needed to be resistant to ionization.
- Comes in two flavours
 - Dynamic random access memory (DRAM)
 - Static random access memory (SRAM)
- Random in this case means you can access locations in memory in any order. Compare with say magnetic tape

DRAM

- DRAM devices are charge based
- Each bit is represented by a charge in a capacitor
- This charge can leak away in a short time so the system needs to be refreshed to prevent data loss
- Reading a bit in DRAM discharges the capacitor so it needs to be refreshed
- Bits being refreshed are not available for reading

DRAM

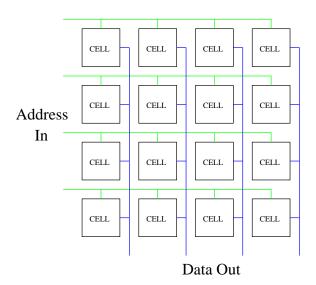
Structure of DRAM cell shown below



DRAM

- DRAM cells are organised as arrays
- Green lines are the Row Address Strobe (RAS)
- They determine which set of cells are being accessed
- Blue lines are Column Lines
- They are used to read off the values of the cells or to write new values back

DRAM Array



DRAM Types

- Asynchronous DRAM
 - No explict clocking of the chip
 - Responds to changes of the RAS
 - Small number of data lines
 - Improvements such as Paged DRAM and EDO DRAM
- Synchronous DRAM
 - Move to an explict clocking with signals read on rising or falling clock edge
 - Double Data Rate (DDR) clocks on both edges
 - Currently DDR4 is current standard

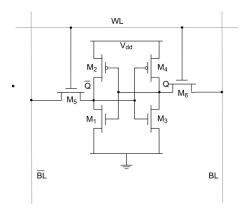
Future of DRAM

- DDR5 specs due by end of 2016
- Very little public information yet
- Alternatives to capacitance based storage
 - Resistive RAM fast switching, led by RAMBUS
 - Magnetoresistive RAM uses magnetism rather than electric charge to store data
 - Phase Change Memory data based on the changes of crystal strucutre of a material

SRAM

- Instead of using the charge in a capacitor, static RAM (SRAM) uses the state of a set of transistors to store a bit
- Static means the value stays in the memory as long as there is power.
- There is no leakage and no need to refresh the memory
- SRAM is used to provide processor registers and caches
- SRAM also found in hard disks, DVD drives etc. to buffer track data before writing

SRAM Cell



SRAM v DRAM

- SRAM is faster than DRAM
- SRAM uses less power than DRAM (at low clock speeds)
- SRAM takes up more space than DRAM
- SRAM costs more than DRAM
- ► SRAM is used if low power or high performance is required
 - embeded devices, caches
- DRAM is used for main memory mainly due to cost

Effective memory access rate

- The effective memory access rate is the average time it takes to load some data
- Suppose 90% of data is found in L1 cache, 4% in L2 cache and the remainder in main memory
- $ightharpoonup 0.9 \times 2ns + 0.04 \times 4ns + 0.06 \times 50ns = 4.96ns$
- You want to organise your code to achieve good hit rates
- Exploit locality of reference
- Use the same data locations
- Amortize the cost of the cache miss over many accesses over and over since they are in the cache