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May 2014

FDMC15N06

N-Channel UltraFET Power MOSFET

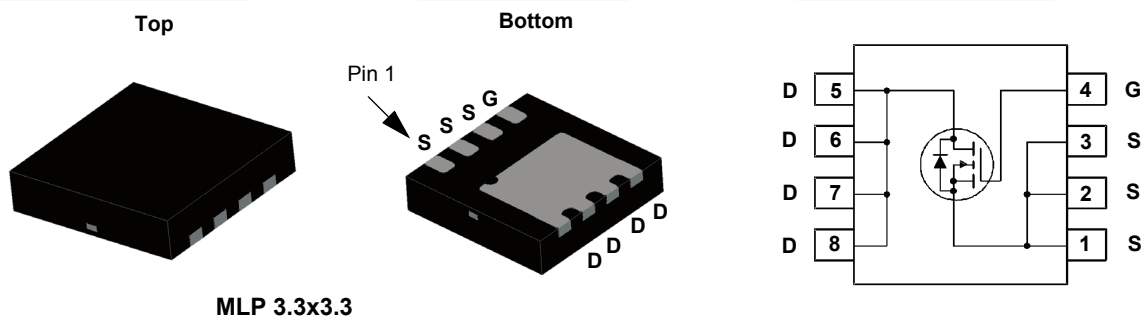
55 V, 15 A, 90 mΩ

Features

- $R_{DS(on)} = 75 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$
- 100% Avalanche Tested
- RoHS compliant

Description

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low voltage bus switches, and power management in portable and battery-operated products.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDMC15N06	Unit
V_{DSS}	Drain to Source Voltage	55	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	A
		- Continuous ($T_C = 100^\circ\text{C}$)	
		- Continuous ($T_A = 25^\circ\text{C}$) (Note 1a)	
I_{DM}	Drain Current	- Pulsed (Note 2)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 3)	mJ
I_{AR}	Avalanche Current	15	A
E_{AR}	Repetitive Avalanche Energy	3.5	mJ
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	W
		($T_A = 25^\circ\text{C}$)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDMC15N06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 1a)	53	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDMC15N06	15N06	Power 33	Tape and Reel	330 mm	12 mm	3000 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$, $T_C = 25^\circ\text{C}$	55	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	70	-	$^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$ $V_{DS} = 45\ \text{V}$, $T_C = 150^\circ\text{C}$	-	-	1 250	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 15\ \text{A}$	-	0.075	0.090	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\ \text{V}$, $I_D = 15\ \text{A}$	-	5	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$ $f = 1\ \text{MHz}$	-	265	350	pF
C_{oss}	Output Capacitance		-	97	130	pF
C_{rss}	Reverse Transfer Capacitance		-	28	42	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 30\ \text{V}$, $I_D = 15\ \text{A}$, $V_{GS} = 10\ \text{V}$ (Note 4)	-	8.8	11.5	nC
Q_{gs}	Gate to Source Gate Charge		-	1.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	3.6	-	nC

Switching Characteristics

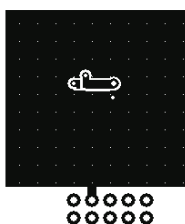
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\ \text{V}$, $I_D = 15\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_G = 25\ \Omega$ (Note 4)	-	9.5	29	ns
t_r	Turn-On Rise Time		-	36.5	83	ns
$t_{d(off)}$	Turn-Off Delay Time		-	22.5	55	ns
t_f	Turn-Off Fall Time		-	22	54	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	15	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	60	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 15 A	-	-	1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 15 A,	-	30	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs (Note 5)	-	35	-	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. 125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2: Repetitive rating: pulse-width limited by maximum junction temperature.

3: $L = 1\ \text{mH}$, $I_{AS} = 8.5\ \text{A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.

4: Essentially independent of operating temperature typical characteristics.

5: $I_{SD} \leq 15\ \text{A}$, $di/dt \leq 200\ \text{A}/\mu\text{s}$, $V_{DD} \leq 40\ \text{V}$, starting $T_J = 25^\circ\text{C}$.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

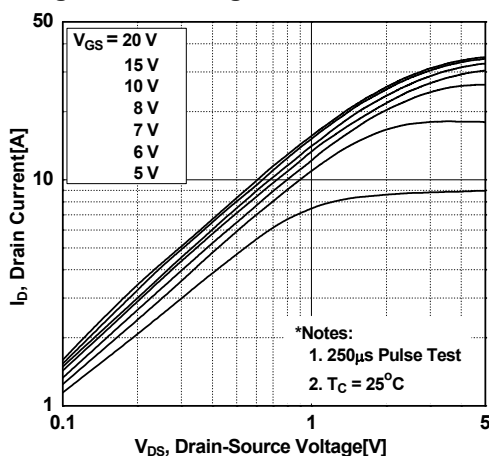


Figure 2. Transfer Characteristics

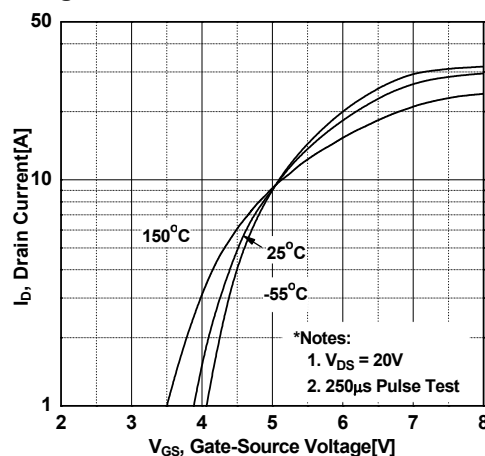


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

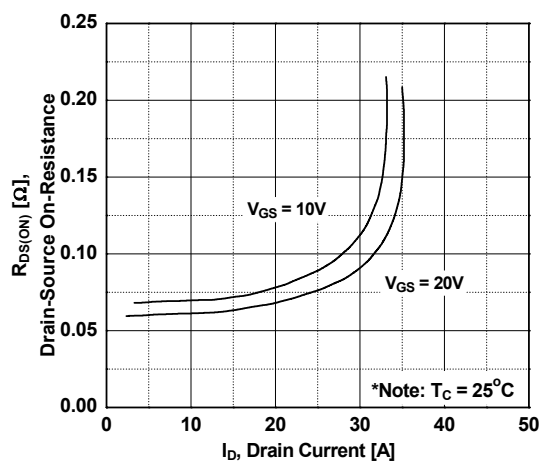


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

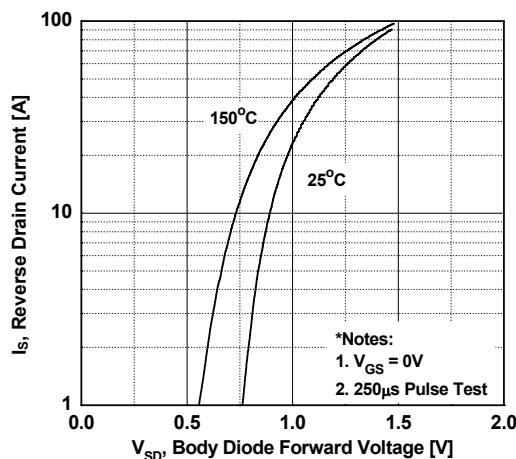


Figure 5. Capacitance Characteristics

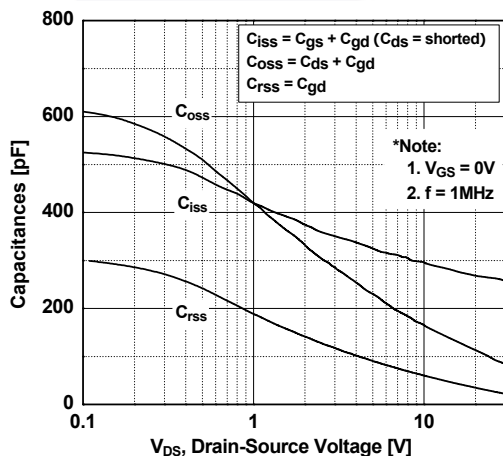
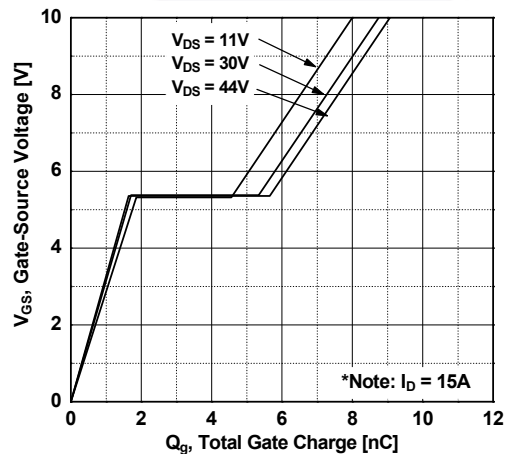


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

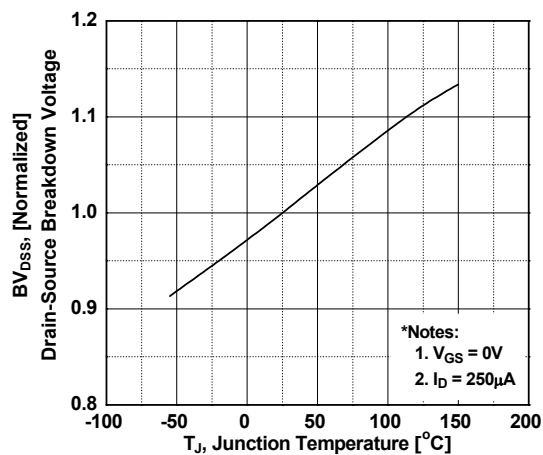


Figure 8. On-Resistance Variation vs. Temperature

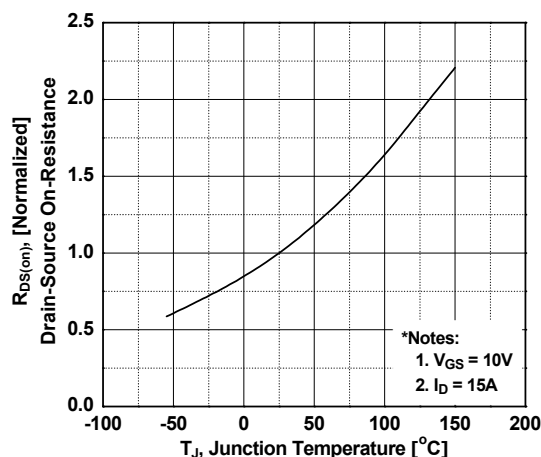


Figure 9. Maximum Safe Operating Area

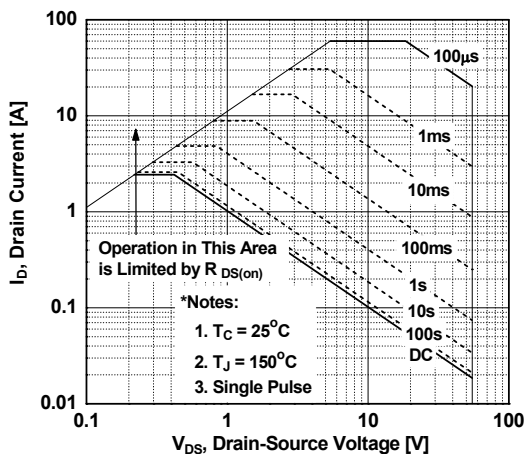


Figure 10. Maximum Drain Current vs. Case Temperature

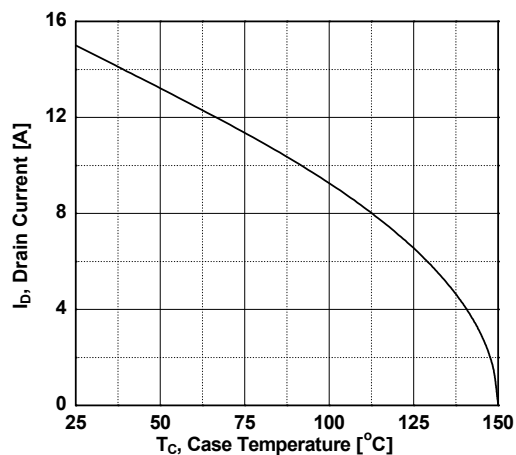
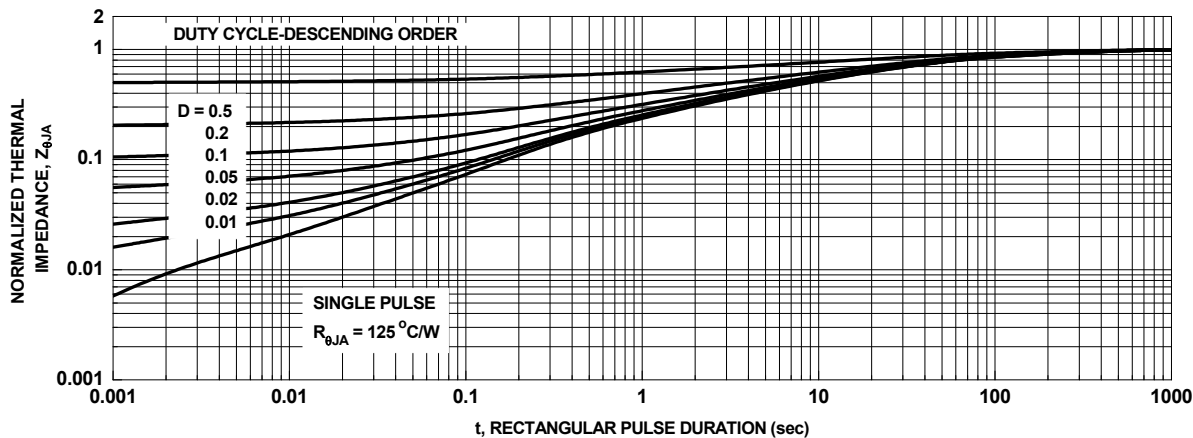


Figure 11. Transient Thermal Response Curve



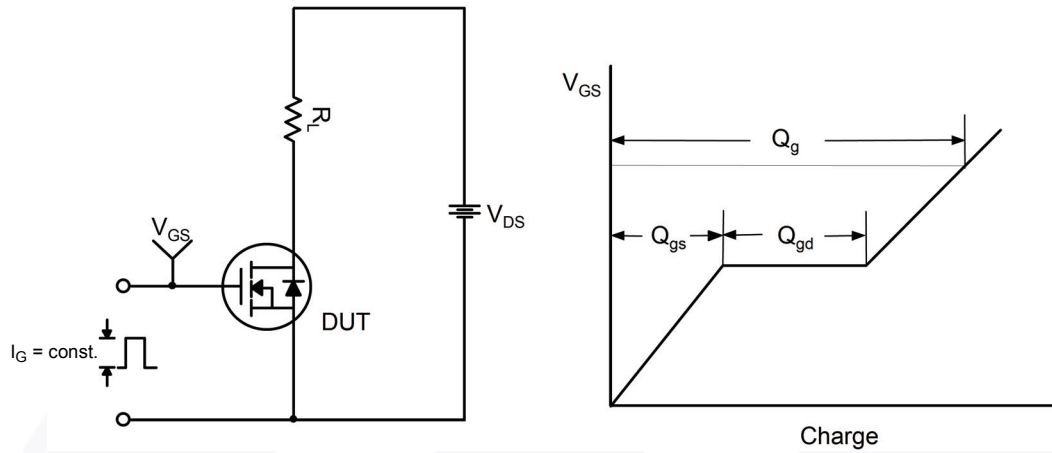


Figure 12. Gate Charge Test Circuit & Waveform

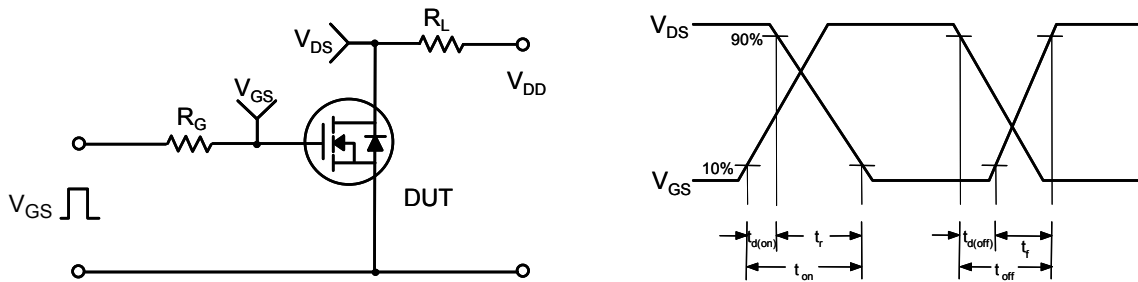


Figure 13. Resistive Switching Test Circuit & Waveforms

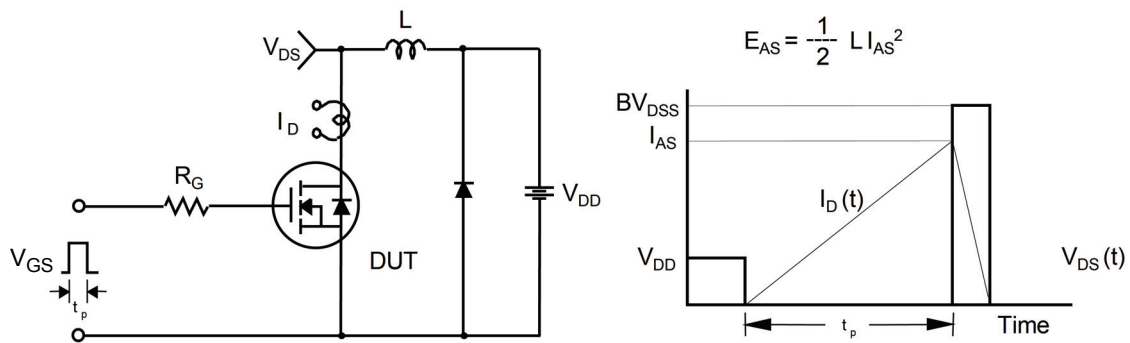


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

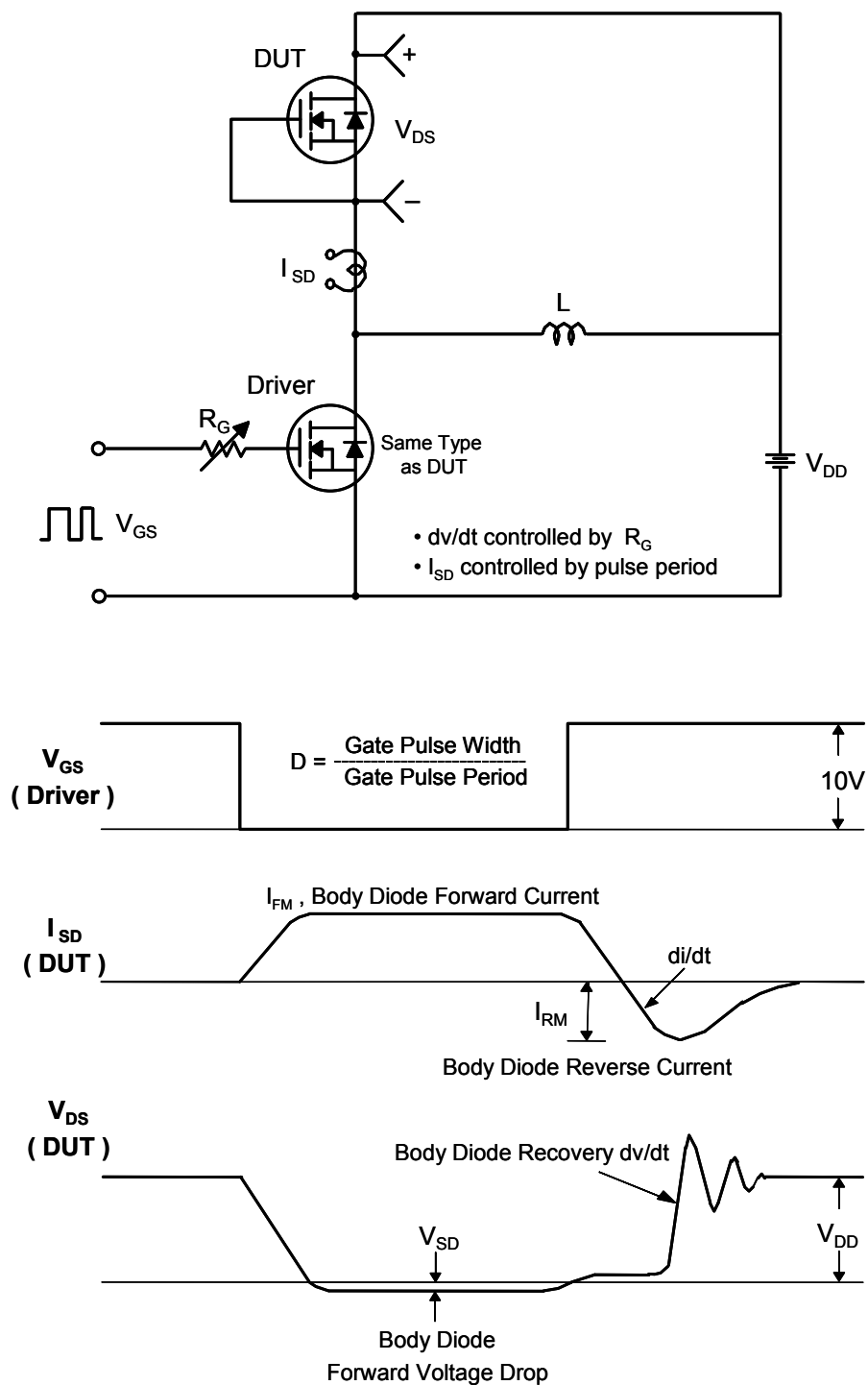




Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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