A VLSI recurrent network of integrate-and-fire neurons connected by plastic synapses with long term memory

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Abstract

Electronic neuromorphic devices with on-chip, on-line learning should be able to modify quickly the synaptic couplings to acquire information about new patterns to be stored (synaptic plasticity) and, at the same time, preserve this information on very long time scales (synaptic stability). Here we illustrate the electronic implementation of a simple solution to this *stability-plasticity problem*, recently proposed ([1]) and studied in various contexts ([2], [3]). It is based on the observation that reducing the analog depth of the synapses to the extreme (bistable synapses) does not necessarily disrupt the performance of the device as an associative memory, provided that 1) the number of neurons is large enough; 2) the transitions between stable synaptic state are stochastic; 3) learning is slow. The drastic reduction of the analog depth of the synaptic variable also makes this solution appealing from the point of view of electronic implementation and offers a simple methodological alternative to the technological solution based on floating gates.

We describe the full custom analog VLSI realization of a small network of integrate-and-fire neurons connected by bistable deterministic plastic synapses which can implement the idea of stochastic learning. In the absence of stimuli the memory is preserved indefinitely. During the stimulation the synapse undergoes quick, temporary changes through the activities of the pre- and post-synaptic neurons; those changes stochastically result in a long-term modification of the synaptic efficacy. The intentionally disordered pattern of connectivity allows the system to generate the randomness which drives the stochastic selection mechanism. The proposed implementation requires only $69 \times 83\ \mu m^2$ for the neuron and $68 \times 47\ \mu m^2$ for the synapse (using a $0.6\ \mu m$, 3 metals, CMOS technology) and hence it is particularly suitable for the integration of a large number of plastic synapses on a single chip.

I. INTRODUCTION

One of the main obstacles that hindered the development of neuromorphic analog systems is the lack of a reliable, robust and simple implementation of a *learning* mechanism, with the associated need of a suitable synaptic device. Difficulties range from the choice of the synaptic (and learning) model, both as to the biological and the computational appeal, to the design of the electronic device implementing the synapse and its learning dynamics. In particular, the synapse has to cope with the need of *long-term* storage, coupled to a *quick* ability to modify its state depending on instantaneous changes in the environment, to effect the learning mechanism.

The combination of digital memories and digital-to-analog converters is not really an option for the integration of large neuromorphic scale networks. Hence, in the past, and still now, one of the favorite solutions for the problem of long-term storage relies on floating-gates (see e.g. [4], [5] and references therein).

Recently proposed models of synaptic dynamics [1] suggest a possible and effective alternative to the solution offered by floating-gates. A network of neurons can perform well as an associative memory even if the analog depth of the synapses is reduced to the extreme (2 stable states on long time scales). Scenarios with binary or multistable synapses explored in the past (see e.g. [6]) usually comprised a first stage in which the structure of the patterns is stored in analog synapses. Only in the end, after all the patterns to be stored have been presented to the network, the analog synapses are clipped to one of the discrete stable states. In case of on-line learning in realistic conditions, this approach is not possible: with binary or multistable synapses the new patterns overwrite the information about the old ones and the forgetting process is too fast to permit any classification [7], [8]. The solution is to change only

a small fraction of synapses when patterns are presented to be learnt. The price to be paid is that the patterns should be presented more than one time and learning is slow. A possible unbiased, local mechanism which would select a given fraction of synapses is stochastic learning: at parity of pre and post-synaptic activities each synapses makes a transition with some probability. This mechanism guarantees that in average the same fraction of synapses changes upon presentation of a given stimulus. Provided that the transition probabilities are small enough, this stochastic selection allows to recover the optimal performances in terms of storage capacity [7].

This approach moves the problem to the generation of the appropriate stochastic process which would provide the needed random selection. Generating rare events in a material device like an electronic synapse is a difficult problem and usually requires either bulky devices, like big capacitors, or fine-tuning of the currents which control the dynamics. Moreover, the analog noise generated by analog devices is rather sensitive to temperature and humidity. The solution proposed in [1] exploits the irregularity of the neuronal activity, which in turn, emerges as a collective property of the network interactions when the pattern of connectivity is intentionally disordered [2], [3]. In particular, the synapse discussed in this paper is designed to encode the mean firing rates of the pre and the post-synaptic neuron. In this specific case the inter-spike variability can be exploited to have stochastic transition between stable states at parity of mean firing rates.

The above scenario for the synaptic dynamics relies on *spike-driven* modifications, which bring us to the adopted neuron model: the integrate-and-fire neuron. This leaves out easier, but poorer, solutions, based on an effective representation of the spiking neural activity (as in the case of neurons implemented through their *transfer function*). So, when on-line, dynamic learning is the goal, spiking neurons are not only an option for biological plausibility, but a computational need.

II. The hardware implementation

We present a VLSI recurrent network implemented on a $3.16 \times 3.16\ mm^2$ standard $0.6\ \mu m$, 3 metals, CMOS technology chip. It contains 21 integrate–and–fire neurons (14 excitatory and 7 inhibitory) randomly interconnected by 129 synapses (connectivity 30%). The 85 synapses between excitatory neurons are plastic, all the others are fixed. The plastic synapses are designed to implement a co-variance based learning rule: when the mean spike frequencies of the pre and post-synaptic neurons are high, the synapse is potentiated with some probability. In case of a mismatched pair of activity – the pre synaptic neuron fires at high rate while the post-synaptic neuron is silent – the synapse is depressed with another probability. No transitions occur for low pre-synaptic activity. Although the synapse has been designed to read and encode mean spike frequencies, the synaptic dynamics is also sensitive to higher order statistics and to the correlations of the pre and post-synaptic spike trains. The synaptic state, which can be potentiated or depressed, determines the excitatory post synaptic current (EPSC), generated by the synaptic circuit when a pre-synaptic spike is emitted.

The non–plastic synapses simply implements the post–synaptic current injection (excitatory or inhibitory) and the disorder intentionally introduced in the pattern of connectivity plays an important role in making the network activity irregular (see below).

A. The neuron

The main building blocks of the network are simple integrate-and-fire electronic neurons with constant leak, functionally equivalent to those described in [9]. These neurons integrate linearly the total afferent current and when a threshold is crossed they emit a spike. The subthreshold dynamics can be described by the equation governing the voltage across a capacitor (which represents the membrane potential of the cell):

$$V_{soma}(t) = V_{soma}(t_0) - I_\beta(t)t + \frac{1}{C}\int_{t_0}^{t} I(t')dt' \quad (1)$$

where $I(t)$ is the sum of the excitatory external current and all excitatory and inhibitory presynaptic currents, I_β is the leak current and C is the soma capacitance. As V_{soma} crosses the threshold θ, a spike is emitted and the membrane potential is reset to V_{reset}. Equation 1 must be complemented by the condition that V_{soma} cannot go below a minimal value V_{rest} which represents also the resting potential of the neuron. This rigid barrier turned out to be essential to achieve a qualitatively similar behavior to the one of the integrate-and-fire neuron with a leakage proportional to the membrane potential [10].

A schematic diagram of the circuit implementing the neuronal dynamics is shown in Fig. 2. It can be divided in four functional blocks:

1) *Input Block.* Transistors $M1$–$M6$ and capacitors $C1$–$C2$ implement the dynamics described by eq. 1. The total dendritic input current $I(t) = I_{exc} - I_{inh}$ is injected into the soma capacitance $C = C1 + C2$ through transistors $M1$ and $M2$, which act as digital switches. They are required to interrupt the current flow when the neuron is emitting a spike and to guarantee that the spike duration is not dependent on the input current.
2) *Leak Block.* The leak current I_β is set by the bias voltage V_β (transistor $M3$) and it is turned off during the emission of a spike ($M4$ acts as a digital switch) such that the duration of the spike acts effectively as an absolute refractory period.
3) *Spike Emission Block.* Transistors $M5$–$M6$, capacitors $C1$–$C2$ and inverters $N1$–$N2$ implement the spike emission mechanism. The input current is integrated by the parallel of the two capacitors $C1$ and $C2$. As V_{soma} crosses from below the switching voltage $V1$ of the inverter $N1$, the output voltage V_{spk} rises from ground to the positive power supply rail V_{dd} (spike activation). A positive feedback loop, implemented by the capacitive divider $C1$–$C2$, increases V_{soma} by $Vdd\frac{C2}{C1+C2}$ [9]. As long as V_{spk} is equal to V_{dd}, the digital switch $M6$ is closed and the current set by the bias voltage V_{pw} can discharge the two capacitors causing the membrane potential to decay linearly. As V_{soma} crosses again (this time from above) the switching voltage $V1$ of the inverter $N1$, the output voltage V_{spk} goes back to the ground level (spike inactivation) and the membrane potential decreases by $Vdd\frac{C2}{C1+C2}$ because of the action of the positive feedback loop (phase (5)). The integration of the input current can then start again.
4) *State Block.* Upon the presentation of a pre–synaptic spike the plastic synapses tend to be potentiated/depressed if the postsynaptic membrane potential is above/below a certain threshold (V_{ref}). A digital signal (V_{st_n}) is generated to encode the state of the neuron (V_{soma} below or above V_{ref}). This function is implemented with comparator $CP1$ and inverter $N3$.

The spike duration (τ_0) can be modified by changing the current I_{pw} and the interval between two consecutive spikes (ΔT) depends on the input currents (I_{exc} and I_{inh}) and the leak current (I_β). This characteristic times, and then the spike rate, can be easily calculated in the simple case of $I_{exc} - I_{inh} - I_\beta$ constant and positive. ΔT is the time needed to the membrane potential to reach $V_{dd}/2$ starting from the reset potential ($V_{dd}/2 - Vdd\frac{C2}{C1+C2}$):

$$\Delta T = V_{dd}\frac{C2}{I_{exc} - I_{inh} - I_\beta} \tag{2}$$

The spike duration is given by:

$$\tau_0 = V_{dd}\frac{C2}{I_{pw}} \tag{3}$$

In this case, V_{soma} is a periodic signal with period:

$$T = \Delta T + \tau_0 = V_{dd}C2\left(\frac{1}{I_{exc} - I_{inh} - I_\beta} + \frac{1}{I_{pw}}\right) \tag{4}$$

An oscilloscope acquisition of the dynamic of the neuron in this simple case is shown in Fig. 3. A small hysteresis (about $50\ mV$) in the switching voltage of the inverter $N1$ affects the spike activation and inactivation thresholds. This hysteresis is due to two sources of non–ideality for the inverter: the differences between PMOS and NMOS transistor parameters and the presence of parasitic capacitances. The order of magnitude of the measured hysteresis is compatible with Spectre simulation results for the neural circuit including the parasitic capacitances extracted from the layout.

During the design of the layout, particular attention was given to prevent possible problems due to the coexistence, on the chip, of fast varying signals (like V_{spk}) and slow analog signals (like V_{soma}). Parasitic capacitances between those signals can cause cross–talk, inducing undesired changes in the analog signal when the fast varying signal changes. To minimize the parasitic capacitances, and then prevent the cross-talk, a layer of metal, connected to the positive power supply rail or to ground, was inserted (wherever possible) between the crossing of two wires (on different layers) connected to different nodes of the circuit.

The layout of the neuron circuit cover an area of about $69 \times 83\ \mu m^2$.

B. The plastic synapse

The excitatory neurons are connected by plastic synapses. Their dynamics is described in terms of the a single internal variable V_{syn}, which represents the voltage across a capacitor. The synaptic efficacy depends on this internal state variable as explained below. Although V_{syn} is inherently analog, the synapse is designed in such a way that only the maximum and the minimum allowable values of V_{syn} are stable on long time scales, in the absence of pre-synaptic neuronal activity. Indeed when V_{syn} is above some threshold V_{thr}, a positive current drives V_{syn} to the upper bound $V = V_{dd}$, otherwise the synaptic capacitor is discharged at a regular pace until V_{syn} hits the lower bound $V = 0$. These two values are then preserved indefinitely and survive also small fluctuations which do not bring V_{syn} across the threshold V_{thr}. This bistability preserves the memory of one of the two states on long time scales and hence we will refer to the two currents described above as to the *refresh* currents. Upon the arrival

of a presynaptic spike the internal state of the synapse is modified to acquire information about the neuronal activity and hence about the stimulus. If the post-synaptic depolarization is above some threshold V_{ref} (see description of the *State Block* in Section II-A) the internal state V_{syn} is pushed upwards, otherwise it is pushed downwards. If these temporary changes accumulate and bring V_{syn} across the threshold V_{thr} the synapse is then attracted towards a different stable state and a transition occurres. As a consequence the role of the synaptic threshold is at least twofold: on the one hand it separates two bands of synaptic values which are the basins of attraction for two stable memory values; on the other hand it provides a simple and automatic mechanism to select only a fraction of synapses which would undergo a permanent change during the presentation of a stimulus. If the neuronal activity is irregular, then this selection is stochastic and implements the mechanism needed to recover the optimal performances of the networks as an associative memory (see also Conclusions). The specific form of the temporary changes induced by the neuronal activity has been designed to encode the mean spike rates of the pre and post-synaptic neuron. The pre-synaptic activity acts as a trigger (for low pre-synaptic spike frequency no transition can occur) and then the direction of the change is determined by the depolarization of the post-synaptic neuron. The latter provides a simple and instantaneous way to read indirectly the post-synaptic mean firing rate (see [1], [8] for more details).

The circuit implementing the described dynamics can be divided into five functional blocks (see Fig. 4 and Fig. 5(a)).

1) *Memory element*. The analog variable of the synapse (V_{syn}) is stored using a capacitor ($C_S = 327\ fF$).
2) *State generator block.* A digital signal (V_{st_s}), representing the state of the synapse (potentiated or depressed), is generated by the comparator $CP1$. V_{st_s} is the input signal for the *refresh block* and the *EPSC block*. If the voltage representing the internal variable of the synapse is greater/less than the threshold voltage V_{thr}, the digital signal V_{st_s} is low/high and the synapse is potentiated/depressed. In fact, in the *EPSC block*, V_{st_s} determines the intensity of the current injected in the postsynaptic neuron upon presentation of a presynaptic spike, and then the synaptic efficacy.
3) *Refresh block*. When the presynaptic neuron is inactive the synapse has to maintain the state generated by the previous stimulations. The transistors $M7$–$M9$ implement this function. When the synapse is depressed its state is maintained by mean of the current I_{refr_n}. When the synapse is potentiated ($V_{st\_s} = 0$) the current injected into the synaptic capacitor is given by the difference $I_{refr\_p} - I_{refr\_n}$, which has to be positive to maintain the potentiated state. We have to set $I_{refr\_p} = 2I_{refr\_n}$ to have an equal amount of positive and negative refresh currents.
4) *Hebbian block.* Transistor $M1$–$M6$ and inverter $N1$ implement the hebbian block. Transistor $M1$ and $M6$ act as digital switches and the current can flow only when a presynaptic spike is active. The sign of the current is determined by the postsynaptic digital signal V_{st_n} through the switches $M3$ and $M4$. If V_{st_n} is low (the membrane potential of the postsynaptic neuron is greater than V_{ref}) the current I_{biasp} charges the synaptic capacitor and tend to potentiate the synapse. If V_{st_n} is high (the membrane potential of the postsynaptic neuron is less than V_{ref}) the current I_{biaspn} discharges the synaptic capacitor and tend to depress the synapse.

5) *EPSC block*. The schematic diagram of the *EPSC (Excitatory Post Synaptic Current) block* is shown in Fig. 5(a). The synaptic current is injected into the postsynaptic soma capacitor only upon the presentation of a presynaptic spike (transistor $M1$ acts as digital switch). If V_{st_s} the digital switch implemented with transistor $M3$ is open and the EPSC is given by $I_{J-} = I_J$ (synapse depressed). If V_{st_s} transistor $M3$ is closed and the EPSC is equal to $I_{J+} = I_J + I_{\triangle J}$ (synapse potentiated).

The layout of the synaptic circuit cover an area of about $68 \times 47\ \mu m^2$.

C. The non–plastic synapse

The non–plastic synapse is implemented with a circuit that inject a fix amount of charge in the post–synaptic membrane capacitance upon presentation of a pre–synaptic spike. It is a simple *EPSC* or *Inhibitory PSC block* with only one possible value for the output current. The schematic diagrams of the excitatory and inhibitory non–plastic synapse are shown in Fig. 5 (b)–(c).

D. The test setup

Extensively testing the electronic neurons and synapses is an important complement to exploring the dynamic collective behavior of the implemented recurrent neural network (such results are reported elsewhere – [2], [11]). A programmable setup has been designed and built which, besides allowing basic chip parameters setting, enables reliable injection of currents with the desired statistical properties in the neurons on the chip, and real time acquisition of the spikes emitted by the neurons.

The analog VLSI network is hosted by a re–configurable micro-controlled I/O board that provides the control parameters, the static network parameters and the input external current, via 12 bit multifunction DAC modules. Output spikes are gathered by another micro-controlled device, the acquisition board, endowed with 64 Kspikes total memory on board; for example, a 50 Hz rate implies about 60 seconds available time span for recording the neurons' activity. Each spike is encoded as the label of the emitting neuron and the attached time label. A workstation handles the communication with the I/O board. A high-level user interface has been developed for parameters setting, spikes recording and data visualization and analysis.

To characterize the input output properties of the single neuron of noisy afferent currents we needed a controlled source of external noise to inject into the neuron. To this end, a suitable off–chip generator of pseudo–random current signals was designed and built. The noise generator is based on a classical scheme exploiting the properties of feedback shift registers ([12], [13]). The output digital waveforms are usually filtered (e.g. by an RC low-pass circuit) to produce an analog Gaussian noise signal, while in this case the integrate–and–fire neuron itself provides the filter acting as an integrator.

III. The single neuron and the network

In order to characterize the dynamic response of the single neuron subject to input current with various statistical properties, some parameters must be estimated first:

Leakage β

The leakage term I^i_β is estimated for each neuron i, for a set of values of the global parameter β which controls I^i_β, in order to check the linearity of I^i_β *vs* β in the range of interest.

I^i_β is simply derived by comparing the slopes of the neuron's depolarization upon injecting a DC external current with and without the leakage term.

It turned out that, while I^i_β is pretty linear for all neurons for $\beta \in [0, 0.2]\mu A$, the slope of the fit has a significant spread among the neurons, apparently due to a high variability in the mirrored I^i_β currents.

The measured values for the slope b of the linear fit are: $< b >= 5.32$ $\sigma^2_b = 0.86$

The time width of the spike

The time duration τ_0 of the spike has been directly measured on the oscilloscope, for an interval of values of $I_{\tau_0} \in [0, 2]\mu A$. The linear fit gives: $\frac{1}{\tau_0} = 10^{-5} \cdot I_{\tau_0} - 10^{-4} ms$; $r^2 = 0.9996$

A. Single neuron current–to–rate transfer function

To characterize the response properties of the implemented neuron for noisy input currents we adopted the following procedure:

- The feedback, shift-register random generator mentioned in Section II-D generates sequences mimicking a binomial process, such as to produce a random switching signal between preset 'high' and 'low' values, a 'random period square wave'.
- The mean and variance of the random simulated current signal are computed as:

$$\mu = \frac{\Delta V_+ - \Delta V_-}{2T}$$
$$\sigma^2 = \frac{(\Delta V_+ + \Delta V_-)^2}{4T}$$

  where ΔV_+ and ΔV_- are the voltage jumps in the neuron's potential induced in a clock period T of the noise generator.
- The computed mean and variance are plugged into the theoretical formula for the neuron's transfer function:

$$\nu = \Phi(\mu, \sigma) = \left[\tau_0 + \frac{\sigma^2}{2\mu^2}\left(e^{-\frac{2\mu\theta}{\sigma^2}} - e^{-\frac{2\mu V_{reset}}{\sigma^2}}\right) + \frac{\theta - V_{reset}}{\mu}\right]^{-1}$$

  Where ν is the spike frequency of the neuron, θ is the spike emission threshold and V_{reset} is the reset membrane potential. All other relevant parameters (θ, V_{reset}, τ_0, I_β) are independently measured as reported above.
- The experimental transfer function is checked against the theoretical predictions.

It is seen from Figure 7 that theoretical predictions are fairly well matched by the measured neuron response. Curiously, some minor discrepancies are reminiscent of similar ones recently encountered in checking the same theoretical predictions against experimental data recorded *in vitro* (e.g. the small defect for very low input current μ

for the deterministic case $\sigma = 0$, and the crossover for high μs [14]). This current-to-rate transfer function contains all the single neurons properties that are relevant for the network collective dynamics in stationary conditions [10].

B. Neurons coupled by excitatory connections

We briefly sketch in the following a few relevant features exhibited by the interacting network, referring the reader to references [2], [11], [3] for a fuller account.

Our intention is to show a glimpse of the rich phenomenology exhibited by such a small electronic network, in view of the scenario outlined in the Introduction, which envisages the recurrent neural activity providing a dynamic source of randomness to be exploited by the synapses to implement stochastic, slow modifications of the efficacies.

We remark that each synapse evolves on the basis of information local in time and space (the instantaneous activities of its pre- and post-synaptic neurons); the high feedback in the network makes the activity of each neuron reflect any sources of disorder, first of all in the pattern of connectivity, which is fixed but random in our case.

1) The excitatory–to–excitatory synapse: As a preliminary step, the effective value of the excitatory–to–excitatory synaptic efficacy I_{EE} *vs* the global parameter J_{EE} has been directly measured on the oscilloscope from the jumps ΔV induced in the depolarization of the post–synaptic neuron by spikes emitted by the pre–synaptic neuron .

$\Delta V/\theta = 5 \cdot \ 10^{-5} J_{EE} - 0.0027$ mV; $r^2 = 0.992$

for $J_{EE} \in [0, 4] \mu A$

2) A deterministic excitatory network: Figure 6 shows an example time record of the synaptic internal state variable (trace 2) and the synaptic efficacy (trace 1) of an excitatory synapse, with the associated time course of the pre–synaptic spike train (trace 3) and post–synaptic membrane potential (trace 4).

Figure 8 shows two *raster* representations of the network activity for uncoupled neurons (all the synaptic efficacies are set to 0, top) and for neurons coupled by excitatory synapses ($J_{EE} \neq 0$, $J_{EI} = J_{IE} = JII = 0$, bottom). The spikes emitted by each neuron are represented by drawing a bar at the corresponding position along the time axis; each row in the raster represents a sequence of spikes emitted by a given neuron (rasters of this kind are a common representation of the neural activity in experimental neuroscience).

The top panel in Figure 8 illustrates a situation in which the same (constant and positive) input current is set for all the uncoupled neurons. Because of the various inhomogeneities (in the current mirrors, in the neurons themselves) the neurons exhibit a wide variability in the firing rate (though we remark that the firing of any given neuron is quite stable and reproducible).

Excitatory synaptic couplings are switched on in the bottom panel (the synaptic dynamic is not active), while the input current is still constant and equal for all neurons; its value is adjusted in order to compensate for the mutual excitation and have the same average firing rate. It is clearly seen that, despite the fact that no additional source of randomness has been introduced, the recurrent excitation through a disordered pattern of connectivity is enough to endow the neurons' firing pattern with high variability.

This qualitative observation can be put on quantitative basis by making contact with the *mean field* predictions appropriate for the given network architecture; detailed checks have been carried out, which provide, for the toy

external stimulation examined, a surprisingly good match between mean field predictions and the behavior of such a small network ([2], [11]).

The resulting confidence in the ability of the electronic network to support controllable stochastic synaptic modifications has been corroborated by a dedicated study in [3].

IV. Conclusions

We described a pilot implementation in the relatively unexplored area of analog VLSI *recurrent* networks of spiking neurons, with *on-chip* unsupervised synaptic dynamics.

Many successful developments in the field of neuromorphic engineering dealt with sensors (visual or auditory) and simple networks designed to provide quick and simple decisions on the basis of sensory information, suited for robot guidance in simple environments, for example([15]). Though those efforts have been, and are, invaluable in sharpening techniques and supporting the feasibility and soundness of the neuromorphic approach to "natural computation", there is little doubt that really interesting neuromorphic systems endowed with complex computational abilities will integrate sensors and "decision modules" with intermediate layers of computation, taking care for example of "classification" of sensory stimuli, a necessary function in view of operation in a realistic environment.

Classification tasks have been in the focus of theoretical research in computational neuroscience for long, and there is a wealth of knowledge to be used to derive design principles for "neuromorphic classifiers" (just to mention relevant keywords, the whole *attractor* picture emerging from *Hebbian* learning in networks of spiking neurons with high feedback and providing models of *working memory* states, provides an example).

The small network described in the present paper includes the essential elements needed to implement such Hebbian spike-driven plasticity through a stochastic mechanism which selects actual changes in the synaptic efficacies, out of the eligible ones, following the approach briefly outlined in the Introduction; stochasticity is autonomously generated by the network activity, thus providing a key plausibility element.

Scaling up the described architecture poses a number of non trivial problems. The first is related to the recurrent connectivity of the network: as the number of neurons N increases the number of synaptic connections can grow as much as N^2, and clever packing strategies have to be devised in order to optimize the layout and the routing of the chip, due to both considerations of total silicon area, and cross-talk effects.

Besidesthe I/O channels needed to experiment with such systems constitute quite a complex complement to the chip. Again, the needed communication bandwidth badly scales with the size of the network (for a given average emission spike rate of each neuron).

We faced the first, packing problem in developing a bigger network (128 neurons, about 3000 plastic synapses) ([16]), to be described elsewhere, in which an optimization algorithm has been developed to find the 'best' placement and routing of synaptic connections.

As for the communication issues, it has long been suggested that a communication channel suited for connecting neuromorphic devices should exploit the asynchronous, instantaneous and stereotyped nature of the spikes (AER bus - Address Event Representation see [17], [18]).

Following the AER principles, we developed a communication system based on a programmable interface connecting the AER bus to the standard PCI bus, and a flexible setup is under development, suited to deal with several chips implementing large networks [19].

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Figure Captions:

Figure 1 Layout of the chip. It is a $3.16 \times 3.16\ mm^2$ chip implemented using standard $0.6\mu m$ 3 metals CMOS technology.

Figure 2 Schematic diagram of the integrate–and–fire neuron. The four functional blocks (input, state, leak, action potential) implement an integrate-and-fire neuron which integrates linearly the input, has a constant leakage, and emits a spike when V_{soma} crosses a threshold. See the text for a detailed description.

Figure 3 Neuronal dynamics. The neuron integrates linearly a constant current. As soon as V_{soma} (bottom trace) crosses the threshold θ for emitting a spike, the action potential is initiated and an impulse (top trace) is generated by the spike emission block. A positive feedback loop drives V_{soma} to $\theta + V_{dd}\frac{C_2}{C_1+C_2}$ from where V_{soma} decays linearly, down to θ. As V_{soma} crosses from above θ the output voltage V_{spk} goes back to the ground level (spike inactivation) and the membrane potential decreases by a fixed amount.

Figure 4 Schematic diagram of the plastic synapse: the internal state of the synapse is determined by the voltage across capacitor C_s. The state generator block and the refresh block ensures the preservation of memory on long time scales and they are equivalent to a digital cell. The hebbian block contains all the information about the learning prescription. See the text for more details.

Figure 5 (a) Schematic diagram of the EPSC block of the plastic synapse. V_{st_s} is a digital voltage representing the synaptic state (potentiated or depressed). An EPSC is generated only upon arrival of a presynaptic spike. The output current is $I_{exc} = I_J$ when the synapse is depressed state and $I_{exc} = I_J + I_{\Delta J}$ when it is potentiated. Both I_J and $I_{\Delta J}$ are set externally. (b) Non–plastic excitatory synapse circuit. When a presynaptic spike occurs, the current I_{IE} (externally set) is injected in the postsynaptic capacitance. (c) Non–plastic excitatory synapse circuit. An IPSC of intensity I_{xI} ($x \in \{E, I\}$, both currents are externally set) is generated upon arrival of a presynaptic spike.

Figure 6 The synaptic dynamics is illustrated by showing the oscilloscope acquisition of the following signals (from top to bottom): digital synaptic state (V_{st_s}), analog synaptic variable (V_{syn}), presynaptic input spike (V_{spk}), postsynaptic membrane potential. The pre–synaptic and post–synaptic neurons are injected a constant current which brings them at the spike threshold at a regular pace (high frequency for the pre–synaptic neuron, low frequency for the post-synaptic one). The synapse starts from the lowest bound (depressed state) and is then pushed up by a succession of pre-synaptic spike which find the post–synaptic neuron in a highly depolarized state. As soon as V_{syn} crosses the synaptic threshold V_{thr}, the synapse is attracted towards the potentiated state ($V_{st\_s} = V_{dd}$). A series of downwards jumps induced by pre–synaptic spikes which occur in coincidence with low post–synaptic depolarization brings V_{syn} below the threshold again. Note that the topmost trace, which represents the digital synaptic state, and hence, the real synaptic efficacy, is either 0 or V_{dd} depending on whether V_{syn} is below or above the synaptic threshold V_{thr}.

Figure 7 The neurons transfer function: the mean frequency as a function of the mean μ and the variance σ^2 of the input current. Each curve represents the predicted firing rate as a function of μ of the current for a specific σ^2. The corresponding measured spike frequencies are indicated by various symbols (diamonds, circles, stars and crosses).

Figure 8 Raster plots of the spikes produced by the network for two different external currents (each tick mark corresponds to a spike, each row contains a different excitatory neuron). The same current is injected to all the excitatory neurons. Top: the neurons are decoupled (the synaptic efficacies are set to zero) and fire very regularly, indicating that the electronic noise is negligible. Bottom: the excitatory interactions are turned on and the external current is reduced in order to get the same mean spike frequency. The neurons now feel the disorder intentionally introduced in connectivity pattern and they fire more irregularly. This is the randomness which drives the stochastic selection mechanism.

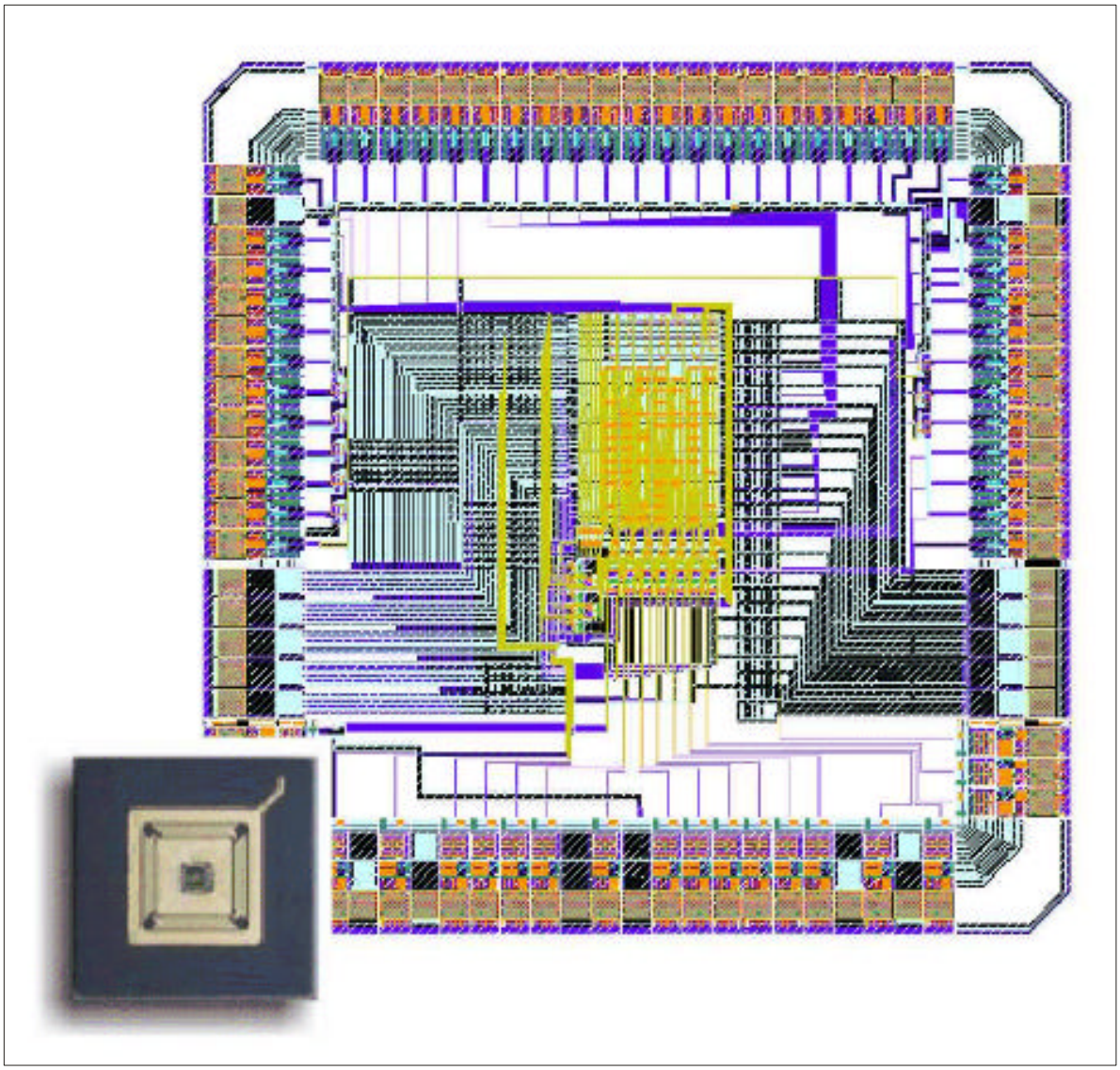

Fig. 1.

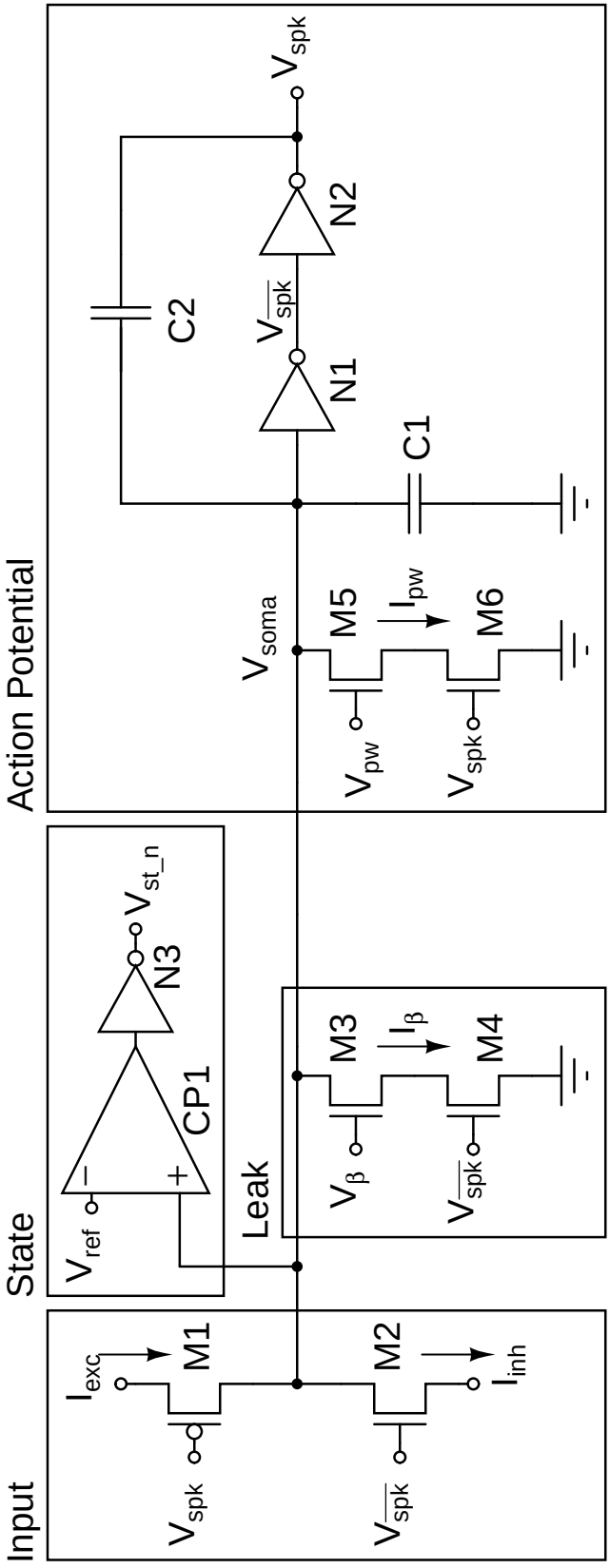
Input
State
Action Potential
Leak
M1
M2
M3
M4
M5
M6
N1
N2
N3
CP1
C1
C2
I_{exc}
I_{inh}
I_{β}
I_{pw}
V_{spk}
$V_{\overline{spk}}$
V_{β}
V_{pw}
V_{soma}
V_{ref}
V_{st_n}

Fig. 2.

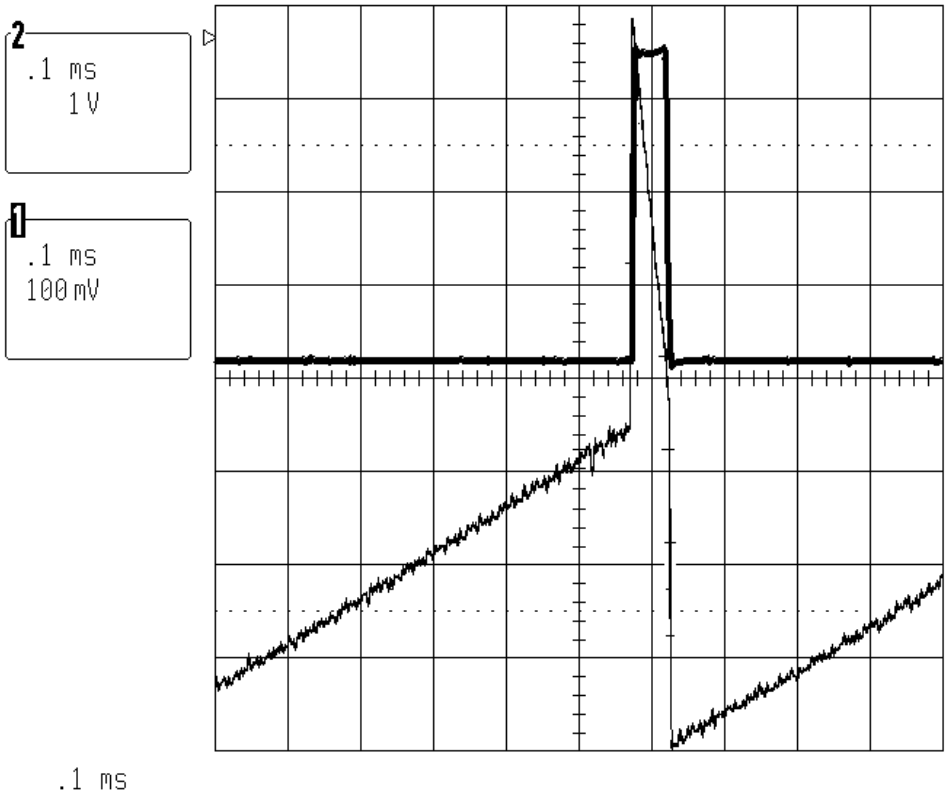

Fig. 3.

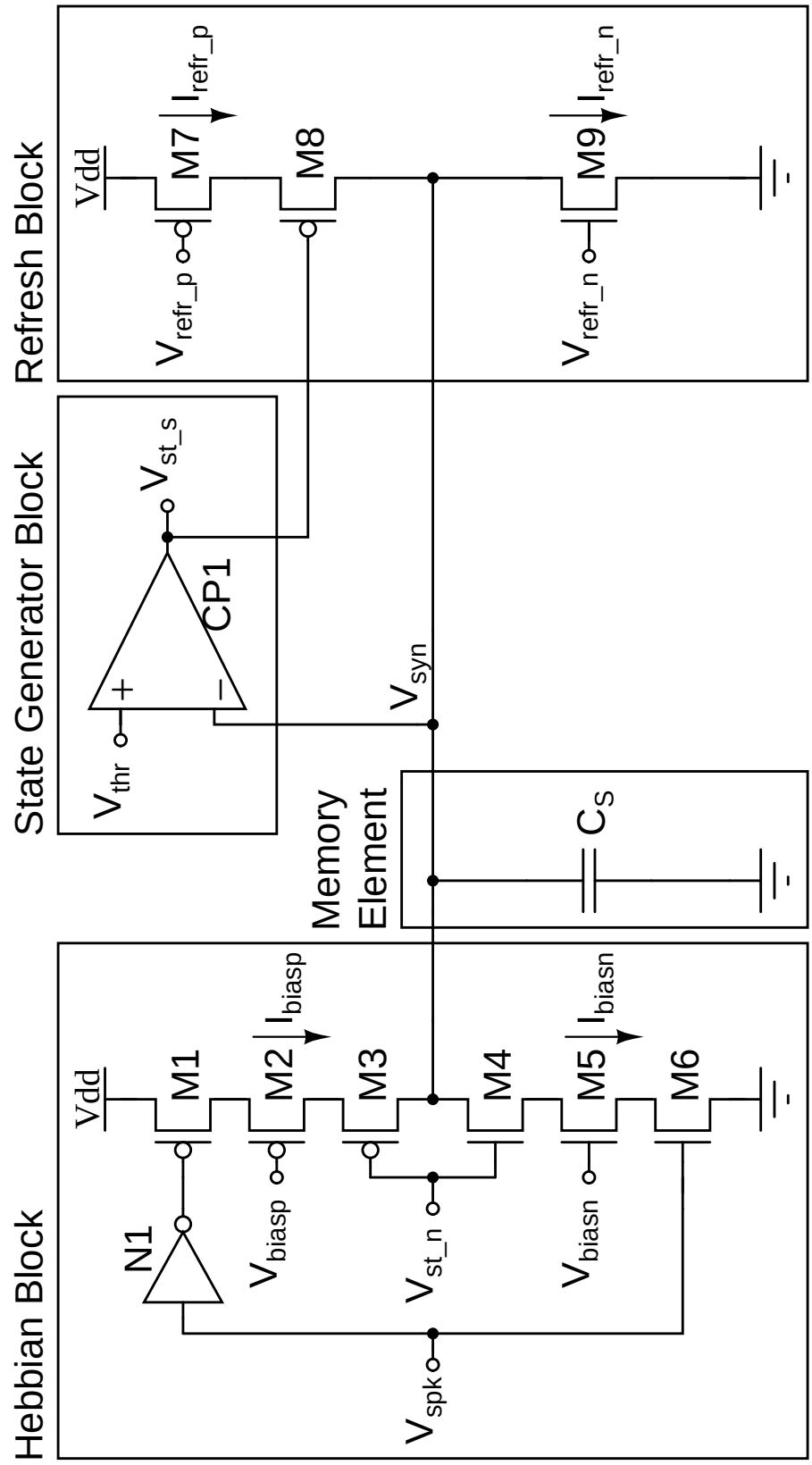
Hebbian Block
Vdd
M1
M2
M3
M4
M5
M6
N1
I_{biasp}
I_{biasn}
V_{biasp}
V_{st_n}
V_{biasn}
V_{spk}
Memory Element
C_S
State Generator Block
V_{st_s}
CP1
V_{thr}
V_{syn}
Refresh Block
Vdd
M7
M8
M9
I_{refr_p}
I_{refr_n}
V_{refr_p}
V_{refr_n}

Fig. 4.

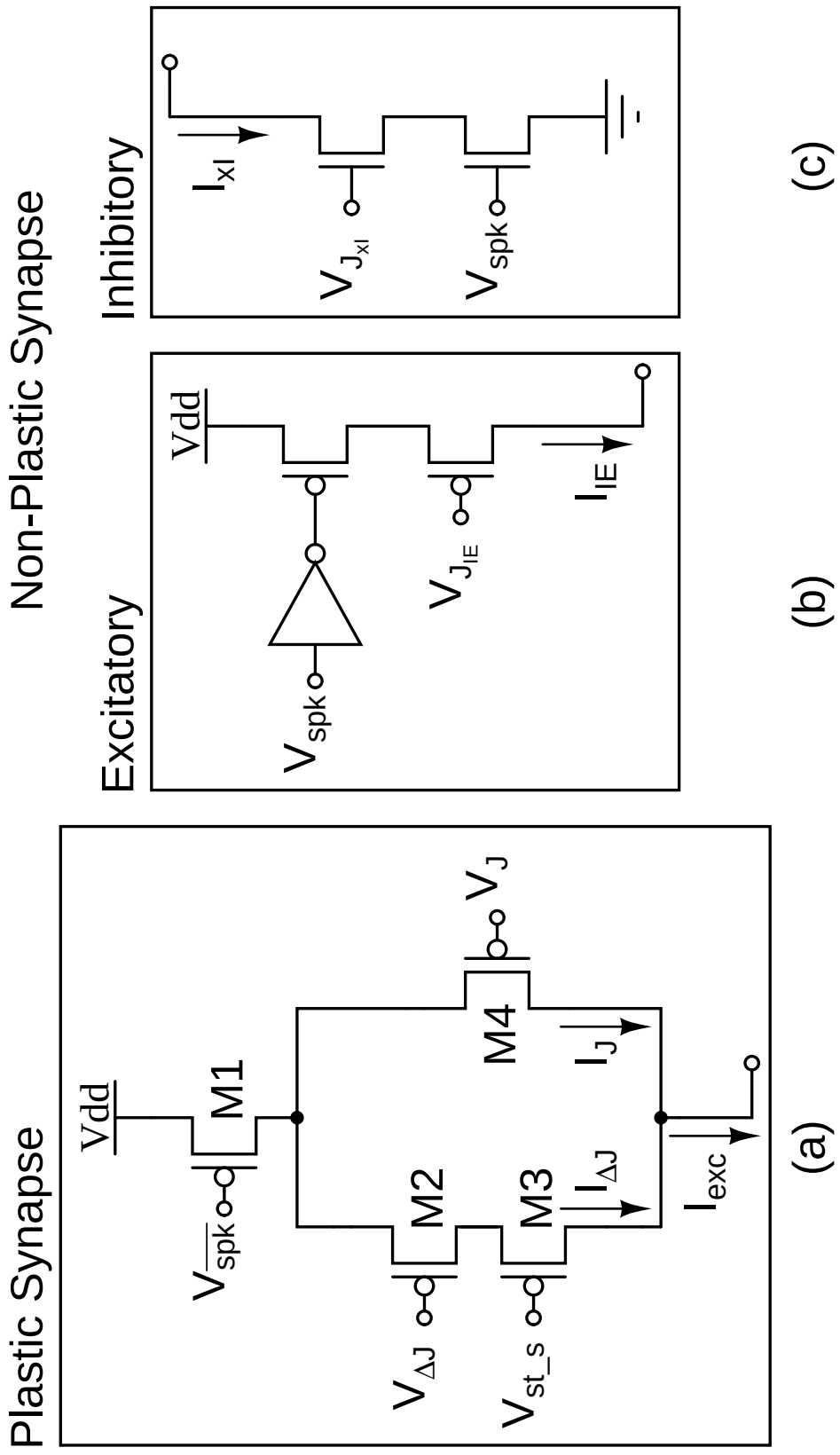
Plastic Synapse
Vdd
M1
M2
M3
M4
$V_{\overline{spk}}$
$V_{\Delta J}$
V_{st_s}
V_J
I_J
$I_{\Delta J}$
I_{exc}
(a)
Non-Plastic Synapse
Excitatory
Vdd
V_{spk}
$V_{J_{IE}}$
I_{IE}
(b)
Inhibitory
I_{xI}
$V_{J_{xI}}$
V_{spk}
(c)

Fig. 5.

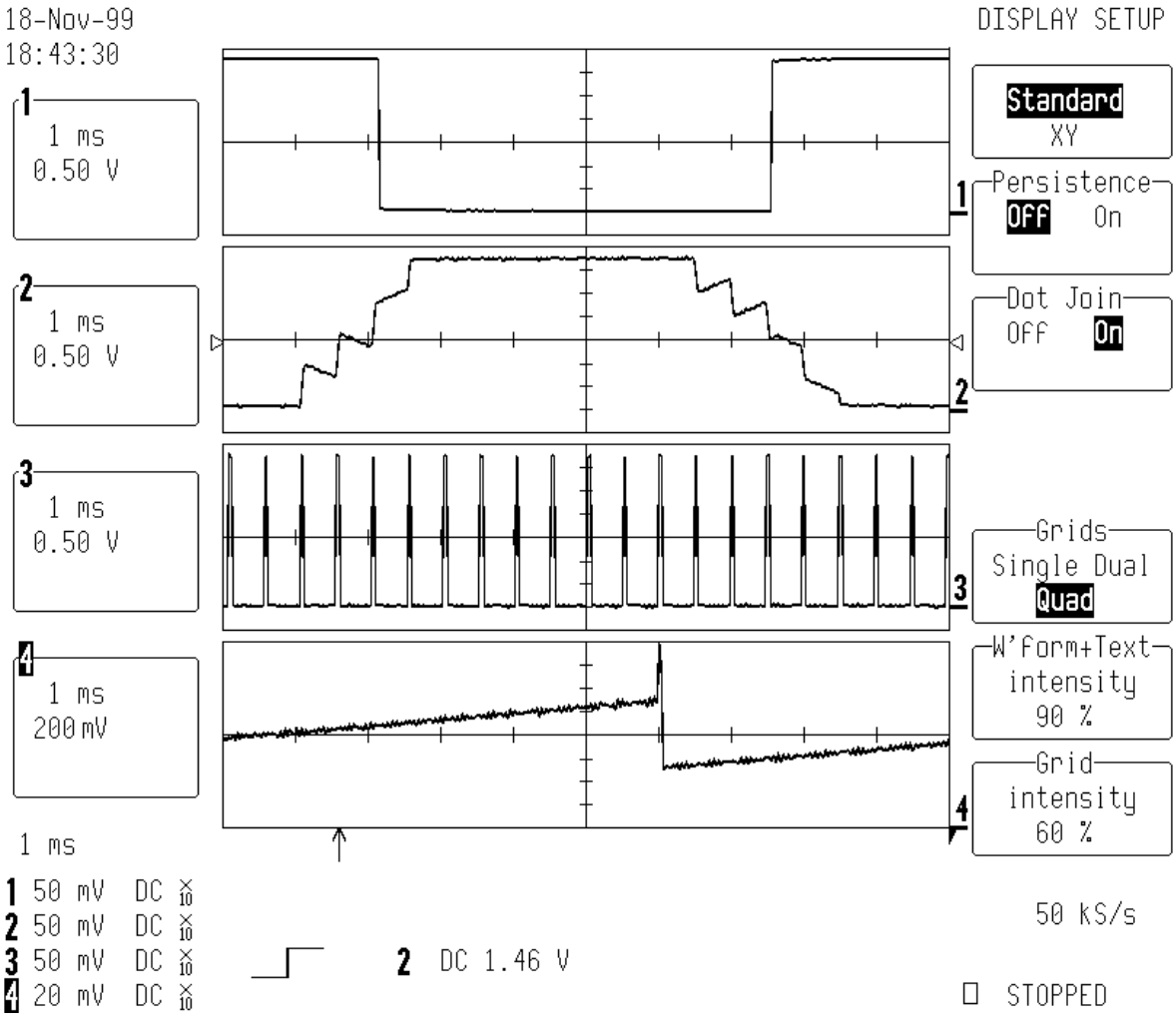
18-Nov-99
18:43:30
DISPLAY SETUP
1 ms
0.50 V
1 ms
0.50 V
1 ms
0.50 V
1 ms
200 mV
Standard
XY
Persistence
Off On
Dot Join
Off On
Grids
Single Dual
Quad
W'form+Text
intensity
90 %
Grid
intensity
60 %
1 ms
1 50 mV DC
2 50 mV DC
3 50 mV DC
4 20 mV DC
2 DC 1.46 V
50 kS/s
STOPPED

Fig. 6.

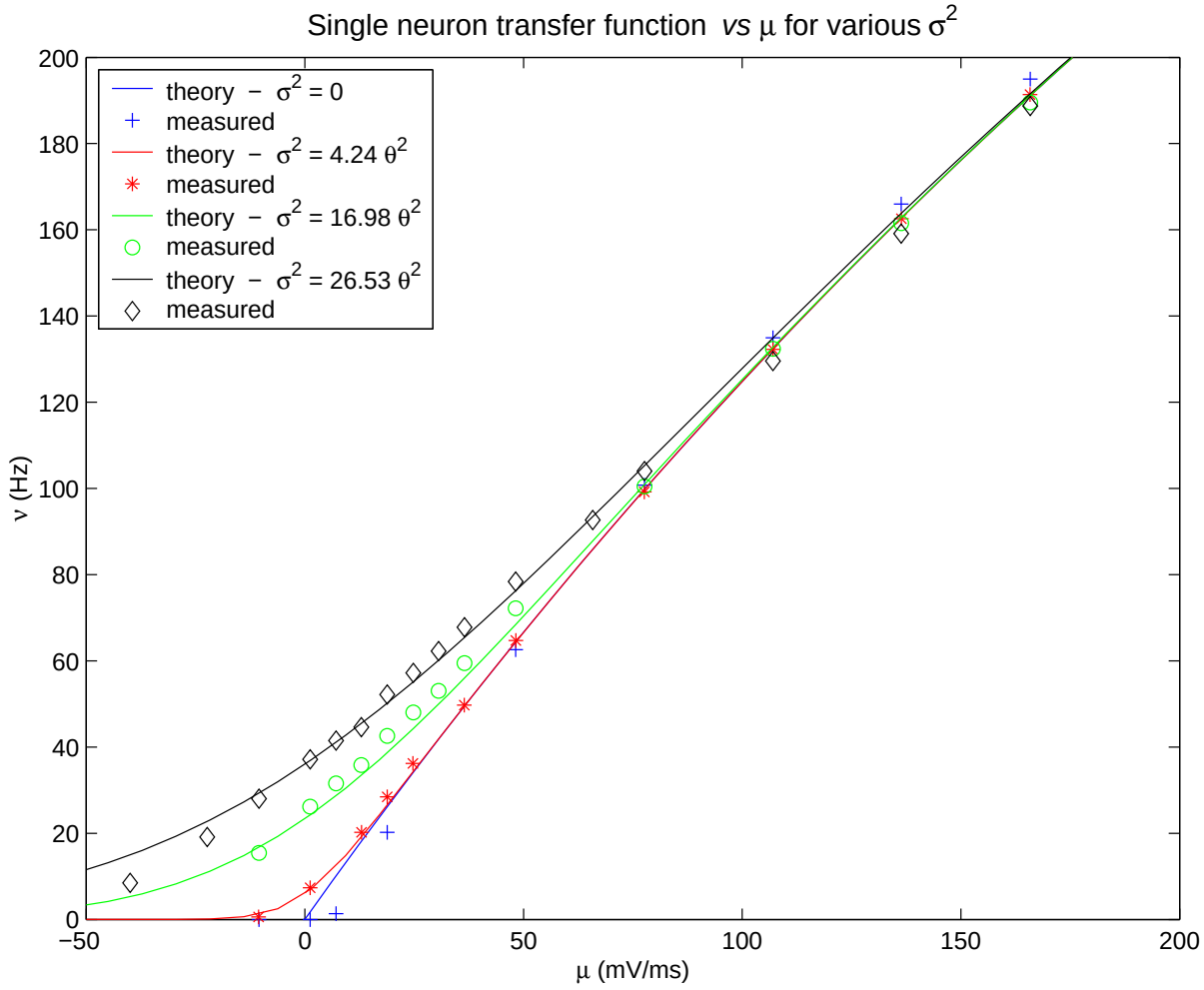
Single neuron transfer function vs μ for various σ2
theory − σ2 = 0
measured
theory − σ2 = 4.24 θ2
measured
theory − σ2 = 16.98 θ2
measured
theory − σ2 = 26.53 θ2
measured
ν (Hz)
μ (mV/ms)
200
180
160
140
120
100
80
60
40
20
0
−50
0
50
100
150
200

Fig. 7.

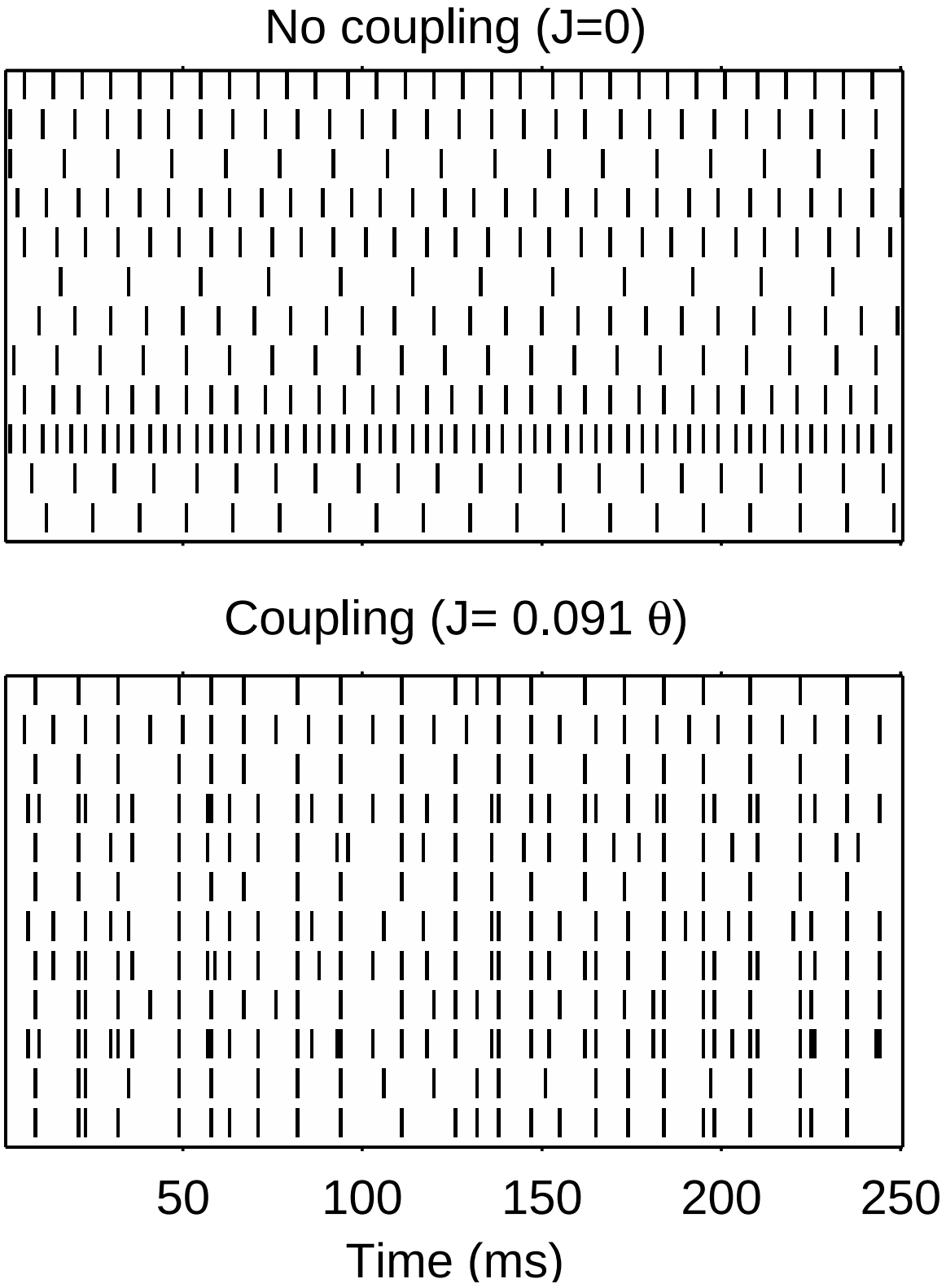

Fig. 8.