Low Power Low Noise Amplifier (LNA) design in 45nm CMOS

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Abstract

Low Noise Amplifier(LNA) is an electronic amplifier that amplifies low signals without degrading the signal to noise ratio. When using CMOS amplifiers, the input signal not only increases but noise from the circuit and external components. LNA are designed to prevent the amplification of noise and the use proper impedance matching and designing the capacitors/inductors to resonate at the design frequency prevent the amplification of noise and ensure maximum gain. LNA are most commonly found in Radio Frequency IC design. They are typically the first component in the receiver chains to amplify the incoming signal.

Introduction

In this paper we will present our calculations and simulation results for a fully functioning LNA. Figure 1 below shows the LNA that was designed in this paper. This LNA is a Cascoded Common-Source Amplifier with a current mirror intended.

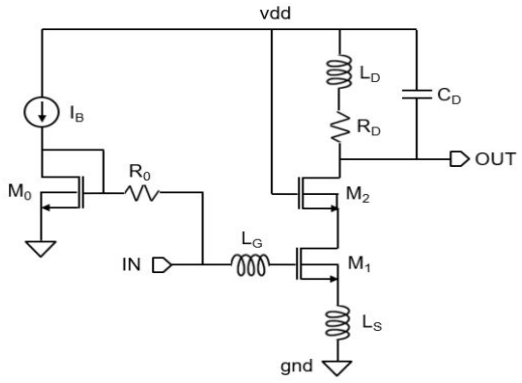

Figure 1. Low Noise Amplifier

Frequency Range	2.4 - 2.48 GHz
S11	< -15dB
S21	> 15dB
S22	< -15dB
Noise Figure.	< 2dB
Power	< 4mW
IIP3	> -20dBm

Table 1. Metrics of Target

Table 1. above shows the deliverable that we are needing to meet. This LNA will be operating at 2.4 - 2.48GHz, meaning that we set our design to 2.44GHz as the resonate metric. The purpose for Low Noise Amplifiers is for Radio-Frequency IC design, to amplify super small signals from something like a transmitter and amplify it for the rest of the system. The reason LNA is more popular for RF design than another conventional Common Source Amplifier is the signal to noise degradation. With LNA the signal to noise ratio is significantly better than the conventional CS Amplifier.

Design

The design on this LNA began with finding the input impedance for LNA which was done by using small signal analysis. The input impedance was determined to be,

$$Zin = \frac{1}{s*C_{gs}} + sL_G + \frac{gm*Ls}{C_{gs}}$$

For the purpose of matching we set the real part of the input equations to the following,

$$\frac{gm * Ls}{C_{gs}} = 50\Omega$$

Then by picking a reasonable size for Ls, for our design we decided to use 1nH we can use the following equation to determine w_t, with knowing Rs = 50. .

$$Rs = 50 = Ls * w_t$$

With a Noise Figure requirement of <2dB we chose a reasonable noise figure to determine the Conductance(gm) of the amplifier which is responsible for gain. The following equations help us determine the conductance needed.

$$gm = \frac{NF - 1}{Rs * \gamma (\frac{w_0}{w_t})^2}$$

Once the conductance is determined needed for the noise figure and input impedance, we can use the following equations to determine the gate to source capacitance.

$$C_{gs} = \frac{gm}{w_t}$$

using Cadence Virtuoso and using the model parameters of the gpdk045 transistors, we can find C_{ox} and k'. We can use the following equations to determine the width and length of the cascode transistors M1 and M2. The equations are as followed.

$$\frac{W}{L} = \frac{gm}{k'(Vdsat)}$$

$$WL = \frac{3C_{gs}}{2C_{ox}}$$

Finally to find the inductor value for L_G using the calculated value for Cgs and the value of Ls we picked to be 1nH we can find the value of L_G. Needing for this sections to be at resonance at 2.44GHz we use the following equations to find L_G.

$$L_G = L_T - L_s$$

$$L_T = \frac{1}{w_o^2 * C_{gs}}$$

Now that we have designed for the bottom portion of the LNA we need to design for the RL parallel C component on the upper sections of the LNA. We first convert the whole RLC to parallel to determine the Rp then will convert the resistance to series R. The following equations is the gain of the system.

$$Gain = \frac{1}{2} Qin * gm * Rp$$

From the first sections we can determine Qin with the following equation

$$Qin = \frac{w_o L_t}{Rs}$$

Now using the gain equation we can determine the resistance R_D.

$$R_p = \frac{2*Gain}{Qin*gm}$$

Now we can determine the last 3 components needed for the LNA, L_D, R_D, C_D. Choosing a reasonable inductor value for L_D to be 8nH. From here using the following equation to determine the Q of the top portion of the LNA and the converted series resistance .

$$Q = 2Qin$$

$$R_D = \frac{(w_o * L_s)^2}{R_p}$$

Then using the equation for resonance we can determine the last component needed for this amplifier. The equation is as follows

$$C_D = \frac{1}{w_o^2 * L_s}$$

This was the design procedure for the LNA circuit designed. Table 1 below shows the values we used and figure 2 and 3 shows the LNA circuit with the test bench.

gm	14.5 mS
W/L	150u/250n
Cgs	-241.773 fF
Ls	750 pf
Lg	14.5 nH
R	25
L	7.4 nH
C	510 pf

Table. 2. Circuit Component Values

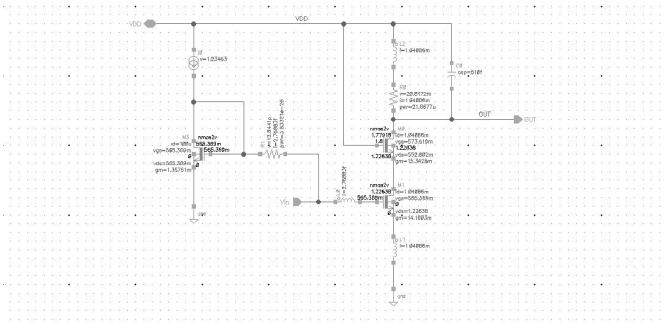

Figure 2. LNA Circuit

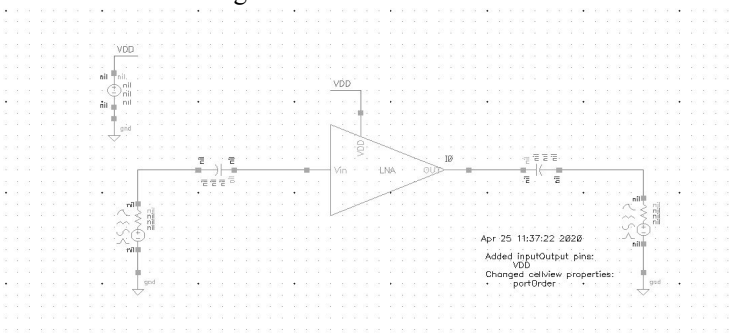

Figure 3. LNA Test Bench

Results

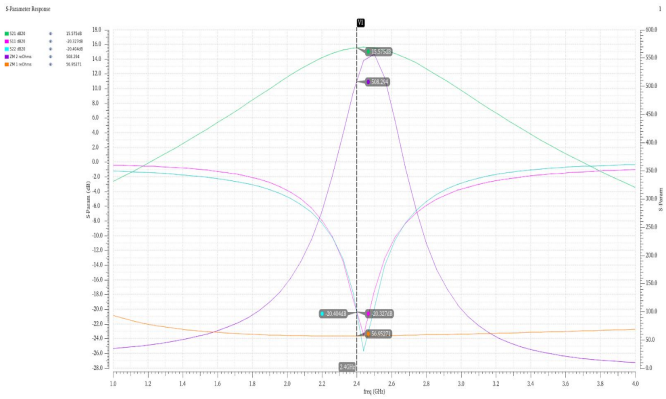

Figure 4. Spectrum Analysis

Av(S21)	**15.575 dB**
S11	**-20.327 dB**
S22	**-20.404 dB**
Z1(Real)	**56.9 reOhms**
Z2(Real)	**508.2 reOhms**
Power	**2.734 mW**

Table. 3 LNA Results

Figure 4 and table 3 shows the results for the LNA our group designed. Our specs were met with the requirements given to us. The overall gain of our system the S21 was 15.575 dB, with an S11 and S22 at about -20 dB each. S22 and S11 are the input and output reflection gain meaning that our circuit matching from 50 Ohms to 500 Ohms was a success.

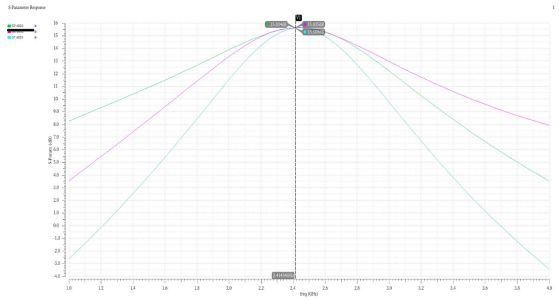

Figure 5. GT, GA, GP

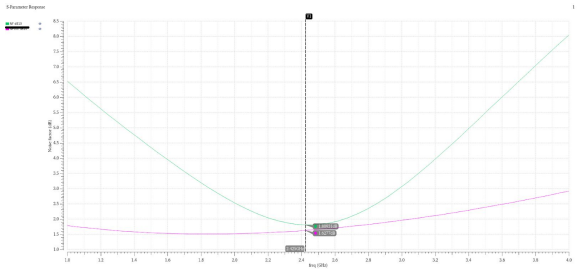

Figure *6.* Noise Figure

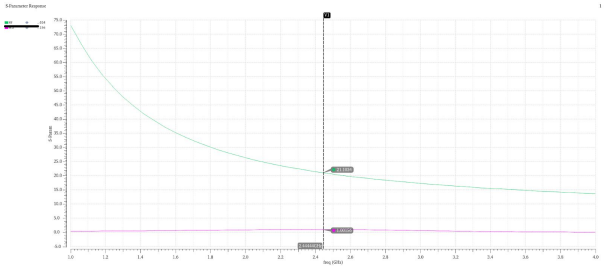

Figure 7. kf/B1f

GT	15.59 dB
GA	15.6 dB
GP	15.6 dB
NF	1.802 dB
NFmin	1.6277 dB
Kf	21.013
B1f	1.00156

Table. 4 Metrics

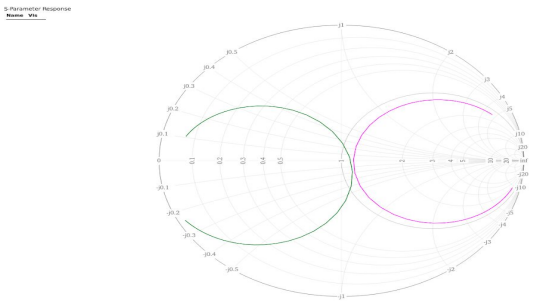

Figure 8. Smith Charts

Figure 8. above shows the Smith Chart of the impedance matching of the circuit. Our goal was to get an output impedance of 500 ohms from an input impedance of 50 ohms. Our circuit was a success as we were able to effectively match input to output.

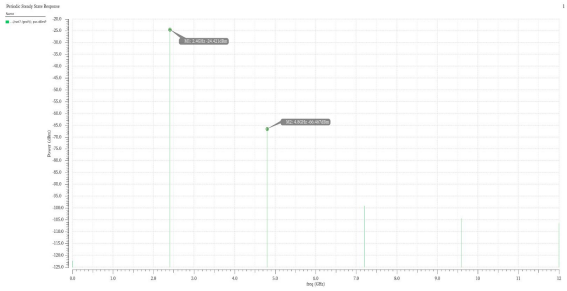

Figure 9. -40dBm PSS

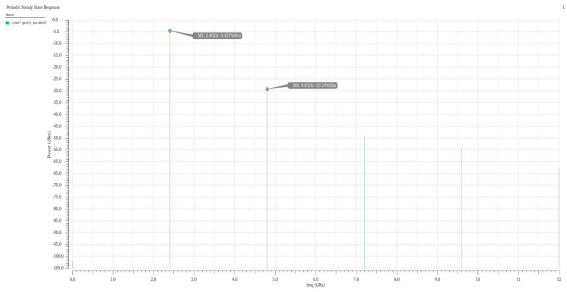

Figure 10. -20dBm PSS

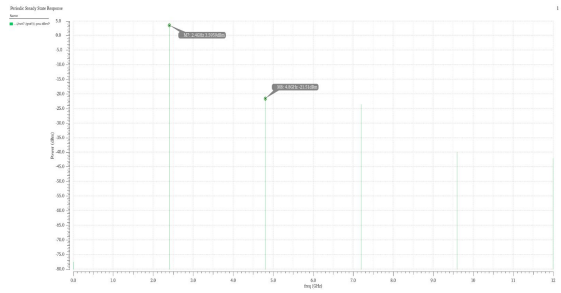

Figure 11. -10dBm PSS

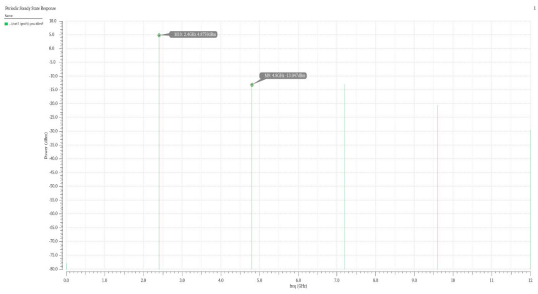

Figure 12. -5dBm PSS

Figures 9 to 12 shows the second and third Harmonics of the circuit when given a different prf ranging from -40 dBm to -5 dbm. Harmonics are due to non-linear loads at multiples of the fundamental frequencies. We try to keep these as small as possible and so that we do not disrupt other bands when designing in RF because they could be used. Our circuit underwent a test to determine the second and third harmonics to see the outcome. Our circuit harmonics are at spec after conducting the tests. Table 5 below shows the values we obtain from the Harmonic tests.

PSS	-40 dBm	2.4GHz	-24.421 dBm	4.8GHz	-66.6d Bm
PSS	-20 dBm	2.4GHz	-4.427 dBm	4.8GHz	-29.429 dBm
PSS	-10 dBm	2.4GHz	3.5959 dBm	4.8GHz	-21.51 dBm
PSS	-5 dBm	2.4GHz	4.8759 dBm	4.8GHz	-13.047 dBm

Table 5. Harmonics Test

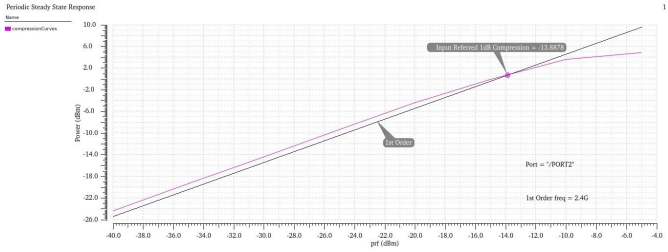

Figure 13. P1dB extrapolated from -40 dBm

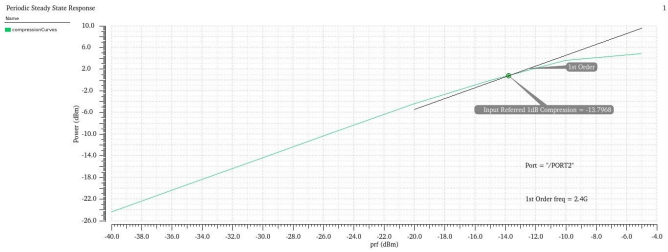

Figure 14. P1dB extrapolated from -20 dBm

Figures 13 to 14 shows the results of P1dB extrapolated from -40 dBm and -20 dBm when given a different prf ranging from -40 dBm to 0 dBm. The circuit's specs were met with the requirements given to us. The overall input referred to 1dB compression is -13.8878 dBm with the first order frequency equals 2.4GHz at -40 dBm and -13.7968 dBm with 2.4GHz at -20dBm. When we plot the gain (log scale) as a function of the input power, we identify the point where the gain has dropped by1 dB. This is the 1dB compression point and our generated results for the input referred to 1dB compression were successful.

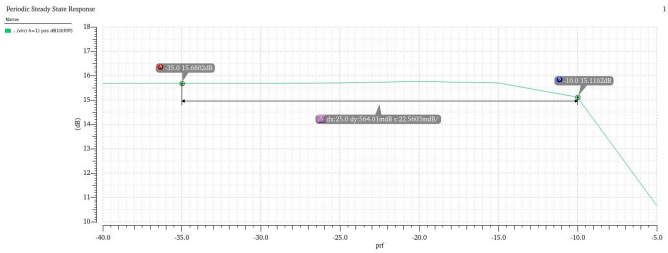

Figure 15. Power Gain

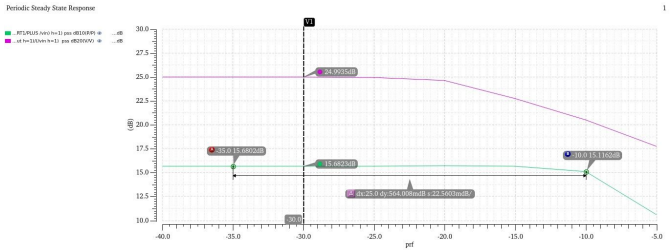

Figure 16. Voltage Gain vs. Power Gain

Figure 15 to 16 shows the results of power gain for our LNA circuit and the comparison between voltage gain and power gain. The power gain maintained 15.6802 dB at prf equals -35 dBm and slowly dropped to 15.1162 dB at prf equals -10 dBm. The voltage gain was 24.9935 dB while the power gain was 15.6823 dB at the specific prf value equals -30 dBM. Our power gain and voltage gain specs were successfully met with the requirements given to us.

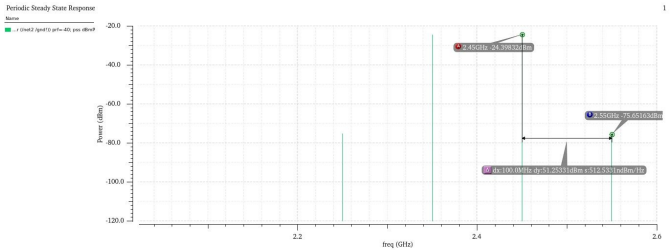

Figure 17. Two-tone pss simulation

Figure 17 shows the result of two-tone periodic steady state(pss) simulation. PSS simulation is used to find a steady-state response of a periodic circuit. In the waveforms above, the power equals -24.39832 dBm for the harmonic at 2.45GHz and -75.65163dB at 2.55GHz. Our specs were met with the requirements given to us.

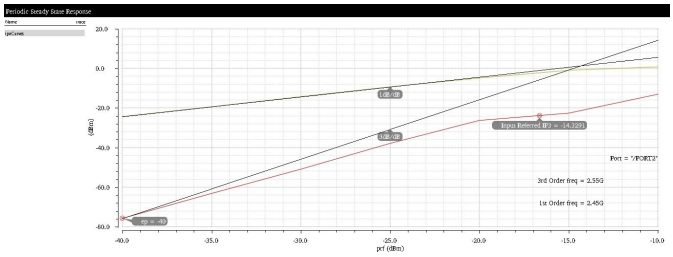

Figure 18. Extrapolated IP3

Figure 18 shows the results of extrapolated IP3 when given a different prf ranging from -40 dBm to -10 dbm. The circuit's specs were met with the requirements given to us. The ep value is -40 and the input referred IP3 equals -14.3291. The extrapolated point where the curves of the fundamental signal and third order distortion product signal meet is the Intercept Point (IP3). Our testing result for the extrapolated IP3 was a success.

Summary

This project was all encompassing of our learning this year in EE 220 RFIC. We designed and implemented a fully functioning Low Noise Amplifier from start to finish. The LNA was a success meeting all target specifications that were required of us. Our amplifier was successfully matched input and output to ensure maximum gain and achieving an overall gain of 15.575 dB. We were able to keep overall power low on the system by keeping it at 2.7mW and still meeting all our power metrics that were required of us.

References

[1] B. Razavi, RF Microelectronics. Upper Saddle River, NJ: Prentice Hall, 1998.

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[3] V. Wright, Circuit Analysis. New York: Nova Science Publishers, 2011.

[4] R. A. Rafla and M. N. El-Gamal, "Design of a 1.5 V CMOS integrated 3 GHz LNA,"Proceedings of the 1999 IEEE International Symposium onCircuits and Systems, vol.2, pp. 440-443, 1999.

[5] J. C. Huang, R. Weng, et al., "A 2 V 2.4 GHz fully integrated CMOS LNA,"The 2001 IEEE International Symposium onCircuits and Systems, vol. 4, pp. 466-469, 2001.

[6] X. Yang, T. Wu, et al., "Design of LNA at 2.4 GHz using 0.25 /spl mu/m technology," Silicon Monolithic Integrated Circuits in RF Systems, pp. 12-17, 2001.

Question and Answer

1) Describe each transistor and passive component in the LNA?
   a) Transistor M2 on the left is the current mirror that we used in this circuit. The purpose of the current mirror is to copy or “Mirror” the current through one trasistor to another. The purpose of M1 the bottom transistor of the cascode is the Main transistor, this is what takes in the input and with M1 the top cascode resistor amplifies the input signal. The inductor Lg and Ls are intended to be used in conjunction with the transistor Cgs

2) Describe how the input and output match are implemented in the design?
   a) For the design we are given an input and output to match to and from depending on the implementation of the circuit. Using the inductor and capacitors we use the equation of resonance to find the values of L and C to resonate at the operating frequency. Also when looking at the input impedance the tail inductor and capacitance are what determine the input impedance. It is due to non-idealities of the 2 passive components.

3) After DC analysis calculated theoretical Gain, NF, and input impedance of LNA. Are the values different than the S-Parameter simulation
   a) Av = 16.37 dB
   b) NF = 1.84
   c) Input Impedance: 43.5 Ohms
   d) When comparing the calculated theoretical response and compared to the simulated results the Noise Figure calculation was spot on however the gain and the Input impedance were slightly different. This is probably due to having to change component sizes slightly to obtain results that were inline with the specs given to the group.

4) Run SP and record S11, S21, S22, ZM1, ZM2
   a) Recorded in the report above.
5) From SP analysis record NF.
   a) Recorded in Design.
6) What is the power gain of the LNA for the fundamental tone? What is the HD2 and HD3? How do these three parameters change for input power of -40dBm, -20dBm and -5dBm?

a) The power gain of the LNA for the fundamental tune = 15.579 dB with Pin = -40 dBm.

b) The power gain of the LNA for the HD2 = -26.6 dB with Pin = -40 dBm. The power gain of the LNA for the HD3 = -58.2 dB with Pin = -40 dBm.

c) When Pin = -40 dBm, the power gains for the fundamental tune, HD2 and HD3 are shown above in the part(a) and part(b). When Pin = -20 dBm, the power gains for the fundamental tune, HD2 and HD3 are 15.573 dB, -9.429 dB and -32.817 dB. When Pin = -5 dBm, the power gains for the fundamental tune, HD2 and HD3 are 9.8759 dB, -8.047 dB and -8.521 dB.

7) From the above simulation results, what is the IIP3 of this LNA?

a) IIP3 = $\sqrt{\frac{4*\alpha_1}{3*\alpha_3}}$ = -14.1 dBm.

8) How does the extrapolated IIP3 compare with your calculation from Q7? Is the difference between the 1dB compression point and the IIP3 what you would expect?

a) IIP3 in the extrapolated IIP3 = -14.3 since the extrapolated point where the curves of the fundamental signal and third order distortion product signal meet is the Intercept Point (IP3). At this point, then, by definition IM3 = 0 dBc. The input power level is known as IIP3, and the output power when this occurs is the OIP3 point. The difference between Q7 and Q8 answers are expected because we use the values only at the input power equals -40 dBm.