Date 05-08-19

Expt. No. 1 Page No. 2

Experiment No :- 1

Aim :- Introduction to 8085 microprocessor and MP kit.

Apparatus :- 8085 μP EXCEL kit.

Theory :-

- **Evolution of microprocessors :-** Evolution of microprocessors are divided into five categories :-

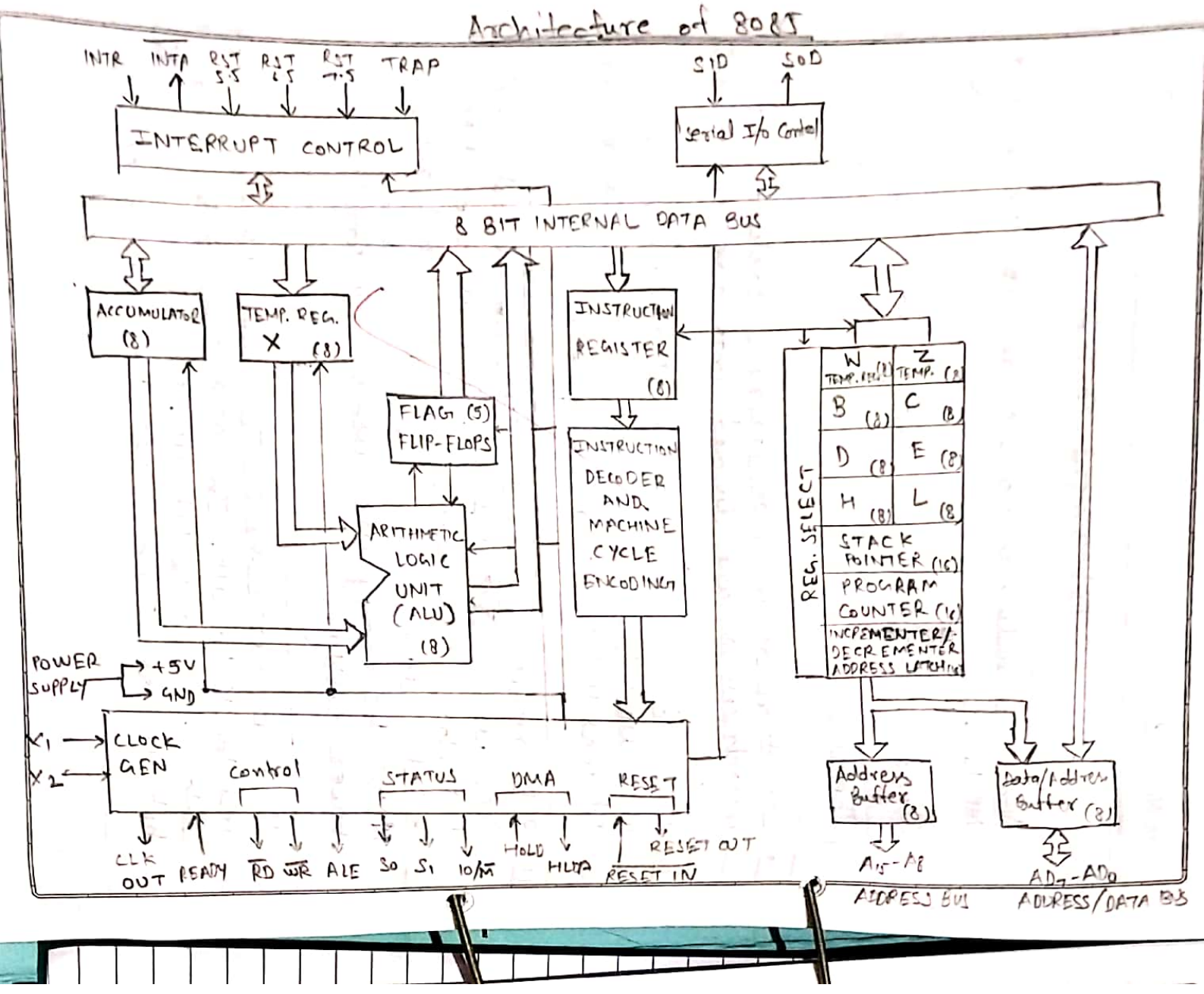
(i) **4 bit microprocessors :-** The Intel 4004 was the first μP introduced in 1971 by Intel corporation. It was 4 bit PMOS microprossear.

(ii) **8 bit microprocessors :-** In 1973, introduced Intel 8008 its first 8 bit μP. This μP uses PMOS technology. In 1975, Intel developed another 8 bit μP. It was Intel 8085 which uses NMOS technology and uses only single +5V power supply.

(iii) **16 bit microprocessors :-** The 8 bit μP's were followed by 16 bit μP. In 1978, Intel introduced Intel 8086, a 16 bit μP. Example of other 16 bit μP are Intel 80186, Motorola 68000 etc.

Teacher's Signature : _____

Architecture of 8085



(iv) 32 bit microprocessors :- Now-a-days microcomputers are now built with 32 and 64 bit µPs. Intel 80386, a more powerful 32 bit µP was developed by Intel in 1985. 32 bit µPs are being used for data processing and computer graphics applications in desktop computers.

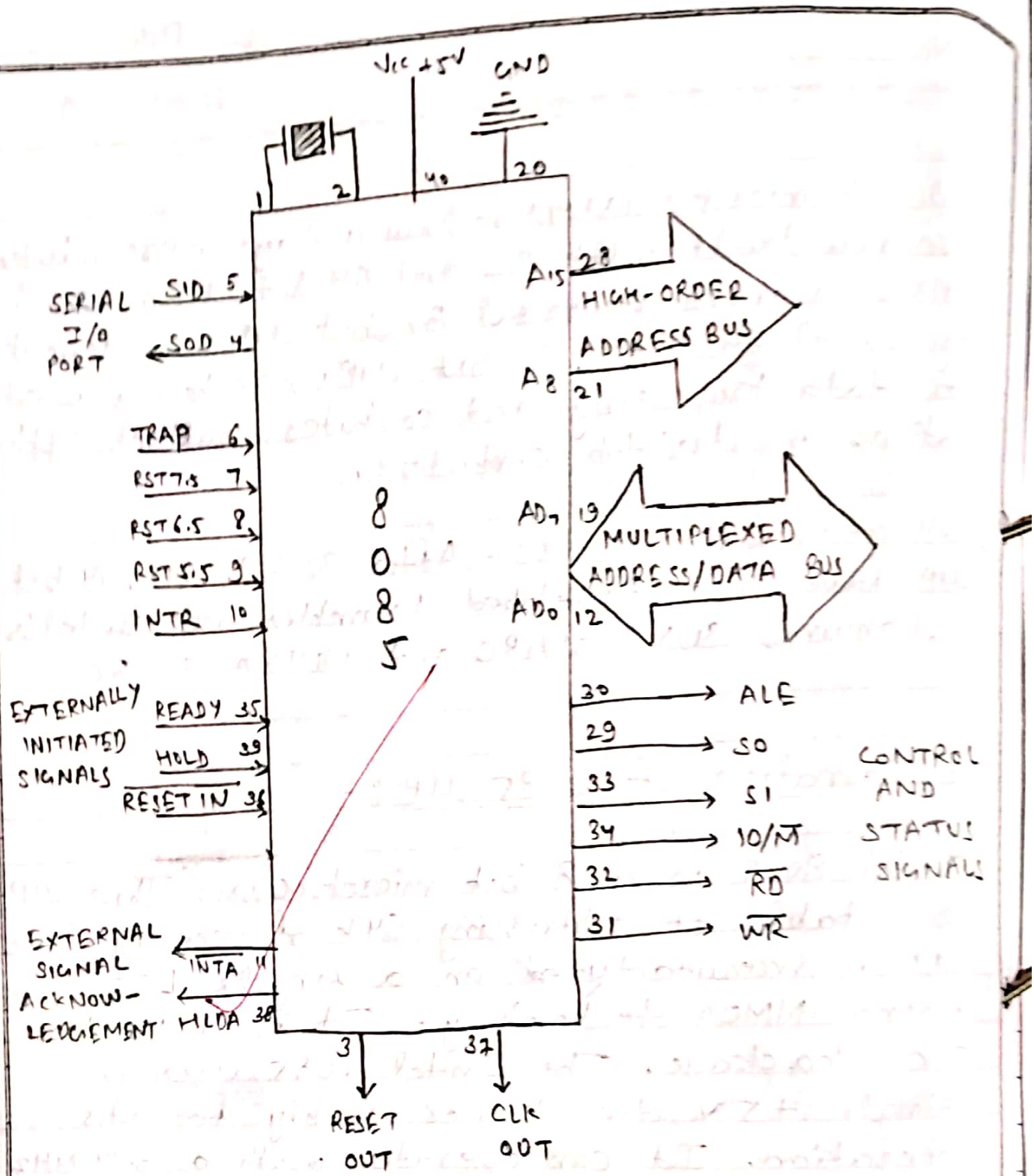
(v) 64 bit microprocessors :- After 32 bit µPs, 64 bit µP have been developed. Examples are Intel's Itanium, SUN'S SPARC and ULTRA SPARC.

- Explaination of 8085 µP :-

Intel 8085 is a 8 bit microprocessor. This µP is capable of addressing 64k of memory. This µP is manufactured on a single L.S.I chip using NMOS technology. It is a 40 pin IC package. The Intel 8085 uses a single +5V d.c power supply for its operation. It can operate with a 3.14 MHz single phase clock. The clock cycle is of 320 µ sec.

8085 µP has 8 data lines AD_7-AD_0 which is combined with lower address lines and 8085 has 16 address lines A_{15}-A_0.

Teacher's Signature : _____



Functional diagram of 8085

Date _____

Expt. No. _____ Page No. 4

Introduction to kit :-

ET-8085 AD-LCD is a Microprocessor training cum development kit designed around 8085 processor which is still the most popular in India. 8085 is a very versatile processor and it is easy for the students to understand its architecture and assembly language programming. In India 8085 processor is still considered the first step for the students to understand the microprocessor technology.

System Specification (Hardware):

CPU	:- 8 bit µP the 8085.
XTAL Frequency	:- 6.144 MHz.
RAM	:- 8k bytes with provision for expansion Battery Back up for RAM (optional)
EPROM	:- 16k/32k bytes of EPROM with the provision for expansion
MEMORY	:- Total on board capacity of 64k bytes.
TIMER	:- Three 16 bit programmable Counters using 8253
I/O LINES	:- 48 I/O lines using Two Nos. of 8255
INTERRUPTS	:- 8 interrupts lines through 8259.

Teacher's Signature : _____

Date _____

Expt. No. _____ Page No. 5

SERIAL INTERFACES :- RS232 through SID & SOD Lines.

OTHER INTERFACES :- Additional RS232C through 8251 USART
a) A/D Converter I/F
b) D/A Converter I/F
c) Relay I/F
d) Opto Isolated Input I/F
e) Printer I/F
f) Real Time clock (optional)

KEYBOARD :- 101/104 Keys ASCII Keyboard

DISPLAY :- 20*2 LCD display (20*4 optional)

BUS :- All data, address and control signals (TTL) available at 50 pin FRC connector.

POWER SUPPLY :- (optional)

REQUIREMENT :- +5V, 1.5 Amp for the kit & Serial I/F, +/- 12V for Aux Serial I/F, +12V, +21V, +24V for programming.

OPERATING TEMPERATURE :- 0 TO 50°C

Teacher's Signature : _____

Date _____

Expt. No. _____ Page No. 6

- 8255 (Programmable Peripheral Interface) :-
8255 is a programmable peripheral interface (PPI) designed to use with 8085 uP. This basically act as a general purpose I/o device to interface with peripheral devices.

- 8253 (Programmable Interval Timer) :-
This chip is a programmabl interval timer/counter and can be used for generation of accurate time delays under software control.

- 8251 (USART) :-
This chip is a programmable communication interface and is used as a peripheral device. This device accepts data character from CPU in parallel format and then convert them into serial data characters for the CPU.

- 8259 (Interrupt Controller) :-
The 8259 is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages 8 level of requests and has built in features for expandability to other 8259's. It is programmed by system's software as an I/O peripheral.

Teacher's Signature : _____

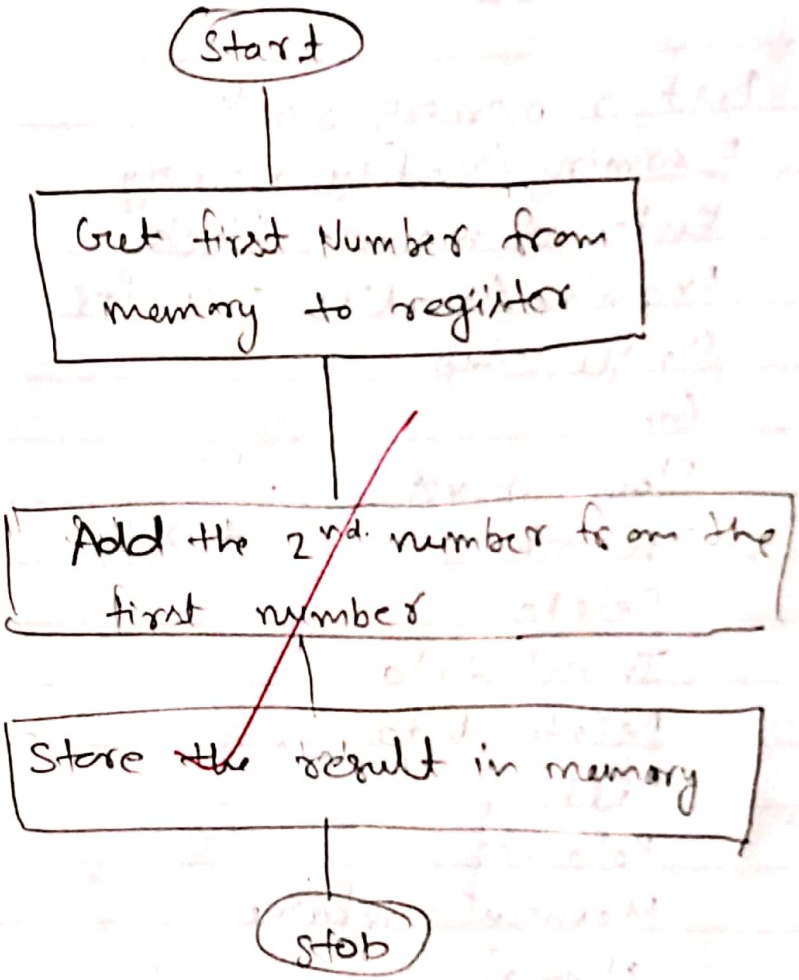
Date

Expt. No. Page No. 7

- List of Commands :-

1.	L	List a memory block
2.	M	Examine / Modify memory
3.	E	Enter a memory block
4.	R	Examine / Modify register
5.	S	Single step
6.	G	Go
7.	B	Block move
8.	I	Insert
9.	D	Delete
10.	N	Insert data
11.	O	Delete data
12.	F	Fill
13.	H	Relocate
14.	J	Memory Compare
15.	K	String
16.	P	Print
17.	I	Assemble / Disassemble

Teacher's Signature :



Date 19-08-19

Expt. No. _____ Page No. 8

Experiment No :- 2

Aim :- Write a program to add two numbers.
(a) Sum 8-bit with and without Carry.
(b) Sum 16-bit with and without carry.

Program :-

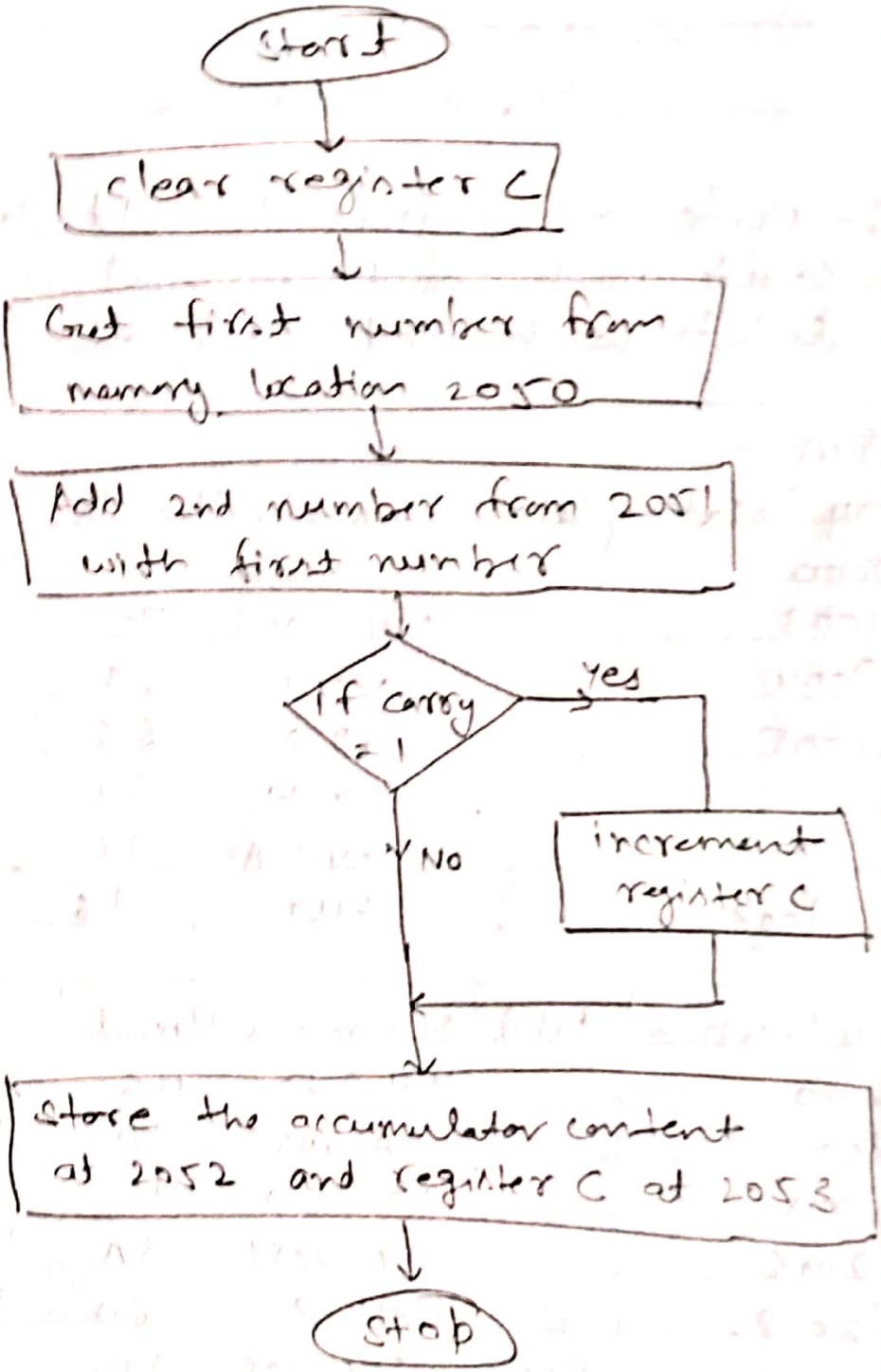
(a)

Memory location	label	Mnemonics	Hex code	T-state	Comment
2000		LXI H, 2050	21	10 T	
2003		MOV A, M	7E	7 T	
2004		INX H	23	6 T	Inc. by one
2005		ADD M	86	7 T	Add the No
2006		INX H	23	6 T	
2007		MOV M, A	77	7 T	Move to memory
2008		HLT	76	5T	End the progr

(b)

Memory location	label	Mnemonics	Hexcode	T-State	Comments
2000		MVI C, 00	0E	7 T	
2002		LDA 2050	3A	13 T	Load the acc.
2005		MOV B, A	47	7 T	Move the data A to B
2006		LDA 2051	3A	13 T	
2008		ADD B	80	4 T	
200A	200E	JNC 200E	D2	10 T	
200D		INR C	0E	4 T	Increment C
200E		STA 2052	32	13 T	
2011		MOV A, C	79	7 T	
2012		STA 2053	32	13 T	
2015		HLT	76	5T	

Teacher's Signature : _____



Date _____

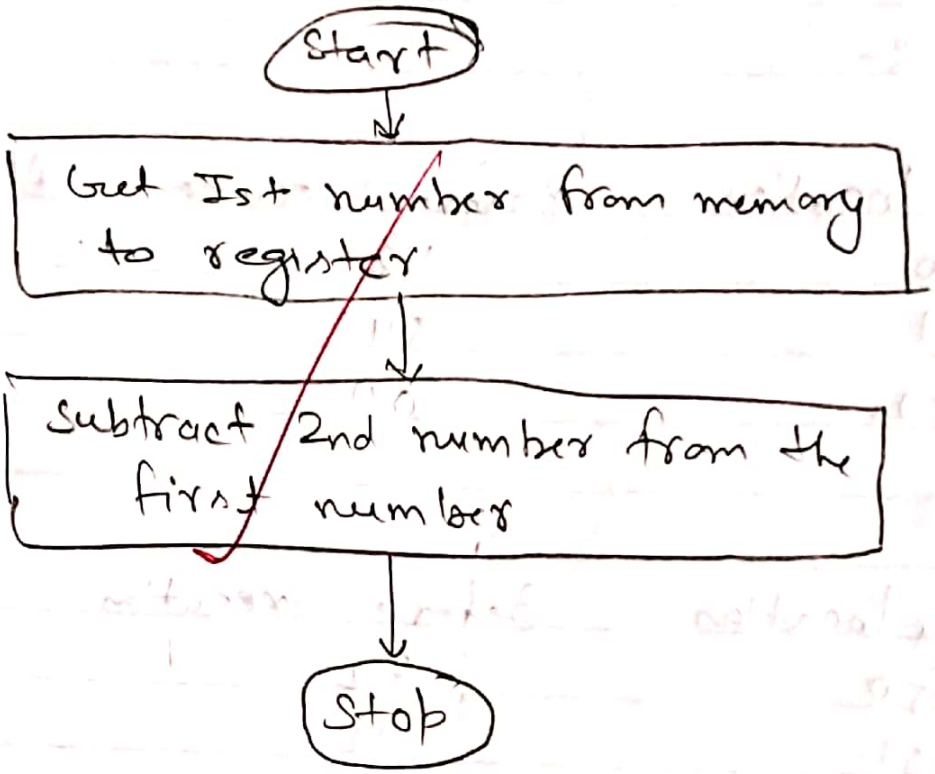
Expt. No. _____ Page No. 1

Result :-

Memory location	Before Execution	After Execution
2050	42	42
2051	54	54
2052	00	96

Memory location	Before Execution	After Execution
2050	F2	F2
2051	12	12
2052	00	04
2053	00	01

Teacher's Signature : _____



Date 16.08.17

Expt. No. _____ Page No. 10

Experiment No :- 3

Aim :- Write a program to subtraction of two numbers

(a) Subtraction of 2 8-bit Numbers.

(b) Subtraction of 2 16-bit Numbers

Program :-

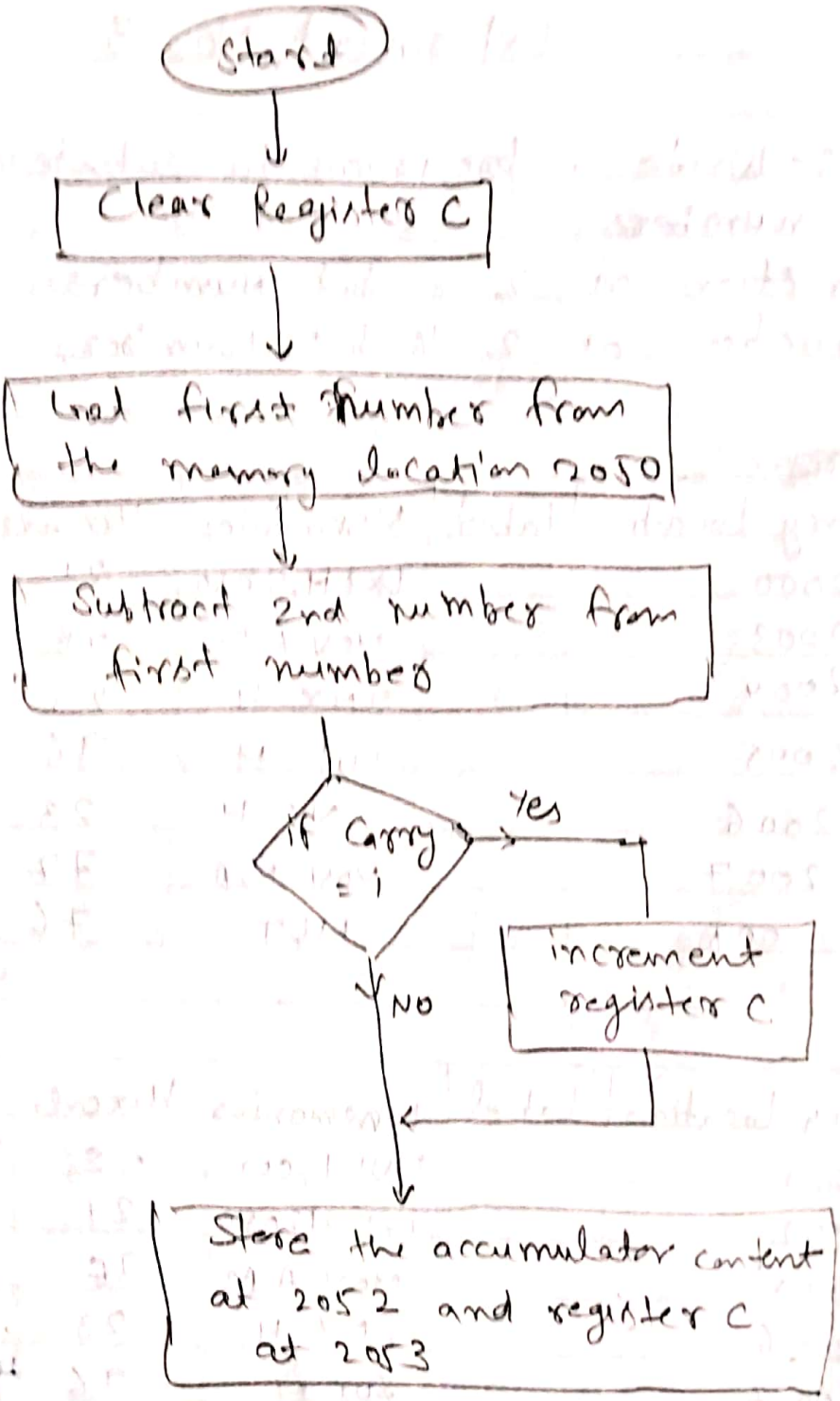
(a)

Memory location	label	Mnemonics	Hexcode	T-state	Comments
2000		LXI H,2050	21	10 T	
2003		MOV A,M	7E	7 T	
2004		INX H	23	6 T	
2005		SUB M	96	7 T	
2006		INX H	23	6 T	Inc. by one
2007		MOV M,A	77	7 T	
2008		HLT	76	5 T	

(b)

Memory location	label	Mnemonics	Hexcode	T-state	Comments
2000		MVI L,00	0E	7 T	set c to 0.
2002		LXI H2050	21	10 T	
2005		MOV A,M	7E	7 T	
2006		INX H	23	6 T	
2007		SUB M	96	4 T	
2008		JNC 200C	02	7/10 T	10/7
200B		INR C	0C	6 T	Inc in C
200C		INX H	23	7 T	
200D		MOV M,A	77	6 T	

Teacher's Signature : _____



200E		INX H	23	6T
200F		MOV M,C	77	7T
2011		HLT	76	5T

Result

(a)

Memory location	Before Execution	After Execution
2050	33	33
2051	10	10
2052	00	23

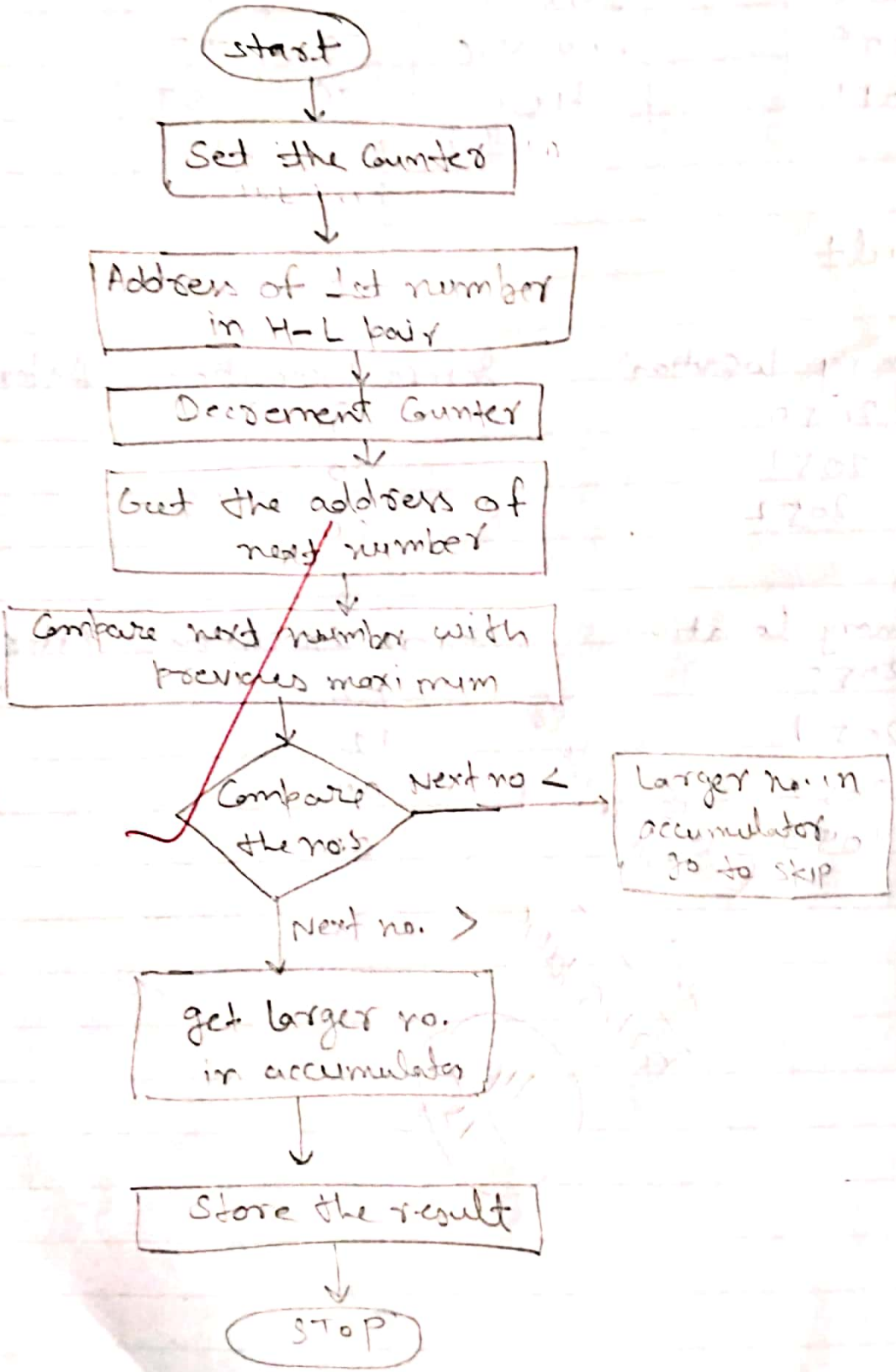
(b)

Memory location	Before Execution	After Execution
2050	F2	F2
2051	12	12
2052	00	E0
2053	00	00

Result incomplete

02/05/2018

14/15



Flow chart of find larger number

DELTA Pg No. 12
Date 02/09/19

Experiment No:- 4

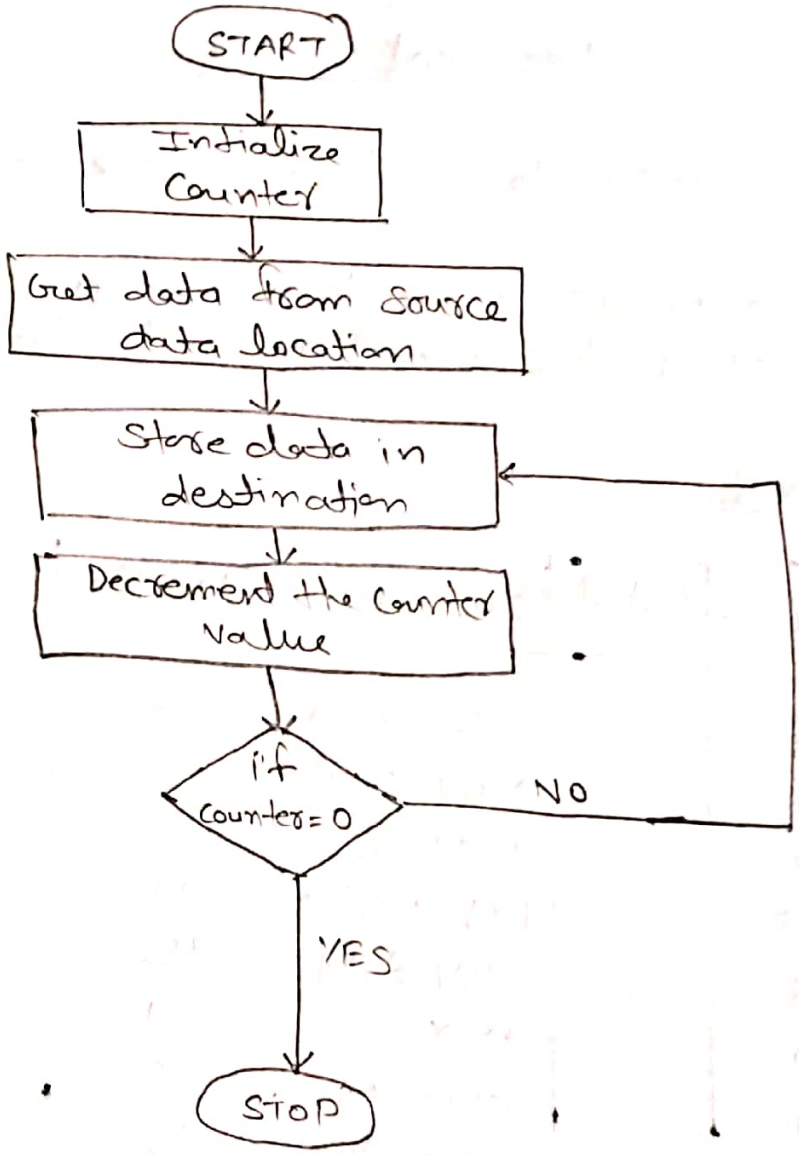
Aim :- (a) W.A.P to find largest number in a given array.

(b) W.A.P to move a block of data from one selection of memory to another selection of memory.

Program :-

(a)

Memory location	Label	Mnemonics	Hexcode	T-state	Comments
2000		LDA 2050	3A	13 T	Load the acc.
2003		MOV C, A	4F	4 T	Move the A to C
2004		DCR C	0D	4 T	Decrement C.
2005		LXI H 2600	21	10 T	Load Immediate H-L
2008		MOV A, M	7E	7 T	Move memory to A
2009		INX H	24	6 T	Increment H-L
200A		CMP M	BE	4 T	Compare M with A
200B	200F	JNC 200F	D2	10 T	Jump if No carry.
200E		MOV A, M	7E	7 T	Move memory to A.
200F		DCR C	0D	4 T	Decrement C.
2010	2009	JNZ 2009	C2	10 T	Jump if No zero
2013		STA 2100	32	13 T	Store the content of A
2016		HLT	76	5 T	stop the Execution



Flow chart of move data from one memory block to another memory block

DELTA Pg No. 13
Date / /

(b)

Memory location	Label	Mnemonics	Hexcode	T-state	Comments
2000		MVI L,0A	2E	7T	Move immediate data
2002		LXI B2100	03	10T	Load immediate B with add.
2005		LXI D 2150	11	10T	Load immediate D with ad
2008		LDAX B	0A	7T	Load acc. with B C
2009		STAX D	12	7T	store the acc. to D E
200A		INX B	03	6T	Increment B-C pair
200B		INX D	13	6T	Increment D-C pair
200C		DCR L	2D	4T	Decrement L.
200D	2008	JNZ 2008	C2	10T/7T	Jump if No zero
2010		HLT	76	5T	Stop the Execution

Result :-

(a)

Memory Location	Before Execution	After Execution
2050	0A	0A
2600	15	15
2601	18	18
2602	11	11
2603	29	29
2604	1F	1F
2605	2E	2E
2606	3A	3A
2607	12	12
2608	2C	2C
2609		

2009	10	10
2100	00	3A

(b)

Memory location	Before Execution	After execution
2050	0A	0A
2100	15	15
2101	18	18
2102	11	11
2103	29	29
2104	1F	1F
2105	2E	2E
2106	3A	3A
2107	12	12
2108	2C	2C
2109	1D	1D
2150	00	15
2151	00	18
2152	00	11
2153	00	29
2154	00	1F
2155	00	2E
2156	00	3A
2157	00	12
2158	00	2C
2159	00	1D

Sap 09/09/2019.

DELTA Pg No. 15
Date 09/09/19

Experiment No:- 5

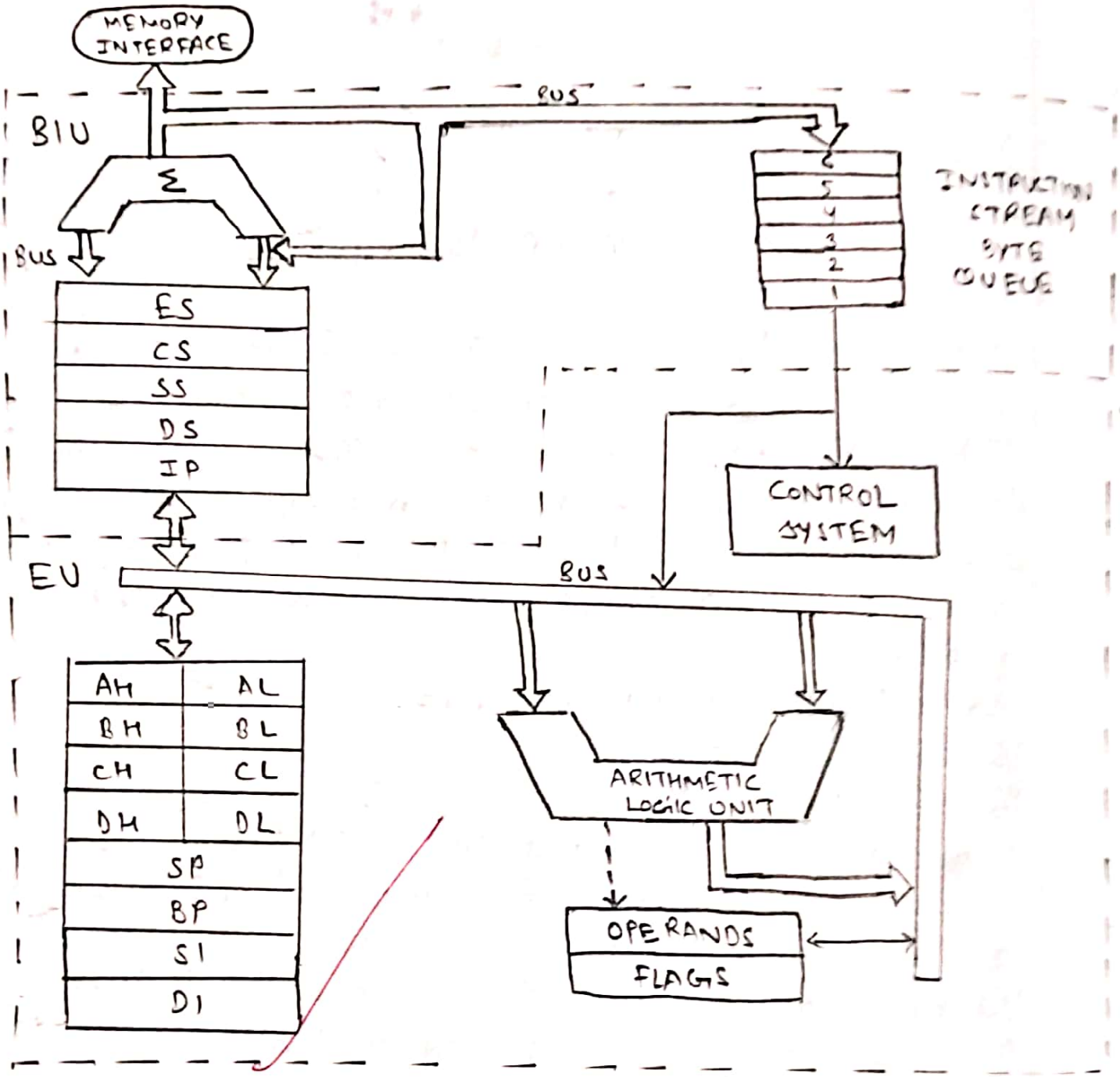
Aim :- Introduction to 8086 µP.

Apparatus :- 8086 µP kit.

Theory :- In the family of 16 bit microprocessor, Intel 8086 was the first one, launched in 1978. It supports a 16 bit ALU, a set of 16 bit registers and provides segment memory addressing capability, a rich instruction set, powerful interrupt structure and a six byte instruction queue.

- Main Features of 8086 :-

(1) 16 bit microprocessor
(2) 16 bit ALU
(3) Maximum clock frequency is 5MHz.
(4) Memory is divided into two banks :- (i) odd bank and (ii) Even bank.
(5) Maximum memory that can be connected is 1MB.
(6) Address range of memory is from 00000H - FFFFFH.
(7) It requires a single +5V power supply.
(8) It has 20 bit address bus.
(9) It can generate 16 bit input/output address, hence it can access $2^{16} = 65536$ I/O ports.
(10) The Intel 8086 is designed to operate in two modes, namely the minimum mode and maximum mode.



Internal block diagram of 8085/8088

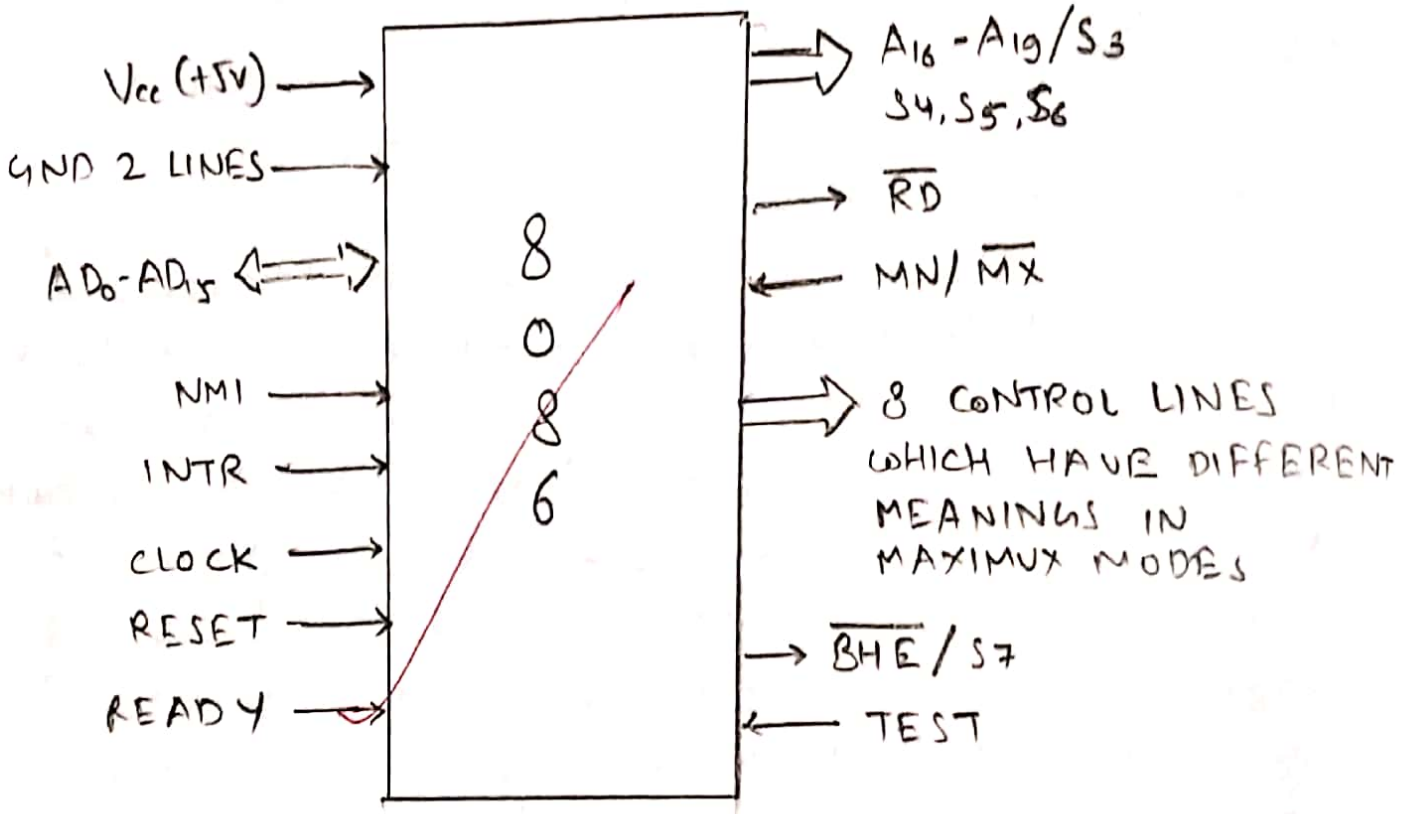
11. 8086 supports multiprogramming.
12. The main feature of 8086 is that it fetches upto six instruction bytes (four instruction bytes for 8088) from memory and queues them in order to speed up instruction execution.

- **Introduction to kit :-**

ET- 8086 LCD is a single board Microprocessor Training kit configured around Intel's 16 bit Microprocessor 8086. This kit has been designed to provide ease in interaction with the 16-bit processor. to enable the students to learn about its architecture and capabilities. This kit has been designed to operate in the max mode. The required Co-processor 8087 and I/O processor 8089 can be added on board 8086 CPU can also be replaced by 8088 CPU.

- **System Specifications (HARDWARE) :-**

CPU	8086, 16 bit µP operating in max. mode or 8088, 8 bit µP.
Co-processor	8087 Numeric Data Processor
I/O	8089 I/O Processor
EPROM	64 k Bytes of EPROM loaded with monitor expandable further using 27010.
RAM	32k bytes of CMOS RAM expandable to 128 k bytes using 62256.



Functional pin diagram of 8086

I/O Lines	48 I/O Lines
Serial	EIA RS 232-C through 8251
Interrupt	8 different level interrupt through 8259
Maskable	1
Non Maskable	8
TIMER/COUNTER	Three 16 bit Timer/Counters through 8253.
other interfaces	EPROM PROGRAMMER for 2764/27128/27256 Real Time clock interface Speaker Interface (Optional) Cassette Interface (Optional)
keyboard & Display	64 Keys ASCII 16 * 2 LCD Display.
BUS	All address, data and control signals are available at edge connector as per Multi Bus.
Power Supply	5V, 2.0 Amps for kits and serial operations
Temperature	0 to 50° C.

- **Battery Backup :-**

The kit provides a battery backup for the on board RAM area. The battery backed up RAM has an address from 10000 H to 2FFFF H. The program/data stored in this area will remain stored even if the power is switched off.

• List of Commands :-

Sl. No	Key Pressed	Command Name	Command Description	Sub Command Available
1.	S	Sub-MIR	Substitute - Memory - I/O - Register	- Read/write into/ from Memory - Read/write into/ from Port Address - Read/write into/ from Register
2.	M	Move	Move - Block - Constant	- Move block of memory to another Destination address. - Fill a constant data Byte in a Memory Block.
3.	C	Compare	Compare - Block - Constant - Master	- Compare two block of memory for being equal - Compare the contents of a memory block with a Constant. - Compare the Contents of the Master Socket.
4.	T	Mem_Tst	Memory Test	- Test a block of RAM memory for being ok.

5.	E	Ex-Mon	Expand Moniter	- Expand the content of Moniter Command.
6.	G	Go To	Execute in - Brust - Sing - STP - Break-Pt	- Execute in Full Speed. - Execute in Single-Step. - execute with break point.
7.	B	Blank	Blank check	- Blank check an EPROM in the ZIF socket.
8.	T	List	List	- List the content of EPROM in the ZIF socket.
9.	P	Program	Program	- Program the EPROM in the ZIF socket.
10	U	ser_out	serial out	- Up Loads a Program/ data to PC/XT/AT in Hex or Binary format.
11.	I	Ser_In	serial Input	- Down Loads a program/ data in to the RAM Area from the PC/XT/AT.

Sign
02/10/2019

14/15

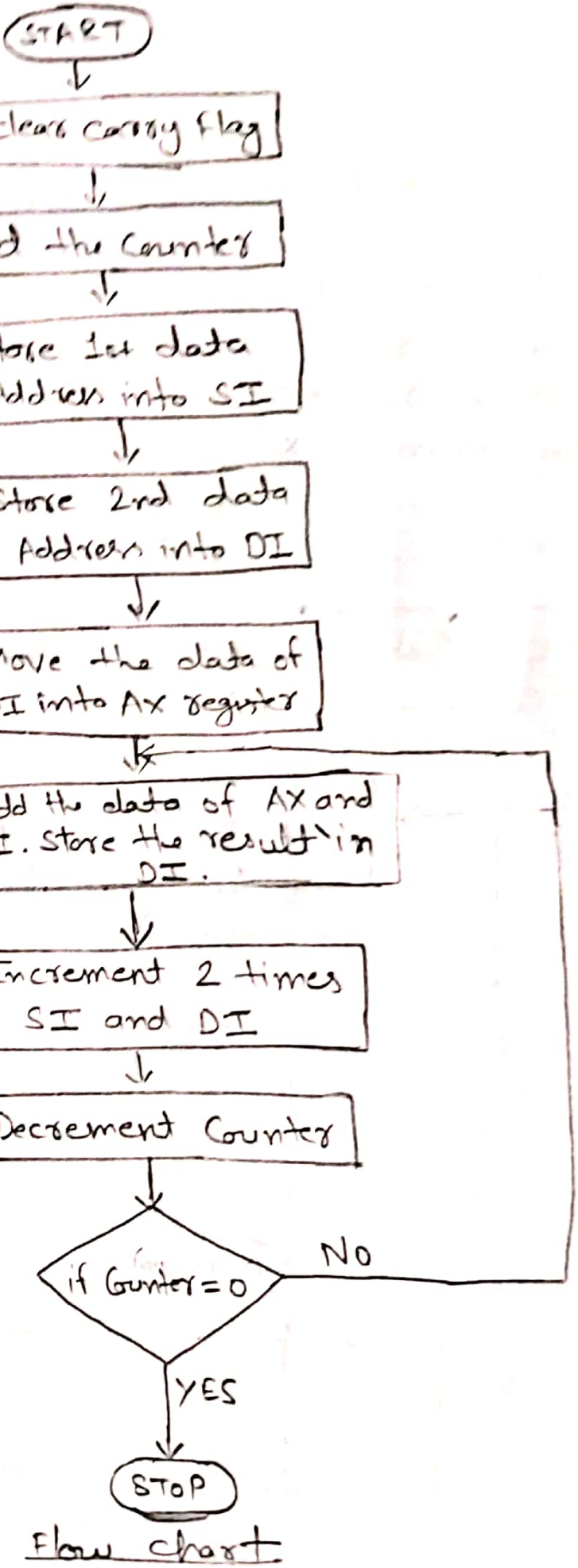
DELTA Pg No. 20
Date 30/09/19

Experiment No :- 6

Aim :- Write a program to add two 8 byte numbers stored from 0000:1300 to 0000:1307 and 0000:1308 to 0000:130F. Result is stored from location 0000:1308.

Program :-

Memory Location	Label	Mnemonics	Comments
1000:1000		CLC	clear carry flag.
1000:1001		MOV CX, 0004	Move 4 to CX.
1000:1004		MOV SI, 1300	Move 1300 to SI.
1000:1007		MOV DI, 1308	Move 1308 to DI.
1000:100A		MOV AX, [SI]	Move the data of SI in AX
1000:100C		ADC [DI], AX	Add AX with DI data.
1000:100E		INC SI	Increment the SI addr.
1000:100F		INC SI	Increment SI address.
1000:1010		INC DI	Increment DI address.
1000:1011		INC DI	Increment DI addres
1000:1012		DEC CX	Decrement CX regist
1000:1013	100C	JNZ 100C	Jump if No zero.
1000:1015		INT A5	Interrup program execution call.



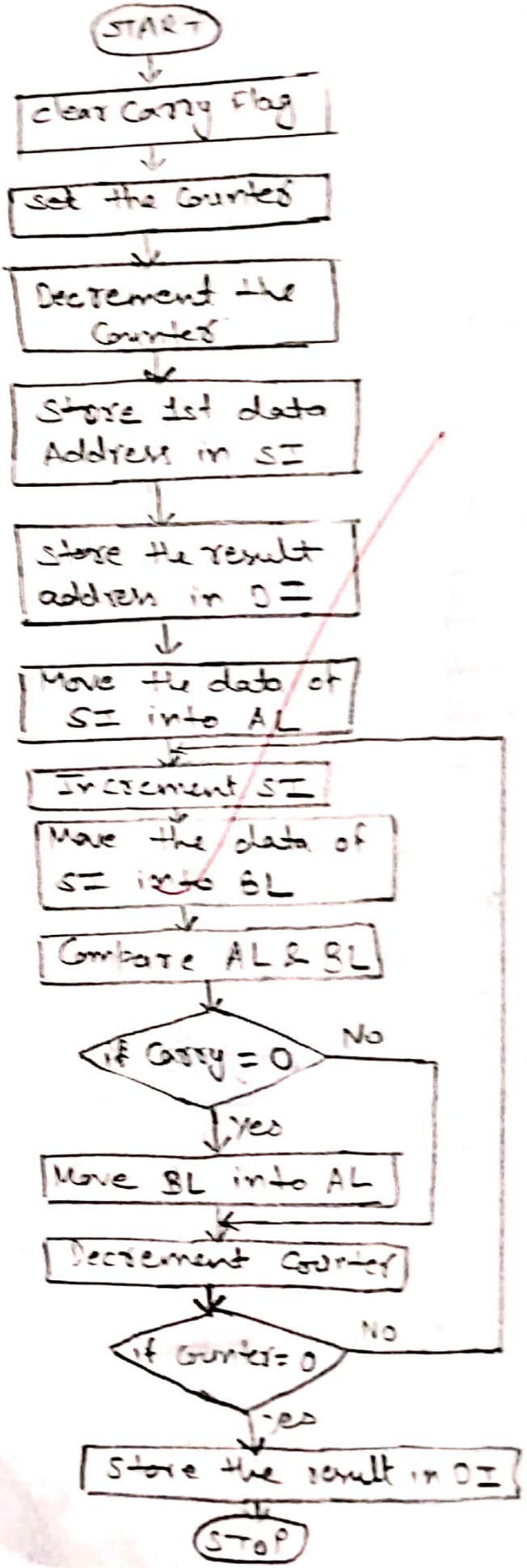
Flow chart

Result :-

Memory Location	Before Execution	After Execution
0000:1300	22	22
0000:1301	22	22
0000:1302	22	22
0000:1303	22	22
0000:1304	22	22
0000:1305	22	22
0000:1306	22	22
0000:1307	22	22
0000:1308	44	6C
0000:1309	44	6C
0000:130A	44	66
0000:130B	44	66
0000:130C	44	66
0000:130D	44	66
0000:130E	44	66
0000:130F	44	66

Sign
07/10/2019

14/15



Page No. 22
Date 07 10 19

Experiment No :- 7

Aim :- Write a program to find largest number in 8086.

Apparatus :- 8086 µP kit.

Program :-

Memory Location	Label	Mnemonics	Comments
1000 : 1000		CLC	clear carry flag.
1000 : 1001		MOV CX, 0005	Move 0005 to CX.
1000 : 1004		DEC CX	Decrement CX register.
1000 : 1005		MOV SI, 1300	Move 1300 to SI.
1000 : 1008		MOV DI, 1305	Move 1305 to DI.
1000 : 100B		MOV AL, [SI]	Move the data of SI in AL.
1000 : 100D		INC SI	Increment SI address.
1000 : 100E		MOV BL, [SI]	Move the data of SI in BL.
1000 : 1010		CMP AL, BL	Compare AL & BL register.
1000 : 1012	1016	JNC 1016	Jump if No Carry.
1000 : 1014		MOV AL, BL	Move the BL to AL content.
1000 : 1016		DEC CX	Decrement CX register.
1000 : 1017	100D	JNZ 100D	Jump if No zero.
1000 : 1019		MOV [DI], AL	Move the AL at DI address.
1000 : 101B		INT A5	Interrupt program execution call.

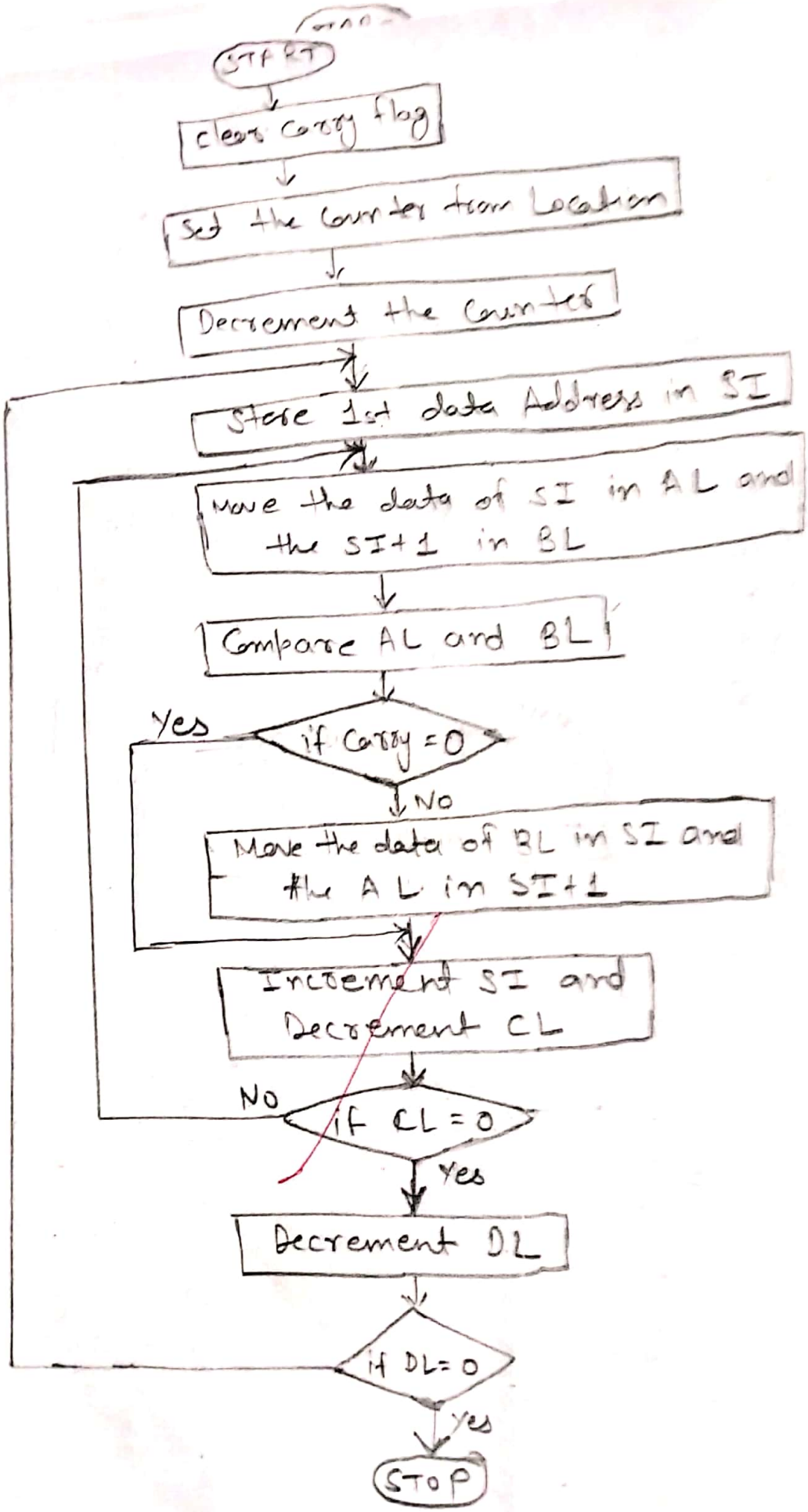
Page No. 23
Date

Result :-

Memory Location	Before Execution	After Execution
0000 : 1300	15	15
0000 : 1301	28	28
0000 : 1302	23	23
0000 : 1303	18	18
0000 : 1304	59	59
0000 : 1305	00	59

Sign
31/10/2019

15
15



Flow chart

Page No. 24
Date 14 10 19

Experiment No :- 8

Aim :- To sort a string of no. of bytes in desending order.

Apparatus :- 8086 µP kit

Program :-

Memory Location	Label	Mnemonics	Comments
1000:1000		CLC	clear carry flag.
1000:1001		MOV SI, 1200	Move 1200 to SI.
1000:1004		MOV DL, [SI]	Move the data of SI in DL.
1000:1006		DEC DL	Decrement DL.
1000:1008		MOV CL, DL	Move DL data into CL.
1000:100A		MOV SI, 1300	Move 1300 to SI.
1000:100D		MOV AL, [SI]	Move the data of SI in AL.
1000:100F		MOV BL, [SI+1]	Move the data of SI+1 in BL
1000:1012		CMP AL, BL	Compare AL and BL.
1000:1014	101B	JNC 101B	Jump if No carry.
1000:1016		MOV [SI], BL	Move the data of BL in SI.
1000:1018		MOV [SI+1], AL	Move the data of AL in SI+1
1000:101B		INC SI	Increment SI.
1000:101C		DEC CL	Decrement CL.
1000:101E	101D	JNZ 101D	Jump if No zero.
1000:1020		DEC DL	Decrement DL.

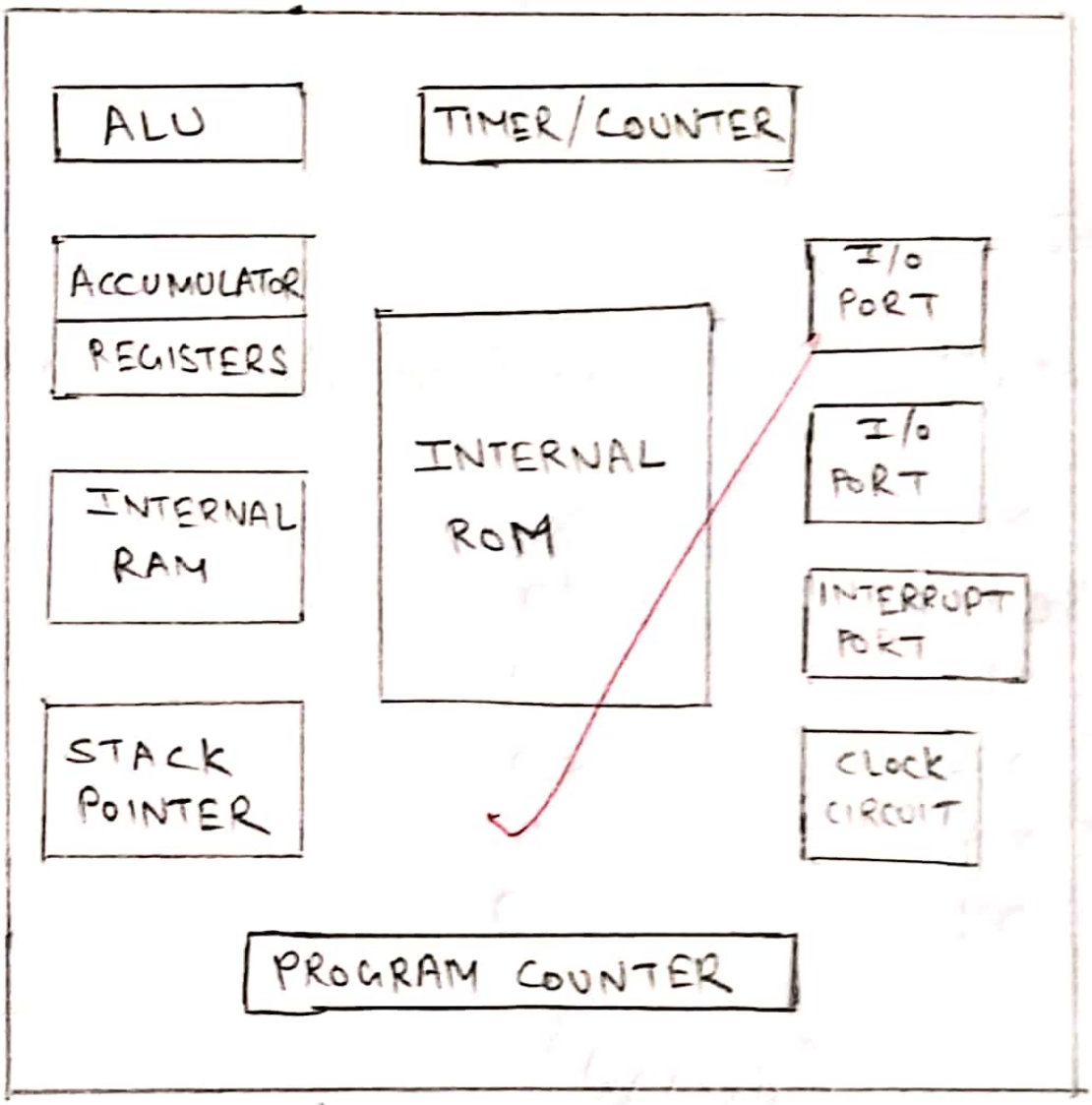
1000:1022 1000:1024	1008	JNZ 1008 INT A5	Jump if No zero. Interrupt program Execution call.

Result :-

Memory Location	Before Execution	After Execution
0000:1200	05	05
0000:1300	40	50
0000:1301	50	40
0000:1302	30	30
0000:1303	10	20
0000:1304	20	10

Sap
21/09/2019

14/15



Block diagram of MicroController

Experiment No :- 9

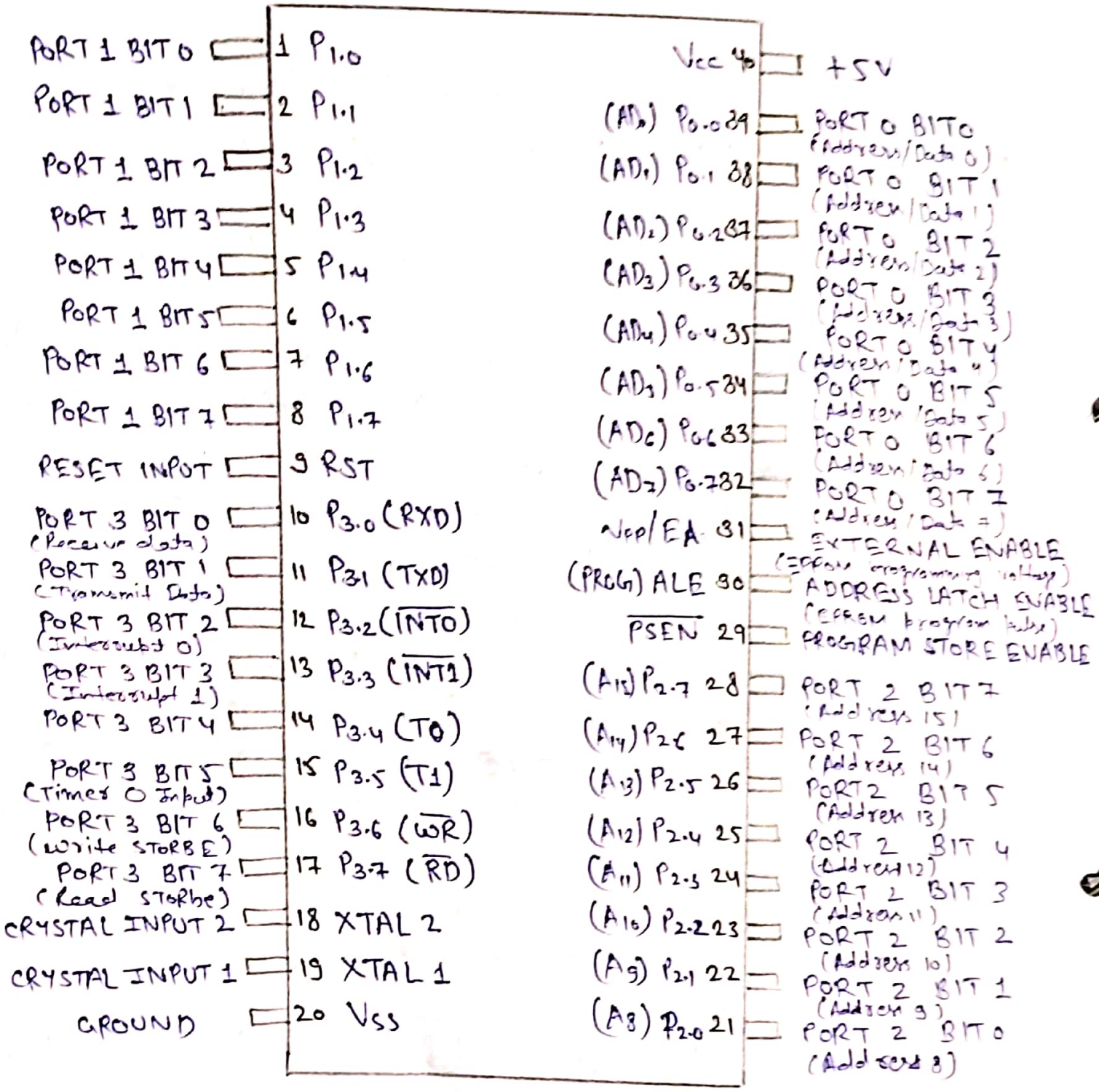
Aim :- Introduction to 8051 Microcontroller and KEIL Programming.

Theory :-

The 8051 is an 8-bit microcontroller originally developed by Intel in 1980. Its architecture is Harvard-Based with external memory read/write capabilities built in as part of the architecture.
The 8051 microcontroller generic part number actually includes a whole family of microcontrollers that have numbers ranging from 8031 to 8051 and are available in NMOS and CMOS construction in a variety of package types.

Features of 8051 microcontroller :-

1. 8 bit CPU with register A (accumulator) and B.
2. 16 bit program Counter and Data pointer (DPTR).
3. 8 bit PSW.
4. 8 bit stack pointer.
5. Internal ROM or EPROM (8751) of 0 (8031) to 4K (8051).
6. Internal RAM of 128 bytes.



8051 pin diagram

32 input/output pins arranged as four 8 bit ports.
Two 16 bit counters/timers.
Fully duplex serial data receiver/transmitter.
Control register.
Two external and Three internal interrupt sources.
Oscillators and clock circuits.

AT89C51 Microcontroller :-

AT89C51 is an 8 bit microcontroller and belongs to Atmel's 8051 family.

Features :-

- Compatible with MCS-51™ products.
- 4K Bytes of In-System Reprogrammable Flash memory.
- Endurance : 1,000 write/Erase Cycle.
- Fully static operation : 0Hz to 24 MHz.
- Three Level program Memory Lock.
- 128 x 8 bit Internal RAM.
- 32 programmable I/O Lines.
- Two 16-bit Timer/Counters.
- Six Interrupt Sources.
- Programmable Serial channel.
- Low-power Idle and power-down Modes.

Description :-

The AT89C51 is low-power, high performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). This device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry standard MCS 51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer.

By combining a versatile 8-bit CPU with Flash 4 on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost-effective solution to many embedded control applications. The AT89C51 provides the following standard features : 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry.

In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes.

Page No. 05
Date

Writing Assembly Level program using KEIL software.

Step 1 :- WAP to add 22H and 33H.

```
Org 0
Start : mov a, #22h
        mov b, #33h
        add a, b
        mov p1, a
```

Step 2 :- Save the file and create hex file.

Now our executable file (Hex file) is ready, we have to load or burn this on to flash memory of the Micro controller 8051 and then we can run these.

Result :- Successfully studied about the 8051 microcontroller and KEIL programming.

4/9/2019
2/10/2019

14/15