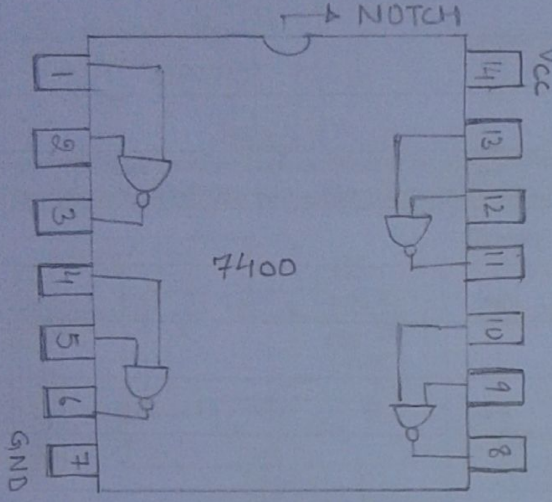
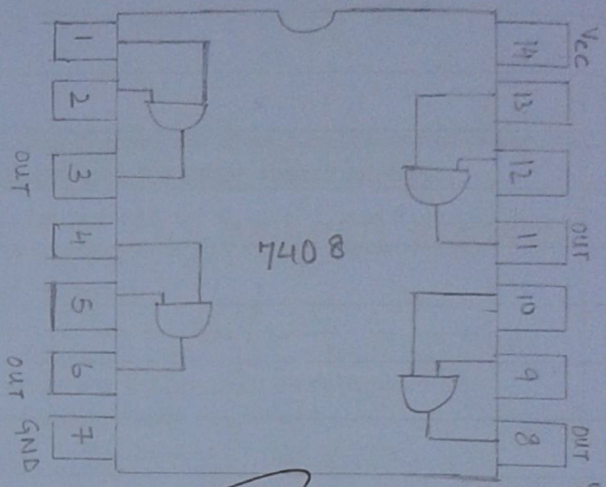
Exp: 1

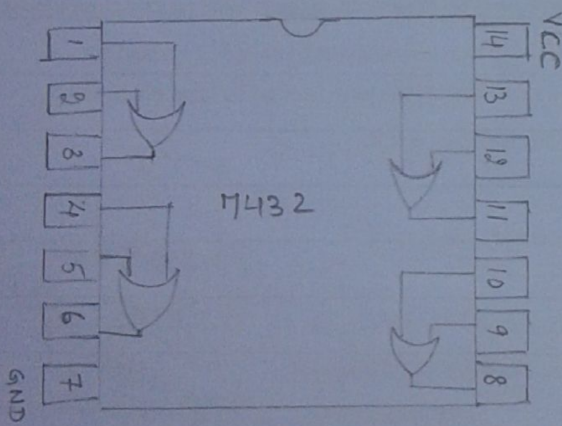
Aim: To study the logic gates and verify their truth tables



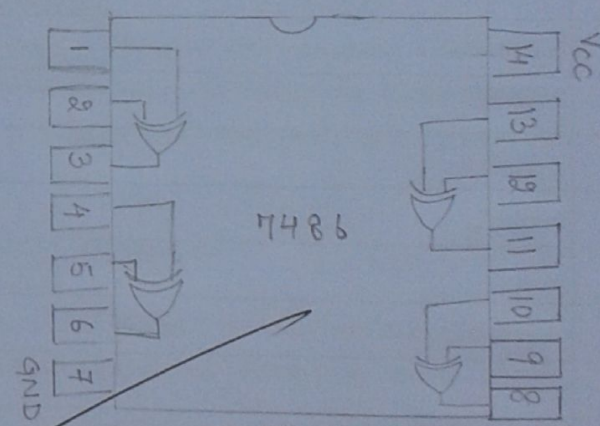
NAND GATE (IC) [7400]



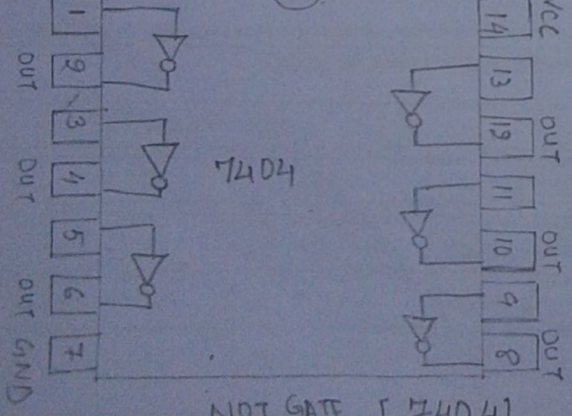
AND GATE (IC) [7408]



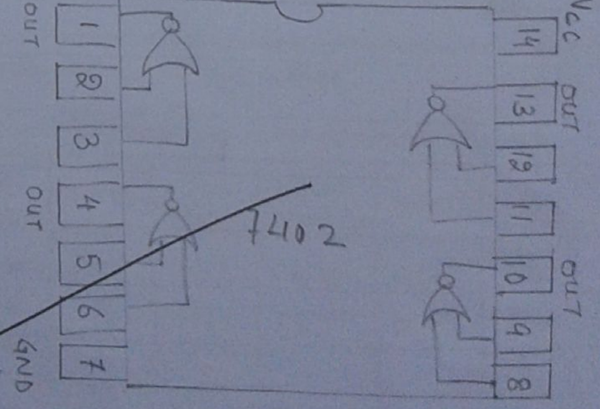
OR GATE [7432]



EX-OR GATE [7486]



NOT GATE [7404]



NOR GATE [7402]

EXPERIMENT NO: 1

AIM:

To study the logic gates and verify their truth tables.

APPARATUS REQUIRED:

Digital Board - 01
DC power supply +5V from external source or Digital Lab ST-2611
Digital Multi meter or Digital Lab ST-2611 , LED , IC's.

THEORY:

Logic gates ~~are electronic~~ circuits which perform logical functions on one or more inputs to produce one output. There are several logic gates (7 in number).

When all the input connections of a logic gate are written in series and their corresponding outputs written along them, then this Input-Output combination is called a TRUTH TABLE.

• DIFFERENT TYPES OF GATES:

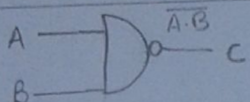
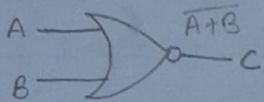
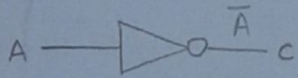
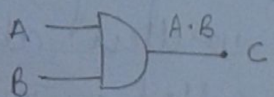
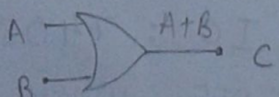
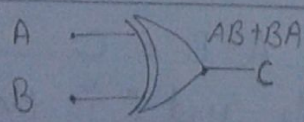
* AND GATE : IC : 7408

A gate is said to be an AND GATE, when the OUTPUT is high only when both the ~~inputs~~ are high, i.e when any 1 is input is low, the ~~output~~ is low.

Follows the operation : $A \cdot B = C$

where, A and B are inputs and C is the output.

OBSERVATIONS:

SERIAL NO:	NAME	SYMBOL	INPUT A	INPUT B	OUTPUT C
1.	NAND IC 7400		0	0	1
			0	1	1
			1	0	1
			1	1	0
2.	NOR IC 7402		0	0	1
			0	1	0
			1	0	0
			1	1	0
3.	NOT IC 7404		0		1
			1		0
4.	AND IC 7408		0	0	0
			0	1	0
			1	0	0
			1	1	1
5.	OR IC 7432		0	0	0
			0	1	1
			1	0	1
			1	1	1
6.	EX-OR IC 7486		0	0	0
			0	1	1
			1	0	1
			1	1	0

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* NAND GATE: IC : 7400

It is the reverse of the Normal AND, i.e inverted result is obtained in NAND, which means if any 1 or both the inputs are low the resulting value is high. It is a AND combined with NOT. i.e NOT+AND.

* OR GATE: IC : 7432

A gate is said to be an OR GATE when either 1 or both the signals are high (i.e 1) then the output is 1 (high), otherwise low (0).

* NOR GATE: IC : 7402

NOR gate is the inversion of OR, an OR in series with a NOT, forming a NOT-OR, combination. Here in, if your both the inputs are low only then the output is high, otherwise low.

* EX-OR GATE: IC: 7486.

An Exclusively OR GATE is known as X-OR GATE
Here in both the inputs ~~are~~ should not be same, if at all this happens, the output is low, otherwise high.

* NOT GATE: IC : 7404

NOT is the most simple GATE, i.e it is a single input Gate & is responsible of inverting the input, i.e
if the input is A, and output is C, then $C = \overline{A}$

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Expt. No. 1

Page No. 3

PROCEDURE:

1) Connect the trainer kit to AC- POWER SUPPLY.
2) Connect inputs of 1 logic gate in IC resting on the breadboard to logic sources.
3) Connect output of logic gate to logic indicator.
4) Insert, different IC's and observe the functioning of different gates for different combinations.
5) Draw, the truth table of different logic gates.
6) Switch off the AC-POWER-SUPPLY, after your experiment is complete.

RESULT:

* Truth tables of all logic gates and universal gates are verified, successfully.

PRECAUTIONS:

* Connections should be carefully and tightly made.
* First, prepare the circuit and then ON, the AC-SUPPLY.
* LED should be working.
* Apply connections according to IC numbers.

10 good

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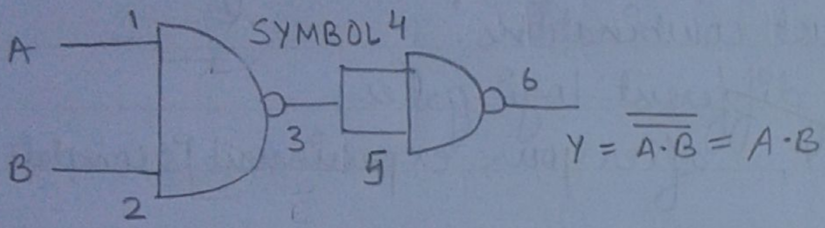
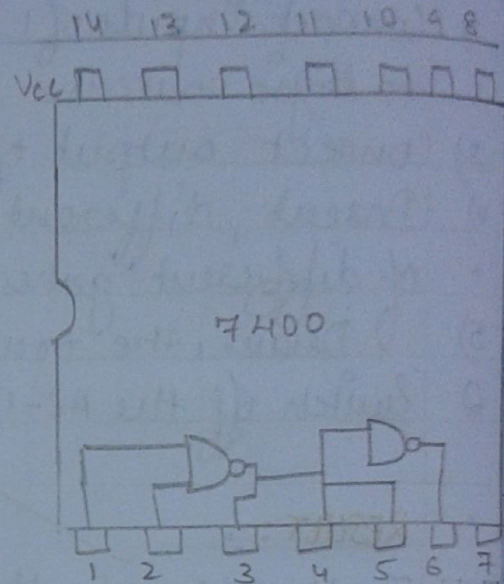
EXPERIMENT NO:2

AIM: To verify truth table of all logic gates using universal gates (NAND, NOR).

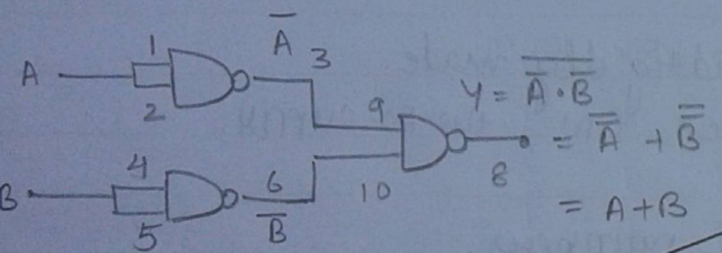
USING NAND GATE:

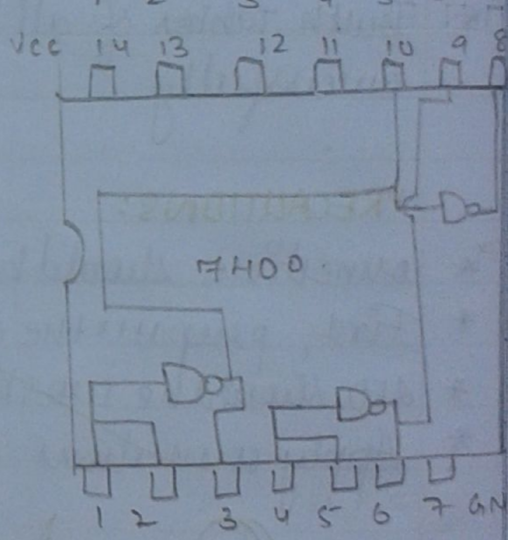
AND GATE:



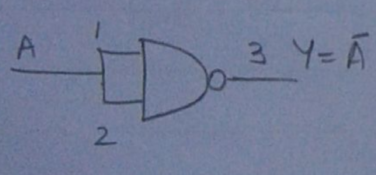


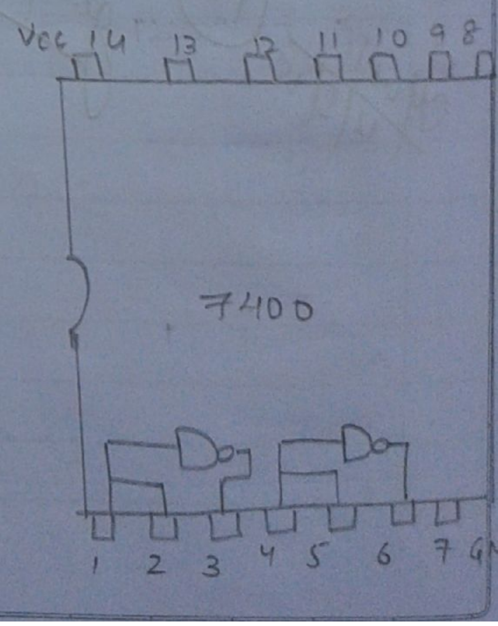
OR GATE:





NOT GATE:





EXPERIMENT NO: 2

AIM:
To verify truth table of all logic (basic) gates (NOT, AND, OR) using universal gates (NAND, NOR).

APPARATUS:
Bread board, connecting wires, IC-7400, 7402, and power supply, LED.

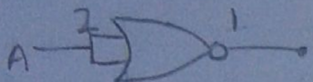
THEORY:
Logic gates are electronic circuits which perform logical functions one or more inputs to produce 1 output. There are 7 logic gates. When all input connections of logic gates are written in series, and their corresponding outputs written along them, their input/output combination form a truth table

Now, Universal gates are ones using which we can get the output for every other gate. NAND and NOR are considered to the universal gates

NAND GATE:
NAND gate is basically formed from the combination of NOT and AND gate in series. It gives output when 1 or both inputs are 0, the output is high for NAND gate. IC NO: 7400.

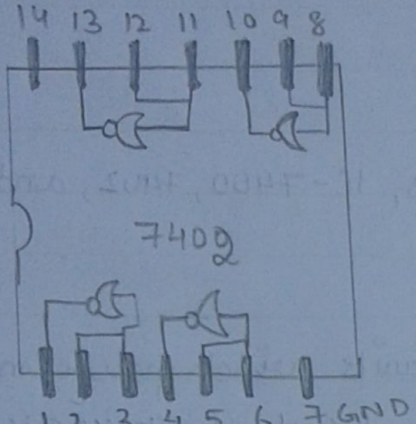
~~NOR GATE:~~ IC: 7402
NOR GATE is basically, NOT and OR gates in series; output of an OR gate taken as an input to NOT gate forms a NOT-OR gate or a NOR gate where output is 1 only when both inputs are 0.

USING NOR GATE:



$Y = \overline{A+A} = \overline{A}$

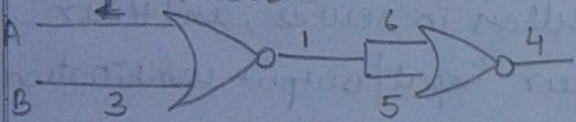
NOT GATE



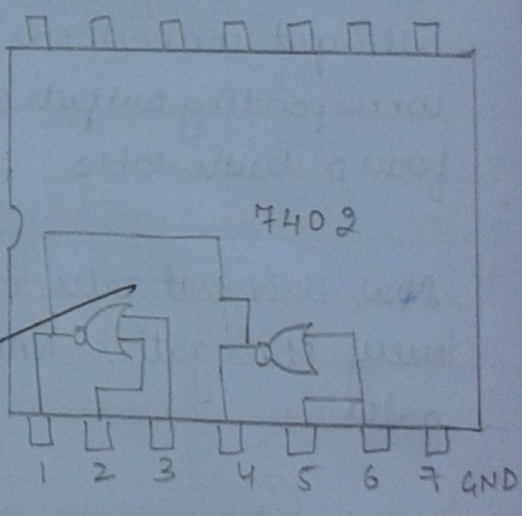
INPUT	OUTPUT
0	1
1	0

OR GATE:

SYMBOL

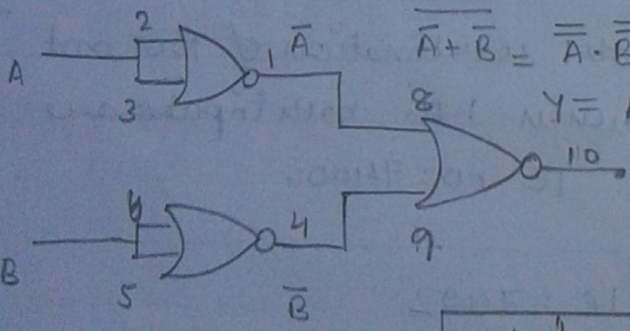


$Y = \overline{\overline{A+B}}$
$= A+B$



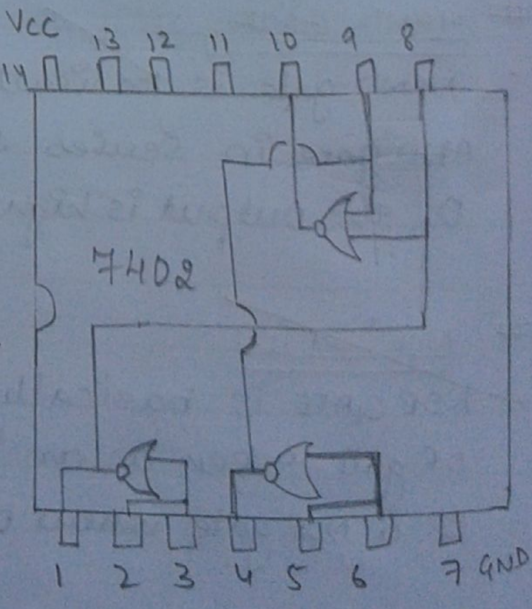
IN(A)	IN(B)	OUT
0	0	0
0	1	1
1	0	1
1	1	1

AND GATE



$\overline{\overline{A}+\overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}}$

$Y = A \cdot B$



IN(A)	IN(B)	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Date 12/08/15

Expt. No. 2 Page No. 5

PROCEDURE:

1. Connect the trainer kit to AC power supply.
2. Using IC-7400 (NAND) and IC-7402 (NOR) make all the logic designs of AND, OR, NOT through different combinations.
3. Draw, the truth table for different logic gates.
4. Verify that truth table with the actual truth table of AND, OR, & NOT
5. Switch off the power supply after the experiment.

RESULT:

* The truth table of all the logic gates matched with the truth table drawn using universal gates. Hence, the experiment was successfully performed.

PRECAUTIONS:

1. All connection should be tight, and neat.
2. LED should be in working condition
3. First, ~~pous~~ prepare the entire circuit on the kit and then switch on the supply.
4. ~~Switch off the power supply as and when you finish your experim-ent.~~

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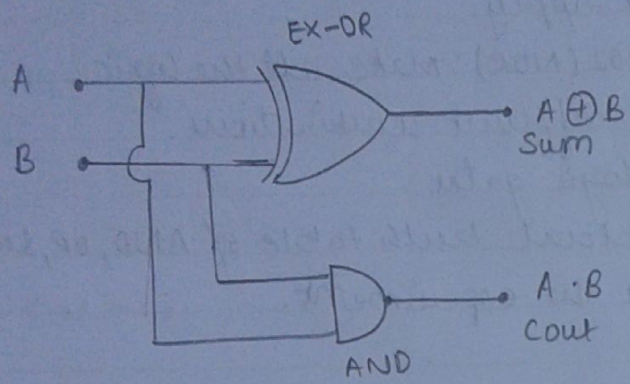
Teacher's Signature :

EXPERIMENT NO: 3

AIM: to realise and verify the truth tables of half and full adders.



CIRCUIT DIAGRAM

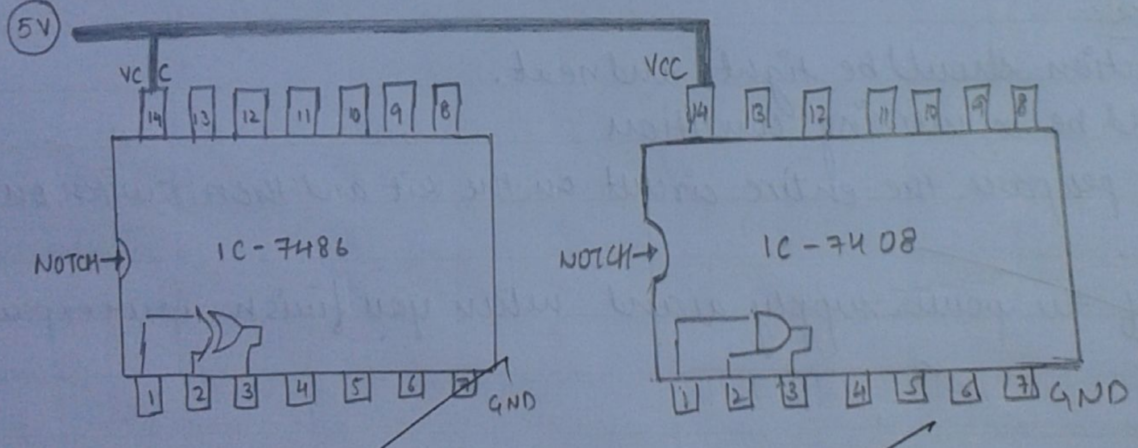
INPUT		OUTPUT	
A	B	Sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

TRUTH TABLE

SUM = $A \oplus B$

Cout = $A \cdot B$

IC DIAGRAM FOR HALF ADDER



EXPERIMENT NO: 3

AIM:

To realise and verify truth table of half adder and full adder.

APPARATUS:

Breadboard, connecting wires, IC's, LED, power supply kit.

THEORY:

Logic gates are electronic circuits which perform logical functions one or more inputs to produce one output. There are seven logic gates when all inputs of gates are written in series, corresponding outputs along them, called a TRUTH TABLE

HALF ADDER:

A half adder is logical circuit that performs an addition operation on 2-binary digits. A half adder produces a sum and a carry value which are both binary digits

Boolean expression: $\boxed{\begin{aligned} Sum &= A \oplus B \\ Carry &= A \cdot B \end{aligned}}$

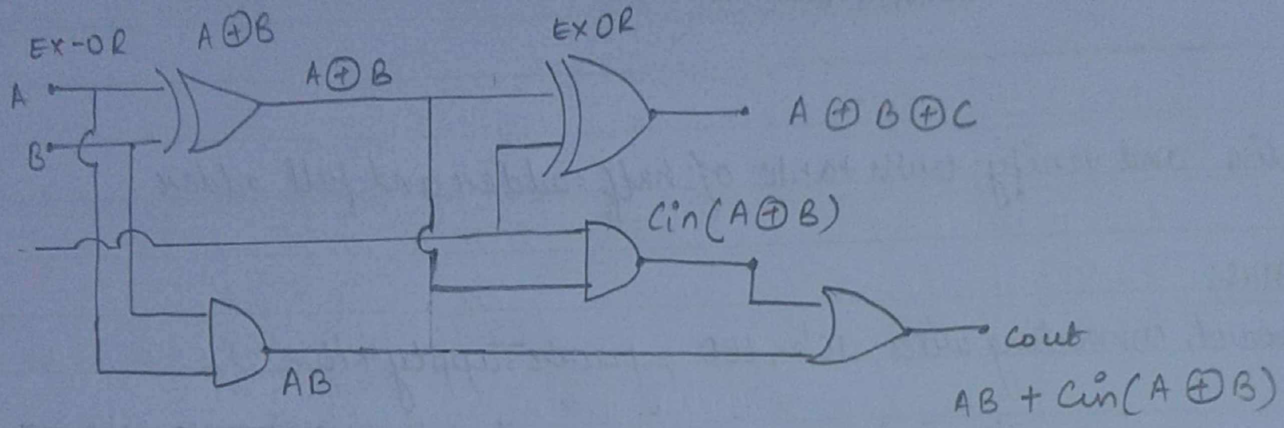
FULL ADDER:

It is a logical circuit that performs addition operation on 3 binary digits. A full adder produces sum and carry value which are both binary digits

Boolean expression:

$$\boxed{\begin{aligned} Sum &= A \oplus B \oplus C \\ Carry &= \cancel{AB + BC + CA} \end{aligned}} \quad AB + C_{in}(A \oplus B)$$

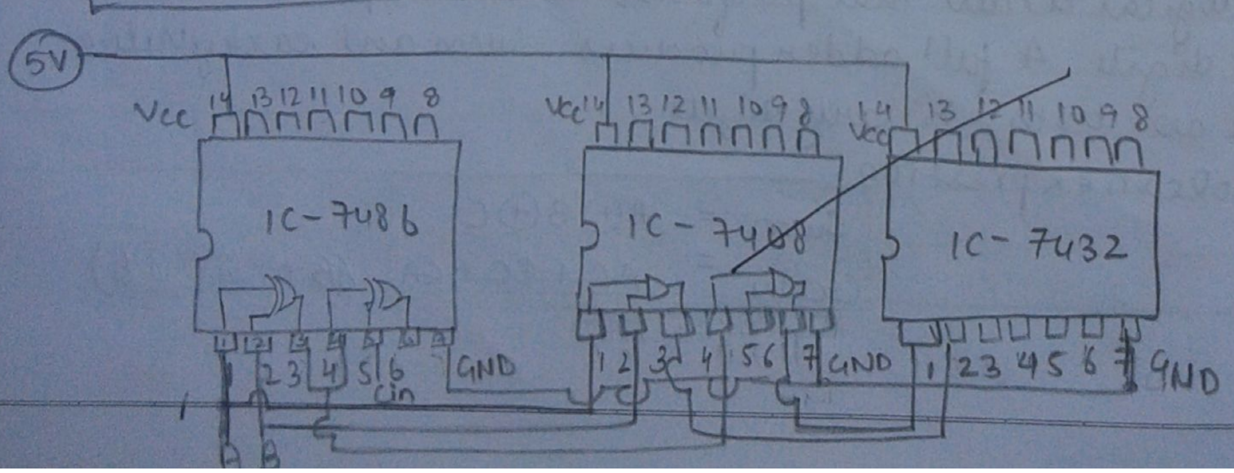
FULL ADDER CIRCUIT DIAGRAM



TRUTH TABLE FOR FULL ADDER

INPUT A	B	Cin	OUTPUT (S)	OUTPUT (Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IC DIAGRAM FOR FULL ADDER



Date 19/08/15

Expt. No. 3

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PROCEDURE:

1. Connect Kit to power supply.
2. Use IC-7486, IC-7408, IC-7404, IC→7432 to make full adder and half adder
3. Draw the truth table with original one.
4. Switch off power supply.

RESULT:

* The truth table for full adder and half adder is verified

PRECAUTIONS:

1. All the connection should be tight.
2. LED should be working.
3. Apply connections, according to AC Number.

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Teacher's Signature :

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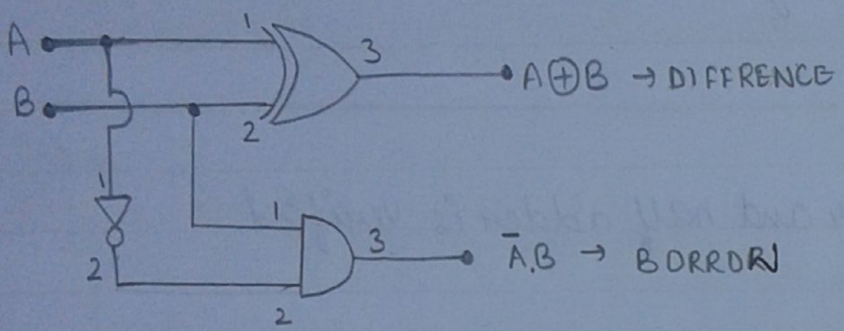
EXPERIMENT NO:4

HALF AND FULL SUBTRACTOR:

AIM: To realise and verify the truth table of the half and full subtractor

LOGICAL CIRCUIT DIAGRAM

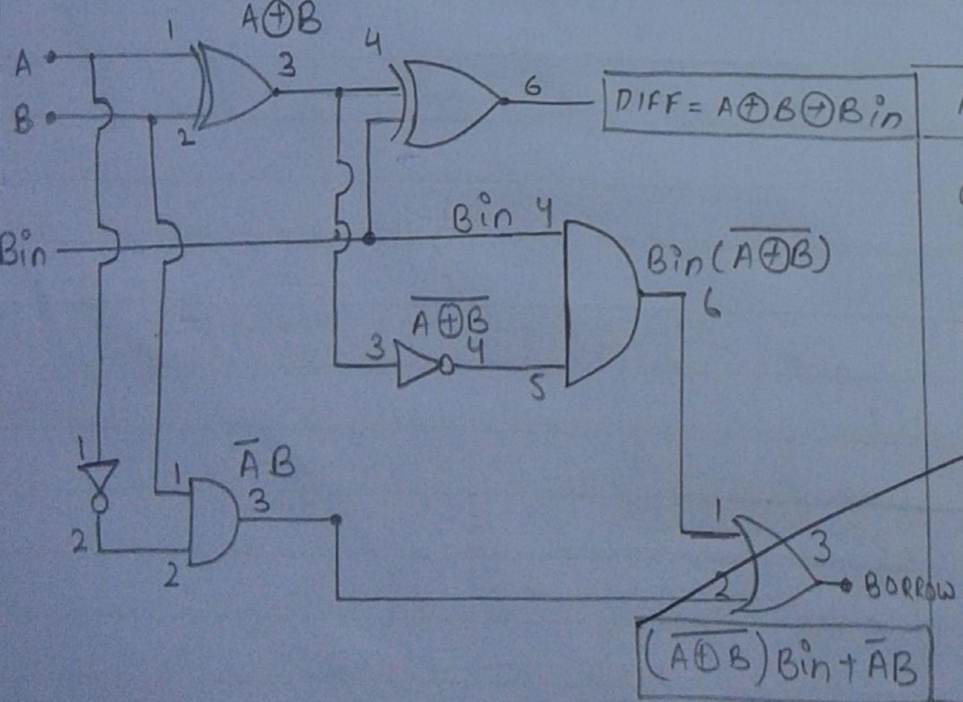


TRUTH TABLE

A	B	DIFF	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

** ABOVE DRAWN IS THE LOGICAL CIRCUIT DIAGRAM AND TRUTH TABLE OF HALF-SUBTRACTOR USING EX-OR and AND and NOT IC's.

LOGICAL CIRCUIT DIAGRAM



TRUTH TABLE

A	B	Bin	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Date 09/09/15

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EXPERIMENT NO: 4
HALF AND FULL SUBTRACTOR

AIM:

To realise and verify the truth table of the half and full subtractor

APPARATUS:

Breadboard, connecting wires, IC's, LED, power supply-kit

THEORY:

HALF SUBTRACTOR:

A half subtractor circuit is a logical circuit that performs subtraction of 2 bits. It has 2 inputs and 2 outputs

Boolean expression: difference : $A \oplus B$
borrow : $\bar{A} \cdot B$

FULL SUBTRACTOR:

It is a logical circuit that performs subtraction operation on three binary digits. It produces difference and borrow value which are both binary digits

Boolean exp : difference → $A \oplus B \oplus B_{in}$

borrow → $\bar{A}B + (\overline{A \oplus B})B_{in}$

Teacher's Signature :

Date 09/09/15

Expt. No. 4

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PROCEDURE

1. Connect kit to the power supply
2. Use IC: 7486, 7404, 7408, 7432 to make full and half subtractor
3. Make the circuit exactly as shown in the circuit diagram
4. Draw the truth table, acc to your observations
5. Verify the truth table with original truth table
6. Switch off power supply after use.

RESULT:

* The truth table of half and full subtractor is verified

PRECAUTIONS:

* All the connections should be tight.
* LED should be working.
* Apply connection according to IC numbers.
* Verify that the notch of the IC is on the ~~~~ right side before performing.

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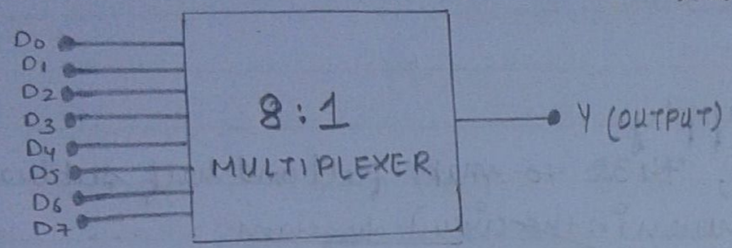
Teacher's Signature :

AIM: To implement 8:1 MUX and verify the truth table and also for 1:2 Demux

LOGICAL OPERATION OF 8:1 MUX.



TRUTH TABLE :

SELECT LINES :			OUTPUT
S_0	S_1	S_2	Y
0	0	0	D_0 $\bar{S_0}\bar{S_1}\bar{S_2}$
0	0	1	D_1 $\bar{S_0}\bar{S_1}S_2$
0	1	0	D_2 $\bar{S_0}S_1\bar{S_2}$
0	1	1	D_3 $\bar{S_0}S_1S_2$
1	0	0	D_4 $S_0\bar{S_1}\bar{S_2}$
1	0	1	D_5 $S_0\bar{S_1}S_2$
1	1	0	D_6 $S_0S_1\bar{S_2}$
1	1	1	D_7 $S_0S_1S_2$

* TRUTH TABLE OF 8X1 or 8:1 MUX

* BEHIND IS THE LOGIC CKT DIAGRAM OF 8:1 MUX

Date 16/9/15

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EXPERIMENT NO: 5

AIM:

To implement 8:1 MUX combinational circuit and verify the truth table, and 1:2 De-mux, using truth table

APPARATUS:

BreadBoard, connecting wires, LED, power supply.

THEORY:

(a) combination circuit:

Circuits made up of combination of different gates are called combinat^n circuits. There are 4 types -

* Multiplexer
* De-Multiplexer
* Encoder
* Decoder

Multiplexer (MUX):

It is combination ckt having 2^n inputs, n-select lines and 1 output. Eg → 8:1 MUX having, 8 inputs, ie 3 select lines and one output.

In 8:1 MUX, output is equal to any one of the inputs depending upon combination of select lines. To get desired output, enabler input should be active low, if enabler input is active high, MUX doesn't work.

PROCEDURE:

1. Connect wires on bread board kit according to ckt diagram.
2. Positive terminal of LED is attached to output position and

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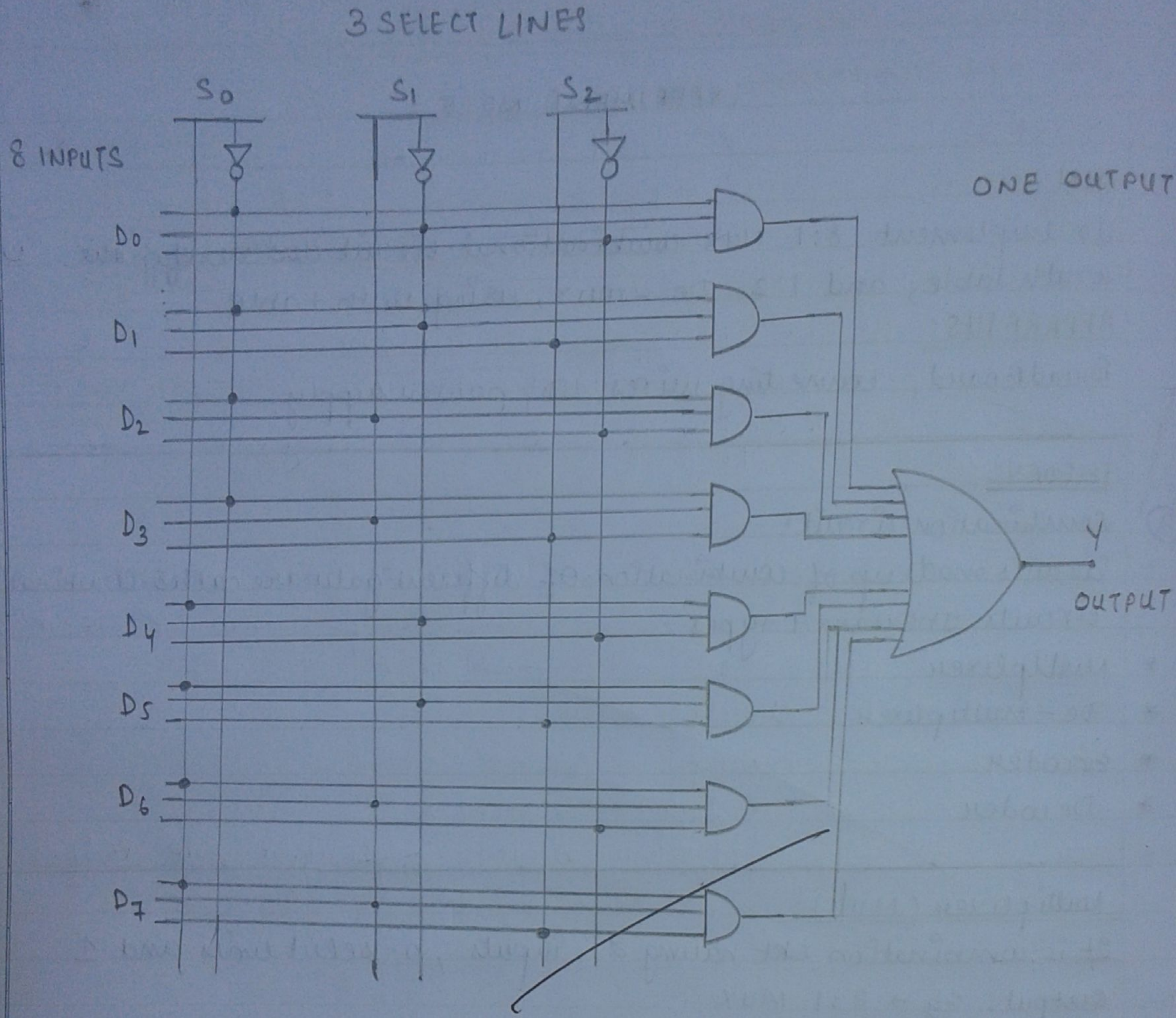
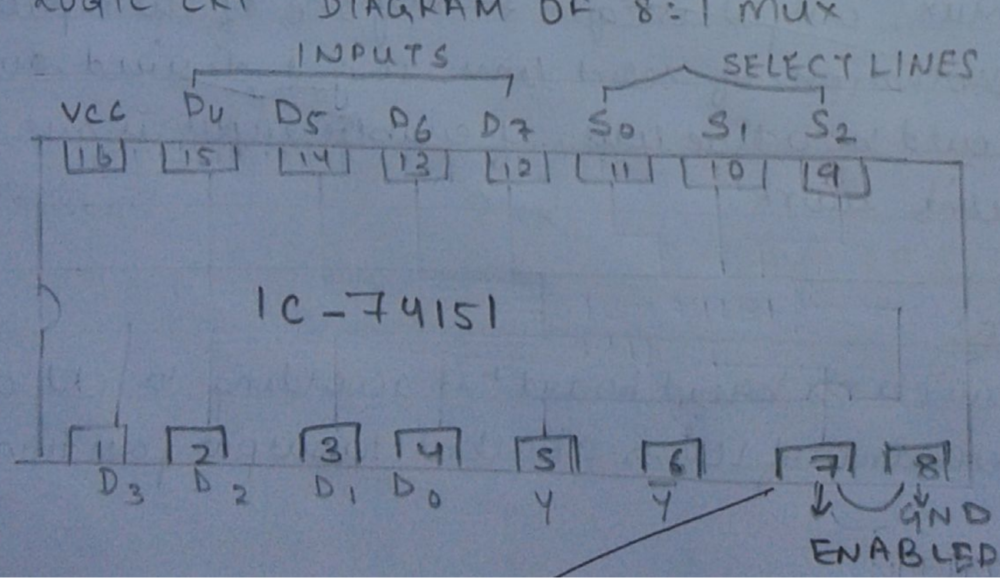


* LOGIC CKT DIAGRAM OF 8 : 1 MUX



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negative terminal is grounded.

3. Connect logic 1 to each data input of multiplexer corresponding to each combination of input variables. For remaining data, inputs connect logic 0.

4. Turn ON power supply and change input (high, low) to check function of multiplexer.

PRECAUTIONS:-

1. Connections should be done properly and tightly on breadboard kit.
2. LED should be in working conditions.
3. Assume that, all connections should be tight and wires should not be broken.

RESULT:-

Truth table of 8:1 MUX was verified.

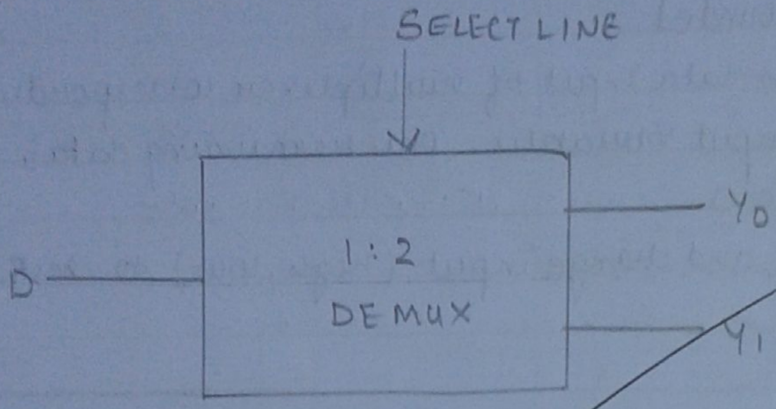
ⓑ DEMUX:

A demux performs the reverse operation of a multiplexer it takes a single input and distributes it over several outputs, so a demultiplexer can be thought of as a distributor. Since it transmits the same data to different destinations, Thus, a demultiplexer is a 1-to-N (or 2^n) device. The select data will be transmitted

PROCEDURE:

1. Connect the wires on the bread-board kit according to the circuit diagram.

GENERALISE FORM OF DE-MUX



TRUTH TABLE OF DEMUX

I/P D	S	Y_0	Y_1
1	0	1	0
1	1	0	1

2. Positive terminal of the battery of LED is attached to the output position and negative terminal is grounded.
3. Turn ON the power supply and change the input (high/low) to check the function of the gate

RESULT :

One 1:2 De-mux combinational circuit is implemented using truth table and is verified.

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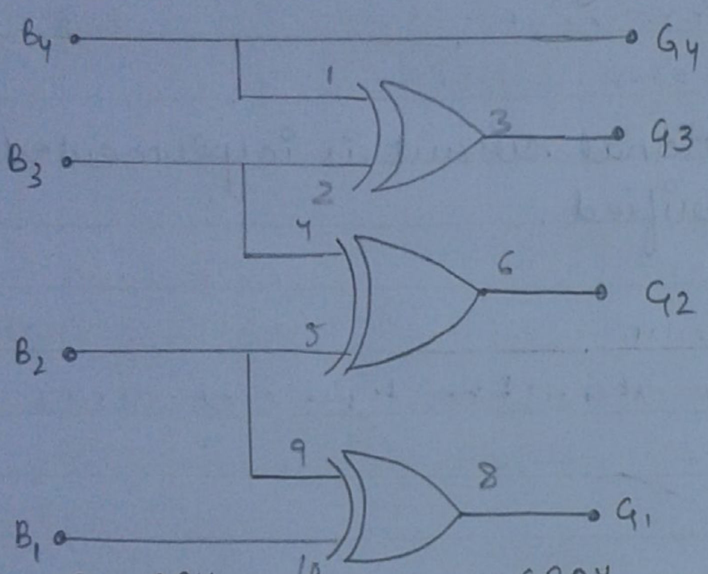
EXPERIMENT NO: 6

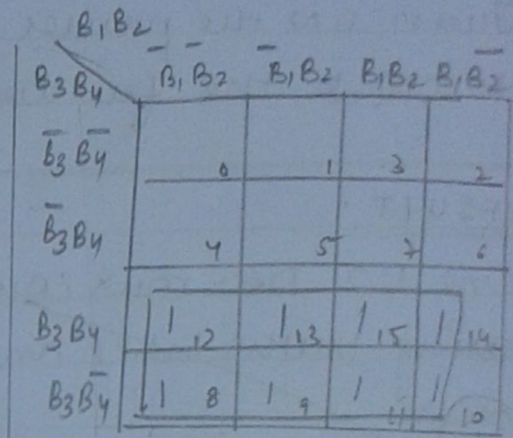
AIM:

To design Binary to Gray and Gray to Binary code convertors.

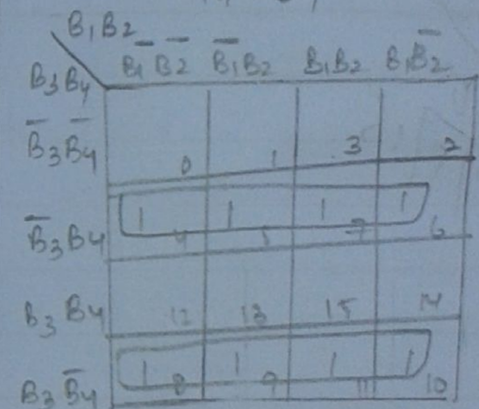
CIRCUIT DIAGRAM

BINARY TO GRAY CONVERTOR

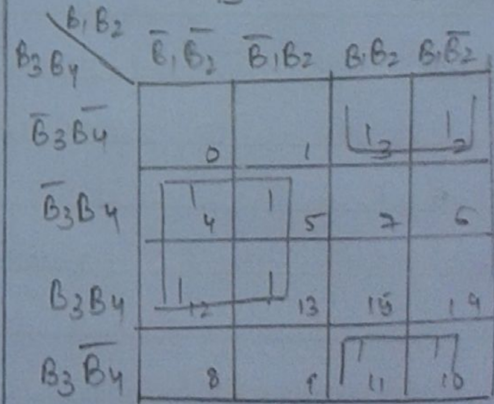




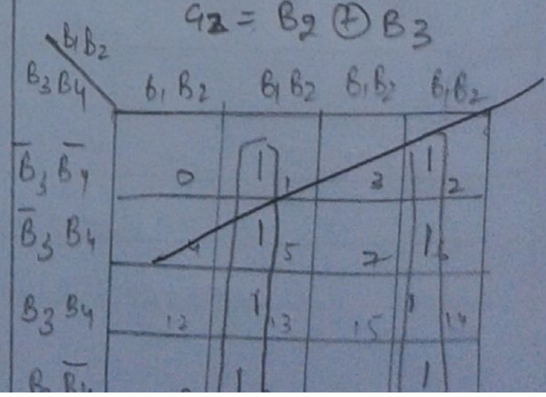
$G_4 = B_4$



$G_3 = B_4 \oplus B_3$



$G_2 = B_2 \oplus B_3$



BINARY				GRAY			
B_4	B_3	B_2		G_4	G_3	G_2	G_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1

EXPERIMENT NO: 6

AIM:

To design a 4 bit Binary to gray and Gray to Binary code converter

APPARATUS:

Breadboard, connecting wires, power supply and EX-OR gate IC. [7486]

THEORY:

BINARY TO GRAY:

The input to the binary to gray (4-bit) code converter is a 4bit binary number and the output to it is a 4bit gray code. There are 16 possible combination of these 4 bits forming 16 different binary numbers and thereby producing 16 corresponding Gray code

GRAY TO BINARY:

Here, the input to the gray to binary code converter is a gray number and the 4 bits are as such that they produce 16 possible combination, and corresponding to which a Binary code can be produced.

OPERATION TO BE FOLLOWED:

Let say, a number is 0111

then,

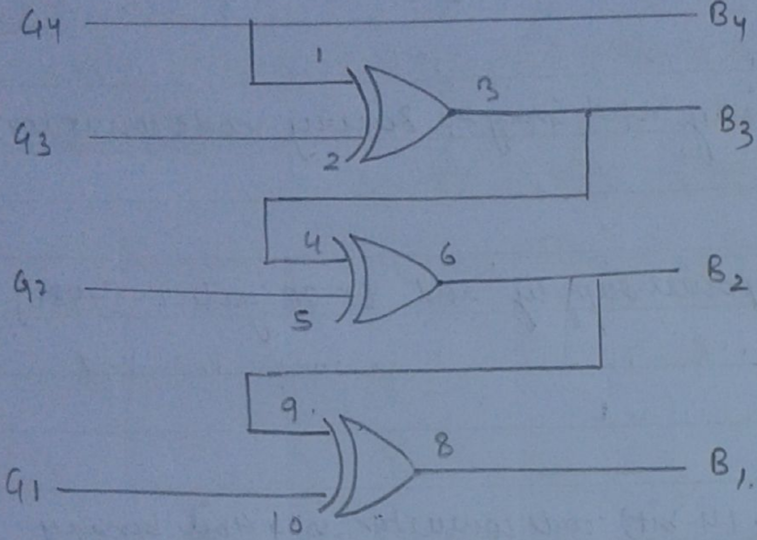
* Binary to Gray conversion follows the following concept:

0111 → 0 then ex-or between others i.e 0⊕1⊕1⊕1 → 0100

and * Gray to Binary conversion follow the following concept:

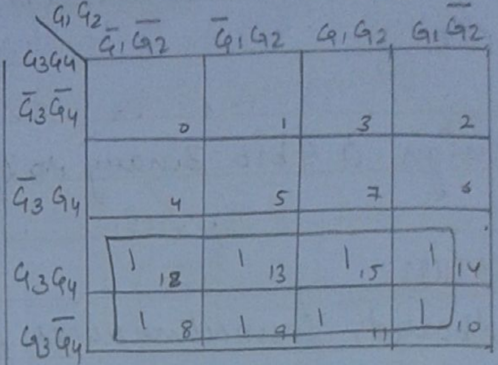
0111 → 0 then ex-or between result and next value i.e 0111 → 0101

GRAY TO BINARY CONVERTOR

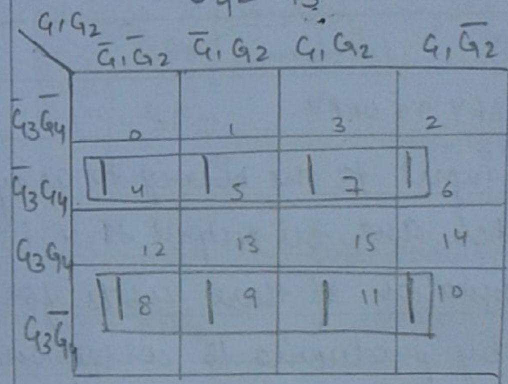


Truth Table :

4 bit Gray				4 bit Binary			
G_4	G_3	G_2	G_1	B_4	B_3	B_2	B_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

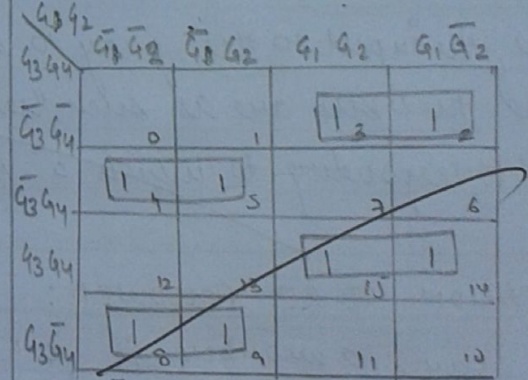


$B_4 = G_3$



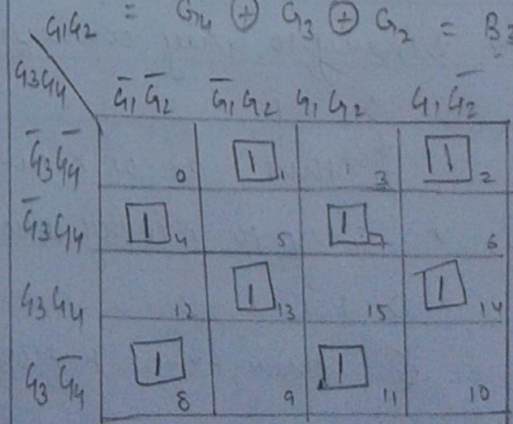
$B_3 = \overline{G_3} G_4 + G_3 \overline{G_4}$

$B_3 = G_3 \oplus G_4$



$B_2 = \overline{G_4} G_3 \overline{G_2} + \overline{G_4}\, \overline{G_3} G_2 + G_4 \overline{G_3}\, \overline{G_2} + G_4 G_3$

$= G_4 \oplus G_3 \oplus G_2 = B_3 \oplus G_2$



$B_1 \rightarrow$

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PROCEDURE :

1) Place the EX-OR IC on the breadboard.
2) Make the connections as shown in the circuit diagram first ~~for~~
3) Binary to Gray and then for gray to Binary conversion.
4) Positive terminal of LED at the output ends (4 leds for 4 outputs) and negative terminal is grounded.
5) Turn on the supply to see the change in circuit when different inputs are given and observe corresponding outputs.
6) Turn off powersupply when not in use.

RESULT:

(a) Truth table of Binary to Gray conversion was verified
(b) Truth table of Gray to Binary conversion was also verified.

PRECAUTIONS:

1) Make neat and tight connections
2) Turn off the power supply after use.
3) Draw the circuit diagram before drawing on main circuit / bread board.
4) Do not ~~short~~ circuit.

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~~4th k-map -~~

~~$B_1 = \bar{G_4}\,\bar{G_3}\,\bar{G_2}\,G_1 + \bar{G_4}\,\bar{G_3}\,G_2\,\bar{G_1} + \bar{G_4}\,G_3\,G_2\,G_1 + G_4\,G_3\,\bar{G_2}\,\bar{G_1}$~~

~~$+\ G_4\,\bar{G_3}\,\bar{G_2}\,G_1 + G_4\,G_3\,G_2\,\bar{G_1} + G_4\,\bar{G_3}\,G_2\,G_1 +$~~

~~$\bar{G_1}\,G_2\,G_3\,G_4$~~

Teacher's Signature :

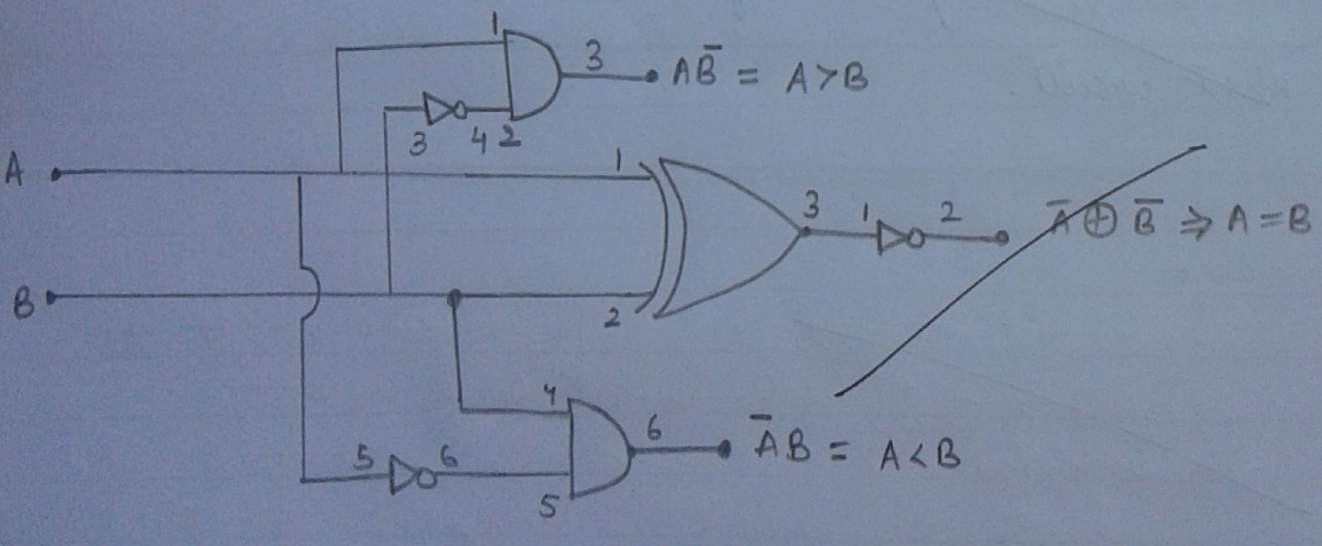
EXPERIMENT NO : 7

AIM: To study the 1 bit magnitude comparator and verify its truth table

TRUTH TABLE:

A	B	A > B	A = B	A < B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0
		$A\bar{B}$	$\bar{A} \oplus \bar{B}$	$\bar{A}B$

LOGIC CIRCUIT DIAGRAM :



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EXPERIMENT NO: 7

AIM: To study a 1 bit magnitude comparator, and verify its table.

APPARATUS:

BreadBoard, IC's (7404, 7408, 7486), 3 LED's, connecting wires, supply.

THEORY:

A magnitude comparator is a combinational circuit that compares two numbers, A and B and determines the relative magnitudes. The output of the comparison is specified by three binary variables that indicates whether $A>B$, $A=B$, $A<B$.
The circuit of comparing two n-bit numbers has 2^{2n} entries in the truth table.

PROCEDURE:

1. Make the connections on the breadboard using the components mentioned as shown in the diagram.
2. The ~~positive terminal~~ of the LED's are connected to 3, 6, of the AND gate and negative to the ground pin.
3. Positive terminal of 3rd LED is connected to 2nd pin of NOT IC and negative to ground.
4. The LED glows only when the either of the 3 conditions ~~are~~ is fulfilled i.e

   $A>B$ [LED at the 3rd pin of AND gate glows]
   $A=B$ [LED at the 2nd pin of NOT gate glows]
   $A<B$ [LED at the 6th pin of AND gate glows]

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5. The above steps are repeated for observing the outcome at every combination.

PRECAUTIONS:

1. Make the connections correct and tight.
2. Turn off the supply when not in use.
3. Take care of the (+ve) and (-ve) terminals of LED before connecting.
4. Do, observe, the notch of the IC and then fix it on BreadBoard.

RESULT:

The magnitude comparator was studied successfully and its table was verified.

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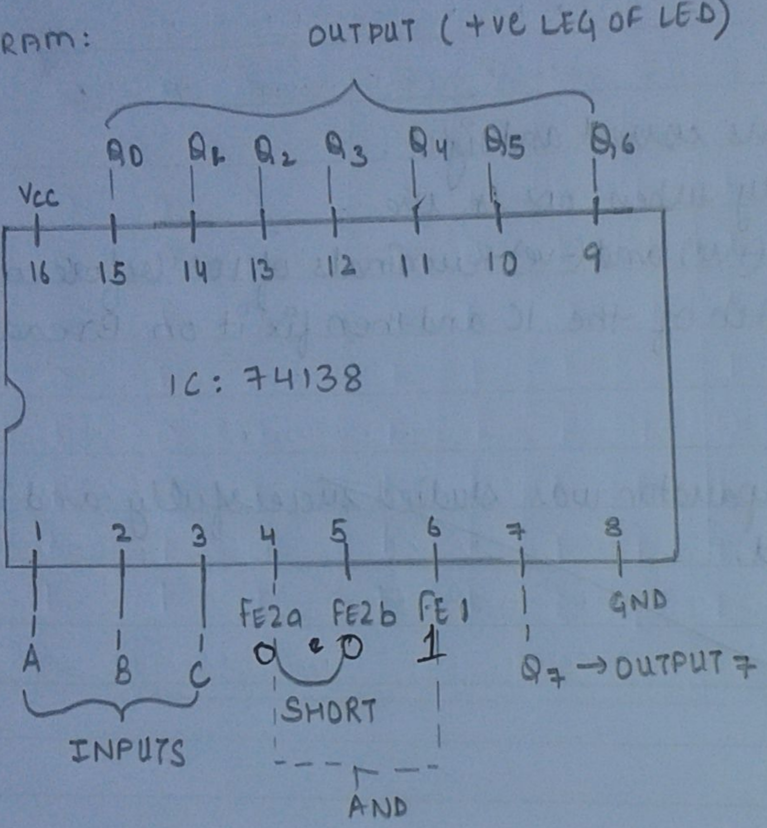
EXPERIMENT NO: 8

AIM: To study a 3 : 8 Decoder and verify its truth table

CIRCUIT DIAGRAM:



ENABLE = $FE1(\overline{Fe2a + Fe2b})$

EXPERIMENT NO: 8

AIM:

To study a 3:8 decoder and verify its truth table.

APPARATUS:

BreadBoard, connecting wires, supply, 8 led's, 74138 IC.

THEORY:

DECODER:

A decoder is a combinational circuit that converts binary information from n- input lines to a maximum of 2^n unique output lines.

3-8 DECODER:

There are 3 inputs which are decoded into 8 outputs, each output represents one of the minterms of 3 input variables. The three inverters provide the compliment of the inputs and each one of eight AND gates generate one of minterms.

A particular application of this decoder would be binary to octal conversion. The input variables may represents a binary number and the outputs will then represent the eight digits in the octal number system.

PROCEDURE:

Make the connections are shown in the circuit diagram.

Make 16^{th} pin of 74138 IC as High i.e Vcc and 8^{th} pin as ground.

On the 1^{st}, 2^{nd} and 3^{rd} pin, give the inputs, by connecting them with Vcc to give 1 and with ground to give 0.

TRUTH TABLE OF A DECODER HAVING INBUILT NAND

ENABLE	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

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4. 4th, 5th and 6th are a combination and forms enable part, where 4th and 5th pin (Fe2a+Fe2b) are short circuited and then are (AND) in that relation with FE1 i.e on 6th pin.
5. Your 8 outputs are on 7th, 9th, 10th, 11th, 12th, 13th, 14th, 15th pins, i.e positive leg of the LED is on these terminals and negative legs are grounded.
6. Each of the combination of truth table is thereby verified.

PRECAUTIONS:

1. Turn off the power supply when not in use.
2. Make, the connection tight.
3. Do, ground the series of LED's ~~ifth~~ if ground is given on any other line of bread board.

RESULT:

The 3:8 ~~decoder~~ was successfully studied

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