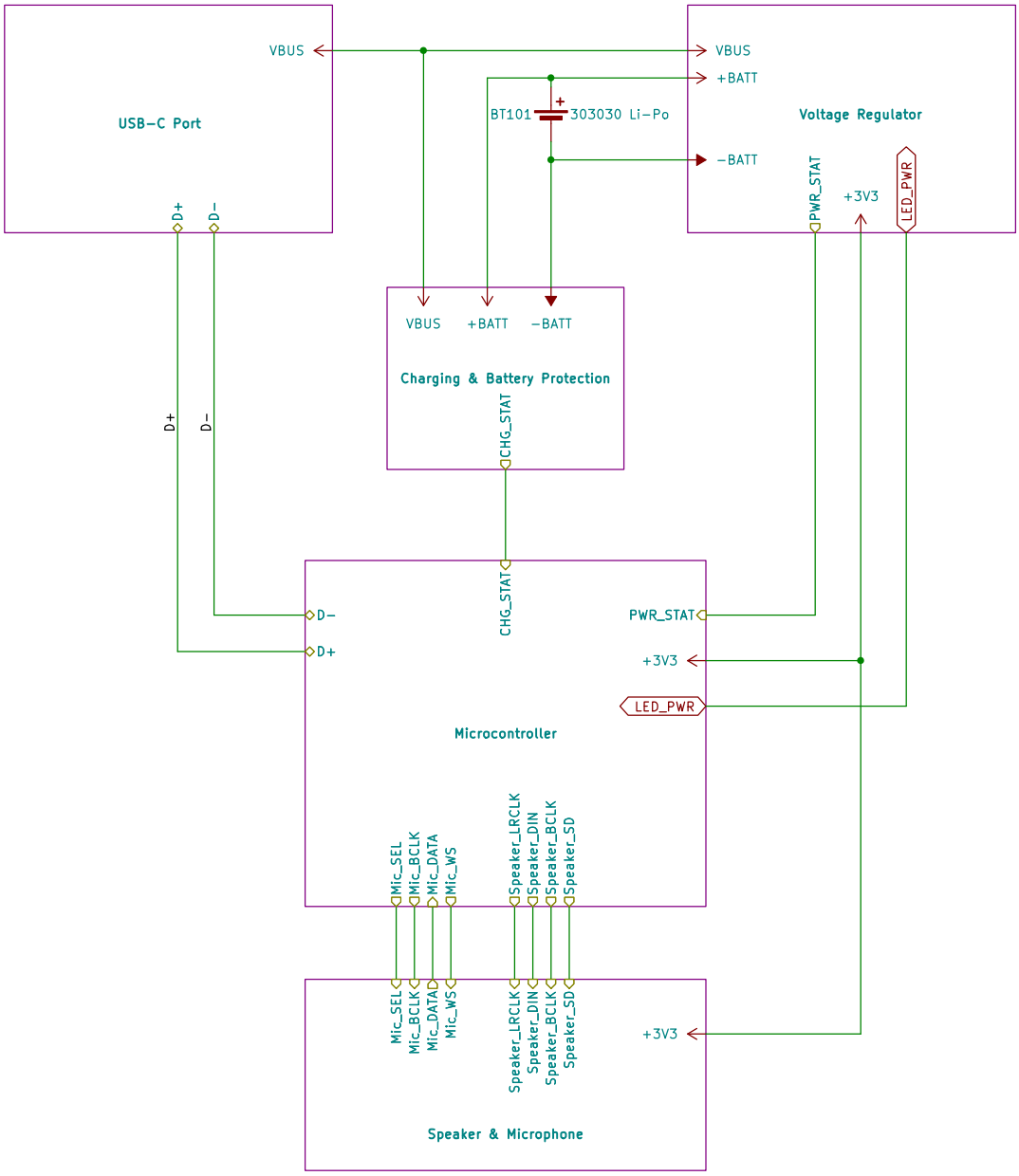
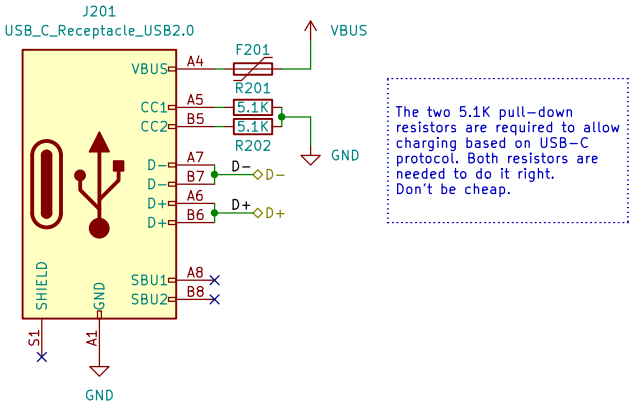


Home Sweet Home Assistant		
Sheet: /		
File: Comms Badge Voice Assistant Project.kicad_sch		
Title: Comms Badge Voice Assistant		
Size: A	Date: 2024-03-02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 1/14



Home Sweet Home Assistant		
Sheet: /USB−C Port/ File: USB−C_Port.kicad_sch		
Title: Comms Badge Voice Assistant		
Size: A	Date: 2024−03−02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 2/14

Based on the Typical Application schematic on page 1 of the MCP73831 Family Data Sheet.

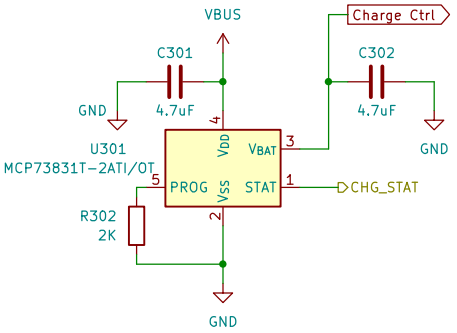
Fast charge current regulation can be scaled by placing a programming resistor (R_{PROG}) from the PROG input to VSS. The program resistor and the charge current are calculated using the following equation:

$I_{REG} = 1000V / R_{PROG}$

Where:
R_{PROG} = kOhms
I_{REG} = mA
[^1]

A 2K resistor results in a 500mA charging rate.

Charging Circuit



The state of the STAT pin is HIGH when in "Charge Complete – Standby" state and LOW when in "Preconditioning", "Constant-Current Fast Charge", or "Constant Voltage" states.

The CHG_STAT pin is connected to the Microcontroller which will change the Status LED to indicate red for charging and green for fully charged.

Mosfet Considerations:

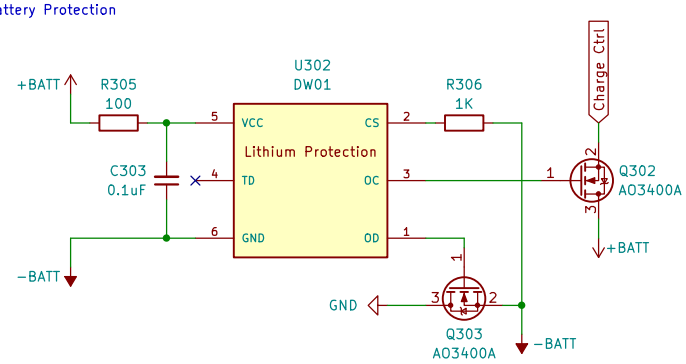
Expected Charge Current: 500mA
Expected Max Load Current: 600mA+

MCP73831:
STAT Pin High Output Voltage: VDD-0.4 – VDD-0.4-1
STAT Pin Low Output Voltage: 0.4 – 1V

DW01:
OD & OC Pin Output "H" Voltage: VCC-0.1 – VCC-0.02
OD & OC Pin Output "L" Voltage: 0.1 – 0.5V

Based on the Typical Application Circuit on page 3 of the DW01-P_DataSheet_V10.pdf datasheet.

Battery Protection



Normally, based on the Typical Application Circuit, the mosfets connected to the OC and OD pins are also connected together and even frequently use a dual mosfet to cut down on components. Because the DW01 will be used in conjuction with the MCP73831, here the Overcharge Protection and Overdischarge Protection are separated and use unconnected mosfets.

The Overcharge Protection cuts off the flow from the Vbat pin of the MCP73831 to the positive terminal of the battery when the voltage reaches 4.2V.

The Overdischarge Protection is connected between the Load of the running components and the negative battery terminal to break the circuit and stop all activity if the battery reaches a low voltage of 2.4V.

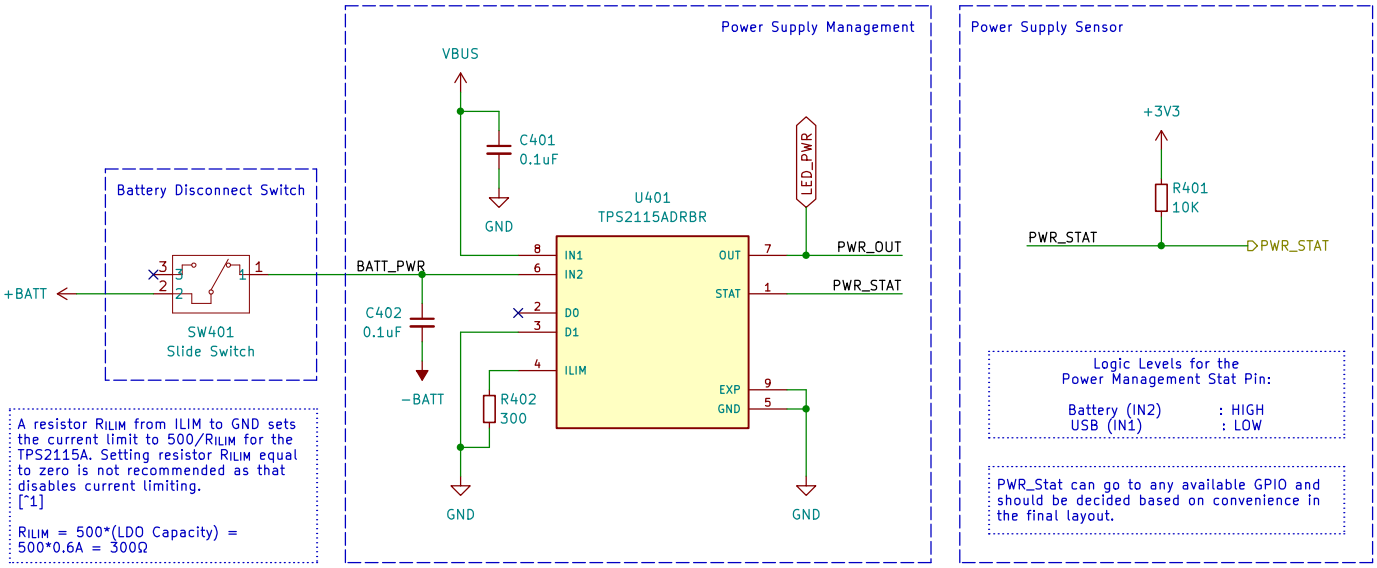
[^1] MCP73831-Family-Data-Sheet-DS20001984H.pdf (page 15)

Home Sweet Home Assistant

Sheet: /Charging & Battery Protection/
File: Charging_Battery_Protection.kicad_sch

Title: Comms Badge Voice Assistant

Size: A	Date: 2024-03-02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 3/14



A resistor RILIM from ILIM to GND sets the current limit to 500/RILIM for the TPS2115A. Setting resistor RILIM equal to zero is not recommended as that disables current limiting. [^1]

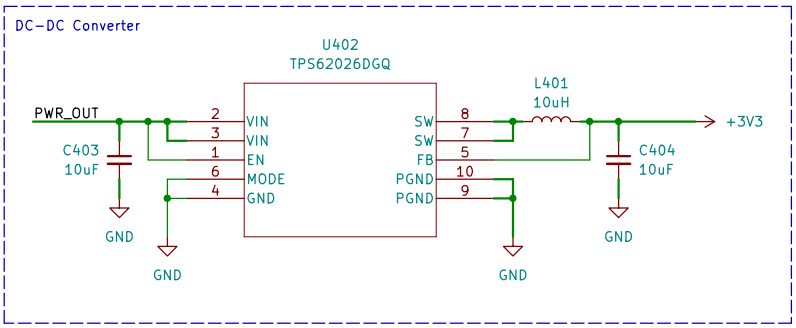
RILIM = 500*(LDO Capacity) = 500*0.6A = 300Ω

Logic Levels for the Power Management Stat Pin:

Battery (IN2) : HIGH
USB (IN1) : LOW

PWR_Stat can go to any available GPIO and should be decided based on convenience in the final layout.

This circuit is based on Figure 21. "TPS62026 Fixed 3.3 V Output Using 10 µH inductor" in the Datasheet [^2]



The TPS6202x uses typically a 10−µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. When changing inductor values, the product of the inductor value times the output−capacitor value (L*C) should stay constant. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance directly influences the efficiency of the converter. Therefore an inductor with the lowest dc resistance should be selected for highest efficiency. [^5]

Connecting the MODE pin of the TPS6202x to GND enables the automatic PWM and power save mode operation. Pulling the TPS6202x MODE pin high forces the converter to operate constantly in the PWM mode even at light load currents. [^3]

Pulling the EN low forces the part into shutdown mode. For proper operation the enable (EN) pin must be terminated and should not be left floating. Pulling EN high starts up the device with the softstart as described under the section Softstart. [^4]

If the layout is not carefully done, the regulator might show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths as indicated in bold. These traces should be routed first. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

To further minimize noise from coupling into the feedback network and feedback pin, the ground plane or ground traces should be used for shielding. A common ground plane or a star ground as shown in the figure should be used. This becomes very important especially at high switching frequencies of 1.25 MHz.

The PowerPAD of the 10−pin MSOP package has an area of 1.52mm x 1.79mm (±0.05 mm) and must be soldered to the PCB to lower the thermal resistance. Thermal vias to the next layer further reduce the thermal resistance. [^6]

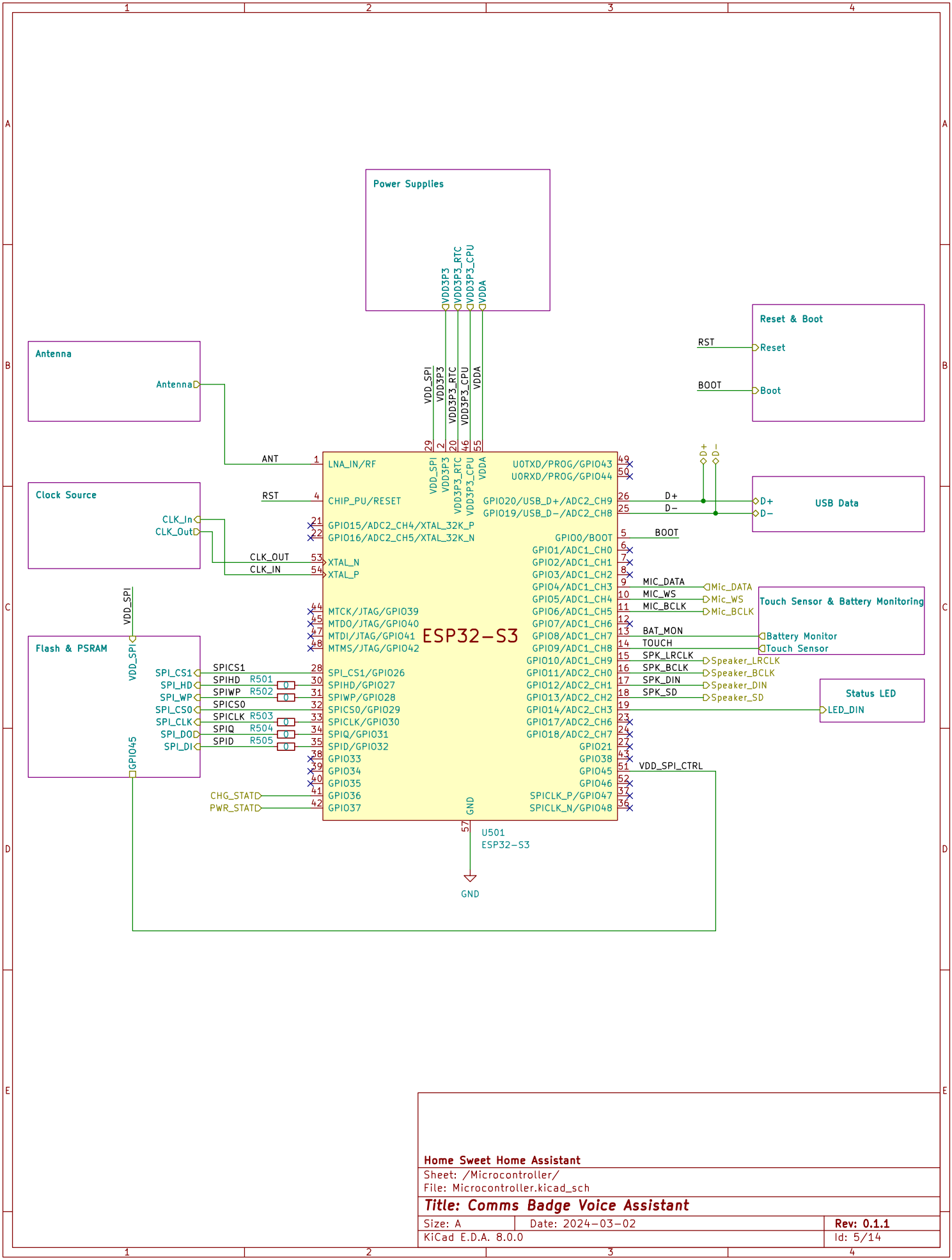
[^1] tps2114a.pdf (page 17)
[^2] 2304140030_Texas−Instruments−TPS62026DGQ_C1356111.pdf (page 17)
[^3] 2304140030_Texas−Instruments−TPS62026DGQ_C1356111.pdf (page 11)
[^4] 2304140030_Texas−Instruments−TPS62026DGQ_C1356111.pdf (page 12)
[^5] 2304140030_Texas−Instruments−TPS62026DGQ_C1356111.pdf (pages 13−14)
[^6] 2304140030_Texas−Instruments−TPS62026DGQ_C1356111.pdf (pages 15−16)

Home Sweet Home Assistant

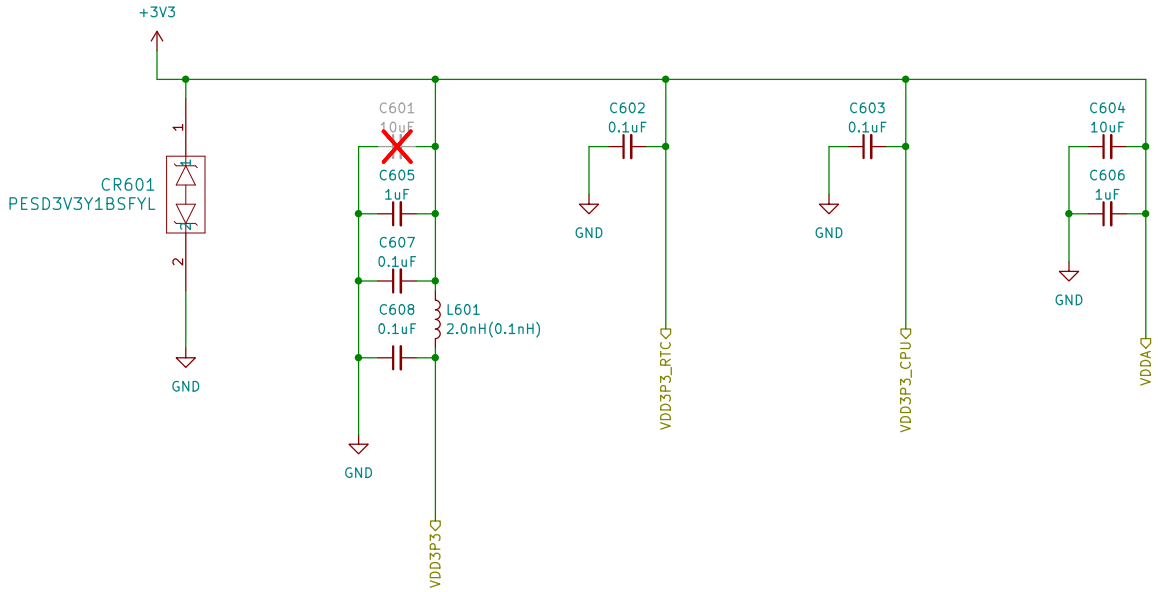
Sheet: /Voltage Regulator/
File: Voltage_Regulator.kicad_sch

Title: Comms Badge Voice Assistant

Size: A	Date: 2024−03−02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 4/14



Home Sweet Home Assistant		
Sheet: /Microcontroller/		
File: Microcontroller.kicad_sch		
Title: Comms Badge Voice Assistant		
Size: A	Date: 2024-03-02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 5/14



General Guidelines [^1]

Four-layer PCB design is preferred.

The power traces should be routed on the inner third layer whenever possible.

Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.

The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.

If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with solder paste, and place ground vias in the gaps, as shown in Figure ESP32-S3 Power Traces in a Four-layer PCB Design. This can avoid chip displacement caused by tin leakage and bubbles when soldering the module EPAD to the substrate.

3.3V Power Layout [^2]

The 3.3 V power layout should meet the following guidelines:

The ESD protection diode is placed next to the power port (circled in red in Figure ESP32-S3 Power Traces in a Four-layer PCB Design). The power trace should have a 10 µF capacitor on its way before entering into the chip, and a 0.1 or 1 µF capacitor could also be used in conjunction. After that, the power traces are divided into several branches using a star-shaped topology, which reduces the coupling between different power pins. Note that all decoupling capacitors should be placed close to the corresponding power pin, and ground vias should be added close to the capacitor's ground pad to ensure a short return path.

In Figure ESP32-S3 Power Traces in a Four-layer PCB Design, the 10 µF capacitor is shared by the analog power supply VDD3P3, and the power entrance since the analog power is close to the chip power entrance. If the chip power entrance is not near VDD3P3, it is recommended to add a 10 µF capacitor to both the chip power entrance and VDD3P3. Also, reserve two 1 µF capacitors if space permits.

The width of the main power traces should be no less than 25 mil. The width of VDD3P3 power traces should be no less than 20 mil. The recommended width of other power traces is 10 mil.

Analog Power Layout [^3]

The analog power layout should meet the following guidelines:

As shown in Figure ESP32-S3 Analog Power Traces in a Four-layer PCB Design, it is recommended to connect the capacitor to ground in the CLC filter circuit near VDD3P3 to the fourth layer through a via, and maintain a keep-out area on other layers. The purpose is to further reduce harmonic interference.

VDD3P3 analog power supply should be surrounded by ground copper. It is required to add GND isolation between VDD3P3, power trace and the surrounding GPIO and RF traces, and place vias whenever possible.

[^1] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#general-guidelines

[^2] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#v-power-layout

[^3] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#analog-power-layout

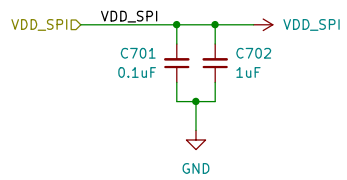
Home Sweet Home Assistant

Sheet: /Microcontroller/Power Supplies/
File: Microcontroller_Power_Supplies.kicad_sch

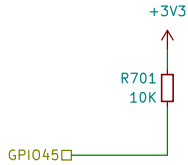
Title: Comms Badge Voice Assistant

Size: A	Date: 2024-03-02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 6/14

VDD_SPI



GPIO45 VDD_SPI Setting



GPIO45 is used to select the VDD_SPI power supply voltage at reset:

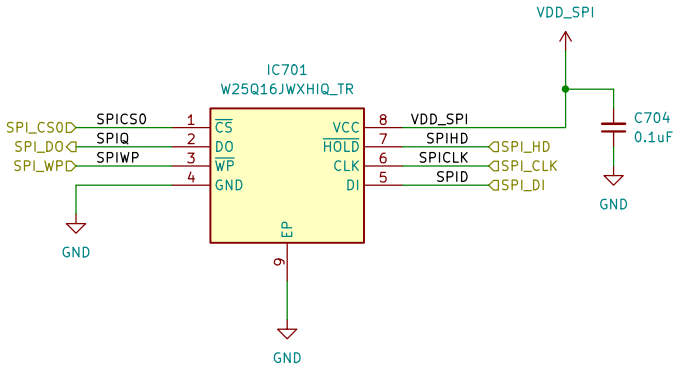
- GPIO45 = 0, VDD_SPI pin is powered directly from VDD3P3_RTC via resistor R_{SPI} . Typically this voltage is 3.3 V. For more information, see Figure: ESP32-S3 Power Scheme in ESP32-S3 Datasheet.
- GPIO45 = 1, VDD_SPI pin is powered from internal 1.8 V LDO.

This functionality can be overridden by setting eFuse bit EFUSE_VDD_SPI_FORCE to 1, in which case the EFUSE_VDD_SPI_TIEH determines the VDD_SPI voltage:

- EFUSE_VDD_SPI_TIEH = 0, VDD_SPI connects to 1.8 V LDO.
- EFUSE_VDD_SPI_TIEH = 1, VDD_SPI connects to VDD3P3_RTC.

[^1]

Flash

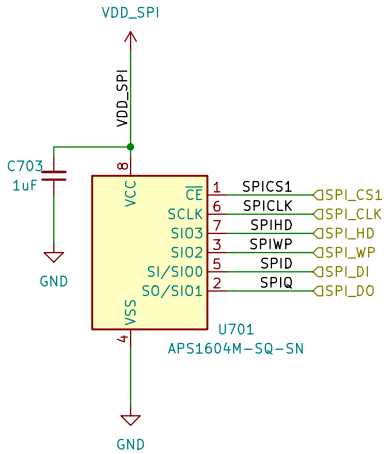


For this project, I am adding a 16Mb flash.

Considerations affecting the choice of flash and PSRAM include the resource-intensive audio and voice assistant functions that make up the core of this project as well as a concern for power usage in a battery-powered wearable. The final decision ultimately came down to package size. Using a XSON-8-EP(2x3) takes up significantly less space than the usual SOIC-8 package, and space is a premium in this project.

The W25Q16JWXHIQ TR runs on 1.8V, which means that the pull-up resistor on GPIO45 will be required to be populated or the eFuse bit set to 0.

PSRAM



PSRAM is an optional addition to the ESP32-S3, but because this project involves resource-intensive functions like audio and voice assistant capabilities, a PSRAM is likely necessary. As with the flash, two 16Mb options have been chosen with the same footprint for easy conversion. The decision for which is to be used is determined by the flash that is chosen. Because they are both running from the same VDD_SPI and share a number of pins, they must also share the same voltage requirements.

In addition to the reasons above, I have chosen 16Mb in order to hopefully have overhead room for expansion of the project over time. One feature that I might like to add is Bluetooth, which is notorious for causing crashes when used with audio and voice assistant functions together. Having a sizeable PSRAM will at least leave room to manage the RAM requirements, though it remains to be seen if the CPU requirements will be met.

APS1604M-3SQR-SN:
VDD_SPI: 3.3V

APS1604M-SQ-SN
VDD_SPI: 1.8V

The layout for flash and PSRAM should follow the guidelines below: [^2]

Place the zero-ohm series resistors on the SPI lines close to the chip.

Route the SPI traces on the inner layer (e.g., the third layer) whenever possible, and add ground copper and ground vias around the clock and data traces of SPI separately.

Place the 0.1 µF capacitor to ground at the VDD_SPI close to corresponding flash and PSRAM power pins.

Octal SPI traces should have matching lengths.

[^1] 2310081041_Espressif-Systems-ESP32-S3_C2913192.pdf (pages 23-24)
&
https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#digital-power-supply

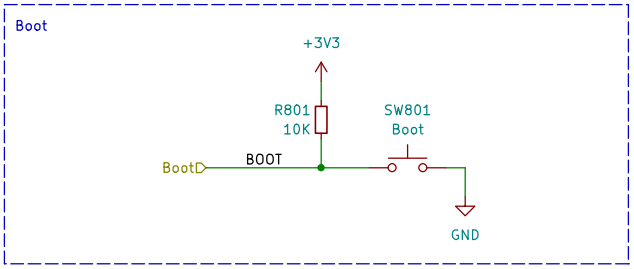
[^2] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#flash-and-psram

Home Sweet Home Assistant

Sheet: /Microcontroller/Flash & PSRAM/
File: Flash_PSRAM.kicad_sch

Title: Comms Badge Voice Assistant

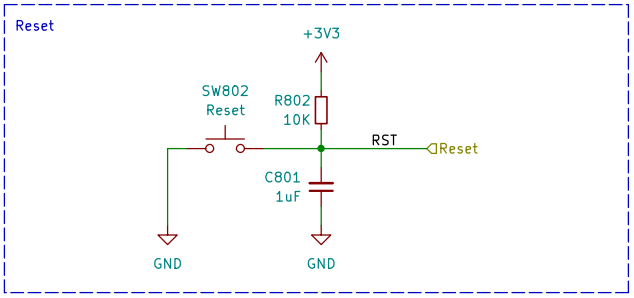
Size: A	Date: 2024-03-02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 7/14



Do not add high-value capacitors at GPIO0 (BOOT), otherwise, the chip may not boot successfully. [^1]

GPIO0 must have a value of 1 for Default Config boot mode. In order to enter Joint Download Boot Mode, GPIOs 0 and 46 must both have a value of 0 at reset.

GPIO46 has an internal weak pull-down resistor enabled in its default configuration. [^2]



To reset the chip, keep the reset voltage V_{IL_nRST} in the range of $(-0.3 \sim 0.25 \times VDD)$ V.

To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible.

[^3]

[^1] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#strapping-pins

[^2] esp32-s3_technical_reference_manual_en.pdf (pages 526-527)

[^3] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#chip-power-up-and-reset-timing

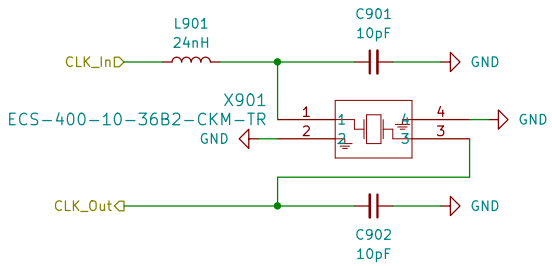
Home Sweet Home Assistant

Sheet: /Microcontroller/Reset & Boot/
File: Reset_Boot.kicad_sch

Title: Comms Badge Voice Assistant

Size: A	Date: 2024-03-02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 8/14

Please add a series component (resistor or inductor) on the XTAL_P clock trace. Initially, it is suggested to use an inductor of 24 nH to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be adjusted after an overall test. [^1]



Cstray includes the pin to pin input and output capacitance of the microprocessor chip at the Crystal 1 and Crystal 2 pins, plus any parasitic capacitances. As a rule of thumb, Cstray may be assumed to equal 5.0 pF. [^2]

https://ecsxtal.com/crystal-load-capacitance-calculator/ used to calculate C901 and C902 to be 10pF assuming the rule-of-thumb 5pF for Cstray.

Properties:

Frequency: 40MHz
Accuracy: +-10ppm
Load Capacitance: 10pF
ESR: 30Ω
Frequency Stability: +-10ppm
Drive Level: 100uW Max

The initial values of external capacitors C1 and C4 can be determined according to the formula: [^1]

$C_L = (C901 \times C902)/(C901 + C902) + C_{stray}$

where the value of C_L (load capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C4 need to be further adjusted after an overall test as below:

Select TX tone mode using the Certification and Test Tool.
Observe the 2.4 GHz signal with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
Adjust the frequency offset to be within ±10 ppm (recommended) by adjusting the external load capacitance.

When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.

When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.

External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

The layout of the crystal should follow the guidelines below: [^3]

Ensure a complete GND plane for the RF, crystal, and chip.

The crystal should be placed far from the clock pin to avoid interference on the chip. The gap should be at least 2.0 mm. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.

There should be no vias for the clock input and output traces, which means the traces cannot cross layers. The clock traces should not intersect with each other.

Components in series to the crystal trace should be placed close to the chip side.

The external matching capacitors should be placed on the two sides of the crystal, preferably at the end of the clock trace, but not connected directly to the series components. This is to make sure the ground pad of the capacitor is close to that of the crystal.

Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.

As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

[^1] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#external-crystal-clock-source-compulsory

[^2] Quartz Crystal Design Parameters.pdf (page 3)

[^3] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#crystal

Home Sweet Home Assistant

Sheet: /Microcontroller/Clock Source/
File: Clock_Source.kicad_sch

Title: Comms Badge Voice Assistant

Size: A	Date: 2024-03-02	**Rev: 0.1.1**
KiCad E.D.A. 8.0.0		Id: 9/14

For the RF traces on the PCB board, 50 Ω impedance control is required.

For the chip matching circuit, it must be placed close to the chip. A CLC structure is preferred.

The CLC structure is mainly used to adjust the impedance point and suppress harmonics, and a set of LC can be added if space permits.

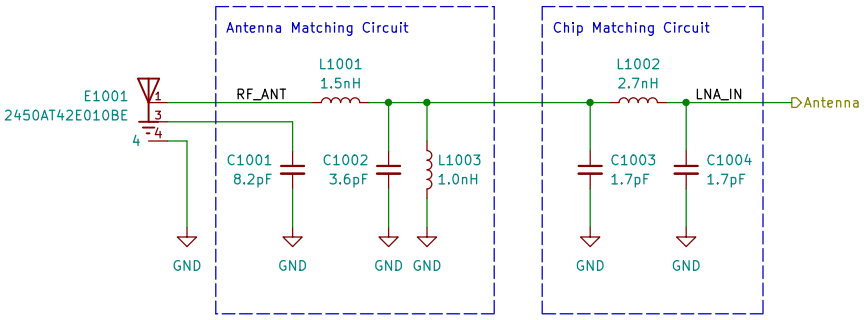
The RF matching circuit is shown in Figure ESP32-S3 Schematic for RF Matching.

For the antenna and the antenna matching circuit, to ensure radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

[^1]

Make sure to have Pin 2 soldered to its PCB land pad but not connected to GND or input, it must be NC (or floating). [^2]

The Antenna Matching Circuit values are based on Mounting Consideration 1: Evaluation Board 2 (Thickness = 2.5mm) in the datasheet. The values may require adjusting on the final board. [^3]



Follow the procedure at https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#rf-tuning to determine the value of the components in the chip and antenna matching circuits.

Recommended Value Ranges for Components in Chip Matching Circuit [^4]

Reference Designator	Recommended Value Range	Serial No.
C11	1.2 ~ 1.8 pF	GRM0335C1H1RXBA01D
L2	2.4 ~ 3.0 nH	LQP03TN2NXB02D
C12	1.8 ~ 1.2 pF	GRM0335C1H1RXBA01D

The RF layout should meet the following guidelines: [^5]

A π-type matching circuit should be added to the RF trace and placed close to the chip, in a zigzag.

The RF trace should have a 50 Ω characteristic impedance. The reference plane is the second layer. For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown below.

Add a stub to the ground at the ground pad of the first matching capacitor to suppress the second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure ESP32-S3 Stub in a Four-layer PCB Design is the stub. Note that a stub is not required for package types above 0201.

The RF trace should have a consistent width and not branch out. It should be as short as possible with dense ground vias around for interference shielding.

The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.

The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.

There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR SDRAM, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

[^1] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#rf-circuit

[^2] 2450AT42E010B.pdf (page 1)

[^3] 2450AT42E010B.pdf (page 3)

[^4] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#rf-tuning

[^5] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#rf

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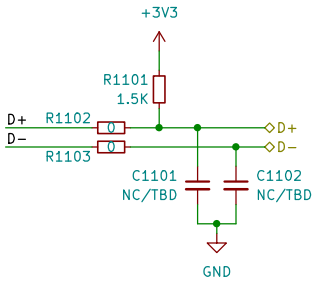
GPIO19 and GPIO20 can be used as D− and D+ of USB respectively. It is recommended to populate zero−ohm series resistors between the mentioned pins and the USB connector. Also, reserve a footprint for a capacitor to ground on each trace, which can be used to address signal integrity and noise suppresion. Note that both components should be placed close to the chip.

Note that USB_D+ will have level output, so please add a pull−up resistor to determine the initial high−level output voltage. Based on the USB2.0 specifications, the standard value for the USB_D+ pull−up resistor for a Full−Speed USB device is typically 1.5KΩ.

If the USB−OTG Download Boot mode is not needed, it is suggested to disable the USB−OTG Download Boot mode by setting the eFuse bit EFUSE_DIS_USB_OTG_DOWNLOAD_MODE to avoid IO pad state change. This particular project does not require it to act as a USB device during operation, so only the USB Serial/JTAG Controller will be used for flashing firmware and debugging.

[^1]



The USB layout should meet the following guidelines:

Place the RC circuit on the USB traces close to the chip side.

Use differential pairs and route them in parallel at equal lengths.

Make sure there is a complete reference ground plane and surround the USB traces with ground copper.

[^2]

[^1] https://docs.espressif.com/projects/esp−hardware−design−guidelines/en/latest/esp32s3/schematic−checklist.html#usb

[^2] https://docs.espressif.com/projects/esp−hardware−design−guidelines/en/latest/esp32s3/pcb−layout−design.html#usb

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Sheet: /Microcontroller/USB Data/
File: USB_Data.kicad_sch

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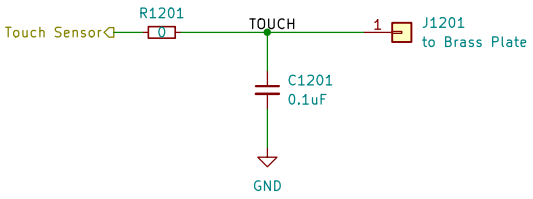
ADC2 has no restrictions, unless there is an on-going Wi-Fi connection. ADC2_CH... analog functions(see Table 2-4 RTC and Analog Pin Functions) cannot be used with Wi-Fi simultaneously. [^1]

Therefore, for this project, analog functions such as the Touch Sensor and battery monitoring are not appropriate for ADC2 pins.

Touch Sensor



When using the touch function, it is recommended to populate a zero-ohm series resistor at the chip side to reduce the coupling noise and interference on the line, and to strengthen the ESD protection. The recommended resistance is from 470Ω to 2KΩ, preferably 510Ω. The specific value depends on the actual test results of the product. [^2] The series resistor should be placed within 1 mm of the touch pin. [^3]

When deciding which GPIO to use, the adjacent pins should not be assigned high-frequency signals such as SPI, I2C, PWM, etc. [^4] After testing all touch sensor channels, it is concluded that channels Touch5-9 are less prone to be affected by the RTC IO output current. Therefore, Touch5-9 are recommended for designs that require high stability. [^5]

The touch sensor pin will terminate at a wire connector. The other end of the wire will be soldered to the underside of the brass plate which will serve as both the face of the device as well as a part of the touch sensor.

Figure ESP32-S3 Sensor Track Routing Requirements illustrates the general guidelines to routing traces. Specifically,

The trace should be as short as possible and no longer than 300 mm.

The trace width (W) can not be larger than 0.18 mm (7 mil).

The alignment angle (R) should not be less than 90°.

The trace-to-ground gap (S) should be in the range of 0.5 mm to 1 mm.

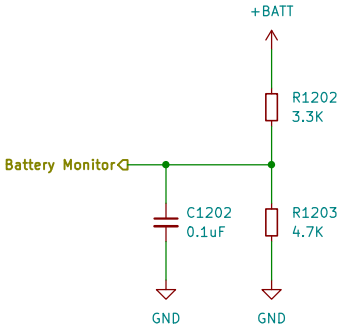
The electrode diameter (D) should be in the range of 8 mm to 15 mm.

Hatched ground should be added around the electrodes and traces.

The traces should be isolated well and routed away from that of the antenna.

[^6]

Battery Monitoring



The calibrated ADC results after hardware calibration and software calibration are shown in the list below. For higher accuracy, you may implement your own calibration methods.

When ATTEN=0 and the effective measurement range is 0 ~ 850 mV, the total error is ±5 mV.
When ATTEN=1 and the effective measurement range is 0 ~ 1100 mV, esp32c6=, the total error is ±6 mV.
When ATTEN=2 and the effective measurement range is 0 ~ 1600 mV, the total error is ±10 mV.
When ATTEN=3 and the effective measurement range is 0 ~ 2900 mV, the total error is ±50 mV.

[^7]

The Voltage Divider takes the maximum V_{IN} of 4.2V and returns a V_{OUT} of 2.468V, which is comfortably below the maximum effective measurement when ATTEN=3 with a power dissipation of 0.002W.

[^1] 2310081041_Espressif-Systems-ESP32-S3_C2913192.pdf (page 20)

[^2] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#touch-sensor

[^3] https://github.com/espressif/esp-iot-solution/blob/release/v1.0/documents/touch_pad_solution/touch_sensor_design_en.md#338-series-resistor

[^4] https://github.com/espressif/esp-iot-solution/blob/release/v1.0/documents/touch_pad_solution/touch_sensor_design_en.md#321-pin-assignment

[^5] https://github.com/espressif/esp-iot-solution/blob/release/v1.0/documents/touch_pad_solution/touch_sensor_design_en.md#323-power-domains

[^6] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#pcb-layout

[^7] https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#adc

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File: Touch_Sensor_Battery_Monitoring.kicad_sch

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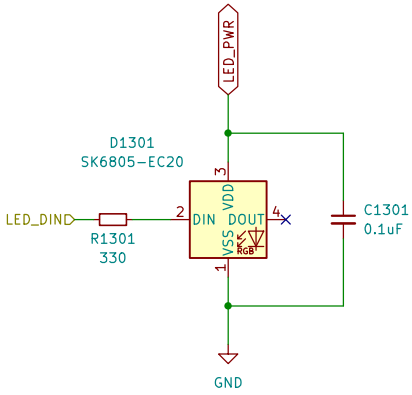

https://learn.adafruit.com/adafruit-neopixel-uberguide

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Sheet: /Microcontroller/Status LED/
File: Status_LED.kicad_sch

Title: Comms Badge Voice Assistant

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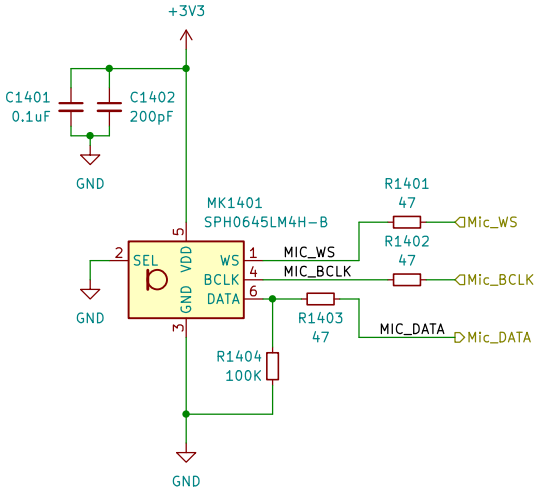
Microphone

The SPH0645LM4H microphone is a "bottom port" microphone, which means that it will have to be mounted on the underside of the PCB with a hole for the microphone's audio input port. The placement on the PCB will be influenced by the location of the Li-Po battery, which will be somewhat centrally located on the back side of the PCB.

Notes: [^1]
1. A decoupling capacitor (C1401) mounted as close as possible is required for optimum SNR.
2. An RF filter Capacitor (C1402) in the range of 20-200pF may be needed depending on the RF environment.
3. If both decoupling and RF filter capacitors are used, the RF filter capacitors should be the closest to the microphone.

The SELECT pin determines when the microphone drives the Data pin. When SELECT = LOW the DATA pin drives the SDIN bus when WS = LOW otherwise DATA = tri-state. When operating a single microphone on an I2S bus, a pull down resistor (100K Ohms) should be placed from the Data pin to ground to insure the bus capacitance is discharged. [^1]



The Microphone is connected to one of the two I2S interfaces on the ESP32-S3 microcontroller. The exact pins will be decided during the process of laying out the PCB based on what is most convenient.

R1401-R1403 are included to dampen or terminate their respective traces. If the traces are electrically long then they should be controlled impedance traces with impedance in the 50-120 Ohm range. Traces are considered electrically long when the length of the trace (in inches) is greater than 2 times the rise/fall time (in nS). According to the datasheet, the Clock Rise/Fall Time is 10nS. [^2]

Even if the traces are not electrically long, R1401-R1403 can be used as dampening resistors (27-51 Ohms) to improve signal integrity by reducing overshoots and ringing caused by stray inductance and capacitance. In either case, R1401-R1403 are to be placed as close as possible to the device that drives the trace (signal source).

The decoupling capacitors (C1401-1402) are most effective if the trace inductance between the capacitor and microphone is minimized. This can be accomplished by using short, wide traces. If a ground plane is used under the microphone, then connect the capacitor ground pads directly to the plane with vias without any trace used.

[^3]

Speaker

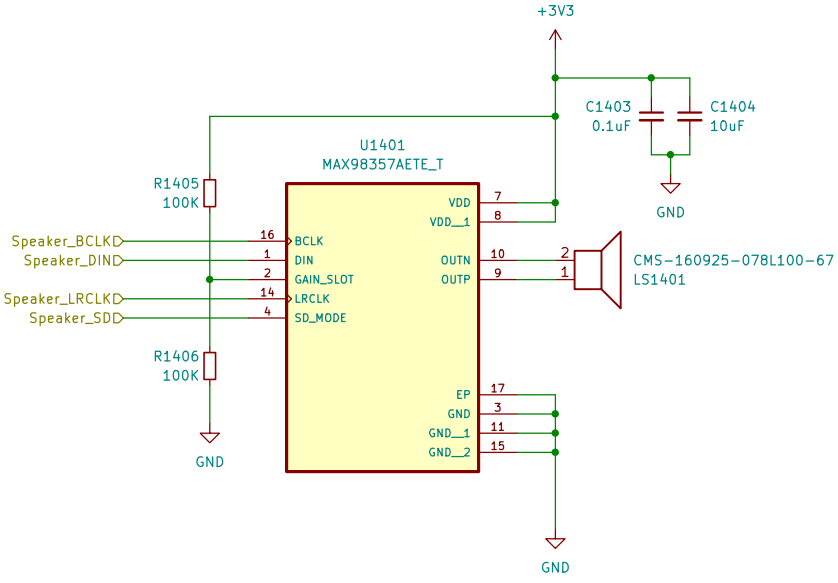
The Speaker amplifier is connected to the second of the I2S interfaces on the ESP32-S3 microcontroller. The exact pins will be decided during the process of laying out the PCB based on what is the most convenient.

For simplicity's sake, both the microphone and speaker will be using the left channel modes. The left channel does not require any resistor on the speaker's SD_MODE pin, which is the only reason the left channel is preferential. [^4]

Gain can be set by using different configurations connected to GAIN_SLOT.

15dB: if a 100K resistor is connected between GAIN_SLOT and GND
12dB: if GAIN_SLOT is connected directly to GND by bridging the R1406 footprint
9dB : if GAIN_SLOT is not connected to anything (this is the default) and no resistor footprints are populated
6dB : if GAIN_SLOT is connected directly to VDD by bridging the R1405 footprint
3dB : if a 100K resistor is connected between GAIN_SLOT and VDD

[^5]



[^1] SPH0645LM4H-B.pdf (page 6)
[^2] SPH0645LM4H-B.pdf (page 3)
[^3] SPH0645LM4H-B.pdf (page 7)

[^4] MAX98357A-MAX98357B.pdf (page 17)
[^5] MAX98357A-MAX98357B.pdf (page 28)

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