

## Lab 4

### Logic Circuits (EET 241)

**Total Points: 100**

**Objective:** Demonstrate experimentally the truth tables for NAND, NOR, Exclusive OR gate.

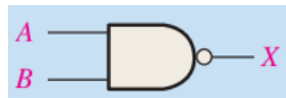
**Materials Needed:**

7400 Quad 2-Input NAND Gate – 1 piece  
7402 Quad 2-Input NOR Gate – 1 piece  
7486 Quad 2-Input Exclusive-OR Gate – 1 piece  
330-ohm resistor – 2 pieces  
Light Emitting Diodes (LEDs) – 2 pieces  
DC Power Supply

**Theory:**

**NAND Gate**

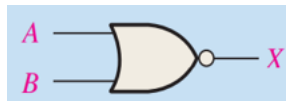
The term NAND is a contraction of NOT-AND and implies an AND function with a complemented (inverted) output. For a 2-input NAND gate, output X is LOW only when inputs A and B are HIGH; X is HIGH when either A or B is LOW, or when both A and B are LOW.



| Inputs |   | Output |
|--------|---|--------|
| A      | B | X      |
| 0      | 0 | 1      |
| 0      | 1 | 1      |
| 1      | 0 | 1      |
| 1      | 1 | 0      |

**NOR Gate**

The term NOR is a contraction of NOT-OR and implies an OR function with an inverted (complemented) output. For a 2-input NOR gate, output X is LOW when either input A or input B is HIGH, or when both A and B are HIGH; X is HIGH only when both A and B are LOW.

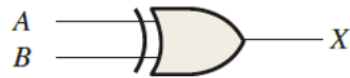


| Inputs |   | Output |
|--------|---|--------|
| A      | B | X      |
| 0      | 0 | 1      |
| 0      | 1 | 0      |

|   |   |   |
|---|---|---|
| 1 | 0 | 0 |
| 1 | 1 | 0 |

### Exclusive OR Gate (X-OR gate)

For an exclusive-OR gate, output  $X$  is HIGH when input  $A$  is LOW and input  $B$  is HIGH, or when input  $A$  is HIGH and input  $B$  is LOW;  $X$  is LOW when  $A$  and  $B$  are both HIGH or both LOW.



| Inputs |   | Output |
|--------|---|--------|
| A      | B | X      |
| 0      | 0 | 0      |
| 0      | 1 | 1      |
| 1      | 0 | 1      |
| 1      | 1 | 0      |

### Procedure:

1.
  - a) Find the pin diagram for the 7400 IC (pin diagram has been provided). Configure the breadboard according to Figure 1. Apply  $V_{cc}$  and ground to the appropriate pins (Connect pin 7 to ground (0V) and pin 14 to  $V_{cc} = +5V$ ).
  - b) You need to connect output pin to a 330-ohm resistor, and the other end of the 330-ohm resistor will be connected to the positive terminal of LED. Finally, the negative terminal of the LED will be connected to ground (0V). If the output is logic 1, LED will turn ON and if the output is logic 0, LED will turn OFF.
  - c) Test NAND gate by connecting all possible combinations of inputs, as listed in Table 1 of the report. Apply a logic 1 by connecting to  $V_{cc}$  and a logic 0 by connecting directly to ground. Use digital multimeter (DMM) to measure the output voltage.
2. Repeat step 1 for NOR gate and X-OR gate. Tabulate your results in Table 2 and Table 3.

Note: The figures, text etc. included here are borrowed from books, websites, author pages and other internet sources such as: [allaboutcircuits.com](http://allaboutcircuits.com), [tutorialspoint.com](http://tutorialspoint.com), [sullystationtechnologies.com](http://sullystationtechnologies.com) for academic purpose only. The author does not claim any originality.

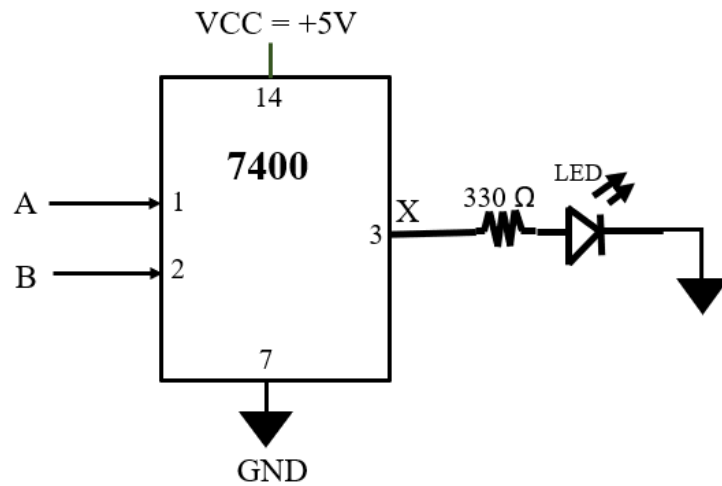


Figure 1. Breadboard connection diagram for NAND

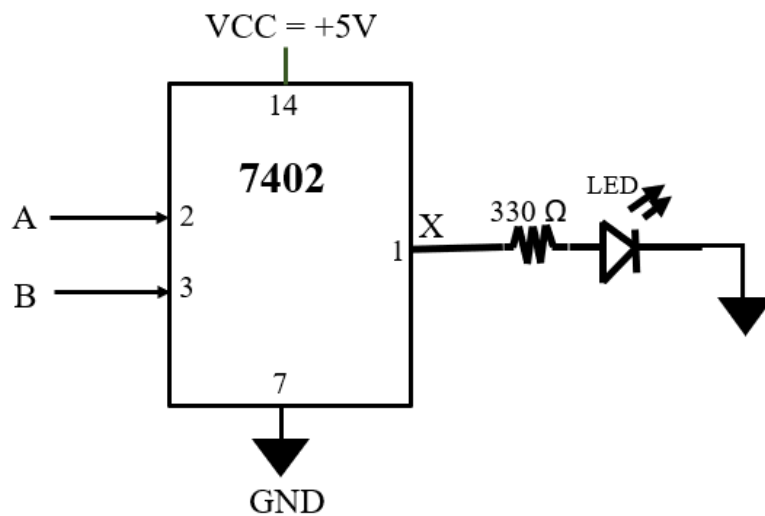


Figure 2. Breadboard connection diagram for NOR

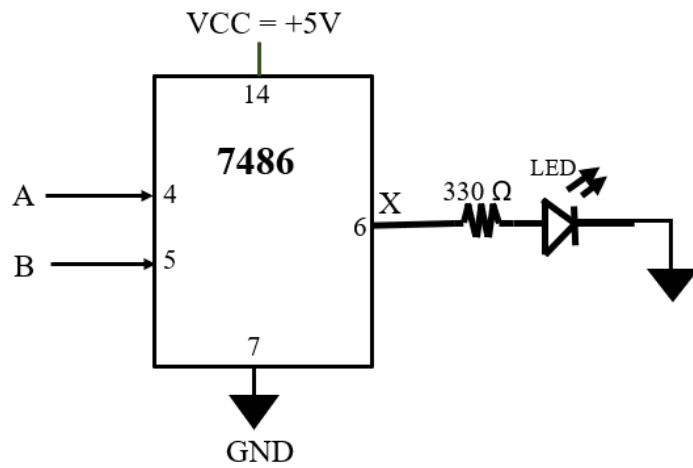


Figure 3. Breadboard connection diagram for Exclusive-OR

## Lab 4 Report

Name:

Data and Observations:

Table 1 NAND Gate

| Inputs |   | Output | Measured<br>Output<br>voltage |
|--------|---|--------|-------------------------------|
| A      | B | X      |                               |
| 0      | 0 |        |                               |
| 0      | 1 |        |                               |
| 1      | 0 |        |                               |
| 1      | 1 |        |                               |

Table 2 NOR Gate

| Inputs |   | Output | Measured<br>Output<br>voltage |
|--------|---|--------|-------------------------------|
| A      | B | X      |                               |
| 0      | 0 |        |                               |
| 0      | 1 |        |                               |
| 1      | 0 |        |                               |
| 1      | 1 |        |                               |

Table 3 X-OR Gate

| Inputs |   | Output | Measured<br>Output<br>voltage |
|--------|---|--------|-------------------------------|
| A      | B | X      |                               |
| 0      | 0 |        |                               |
| 0      | 1 |        |                               |
| 1      | 0 |        |                               |
| 1      | 1 |        |                               |

### Submission Process

You do not need to submit tutorial or procedure. You just need to submit lab 4 report and screenshot of the circuit.

I would suggest you create a folder and name it as lab4 and copy your lab 4 report and screenshots. Then you will zip the Lab4 folder. Finally, upload the zipped Lab4 folder on the Canvas.