

Loop	ALU	ALU	ALU	ALU	MEM	MEM	MEM	MEM	Clock cycle
					ldr w6, [x2]	ldr w6, [x2, #4]	ldr w6, [x2, #8]	ldr w6, [x2, #12]	1
	add w1, w1, w6	add w4, w4, w6	add w3, w3, w6	add w0, w0, w6					2
	add x2, x2, #0x10								3
	cmp x2, x5								4
	bne Loop								5

The diagram illustrates the execution of a loop over five clock cycles. The first cycle (Cycle 1) contains four memory load instructions: `ldr w6, [x2]`, `ldr w6, [x2, #4]`, `ldr w6, [x2, #8]`, and `ldr w6, [x2, #12]`. The second cycle (Cycle 2) contains four ALU add instructions: `add w1, w1, w6`, `add w4, w4, w6`, `add w3, w3, w6`, and `add w0, w0, w6`. The third cycle (Cycle 3) contains one ALU instruction: `add x2, x2, #0x10`. The fourth cycle (Cycle 4) contains one ALU instruction: `cmp x2, x5`. The fifth cycle (Cycle 5) contains one ALU instruction: `bne Loop`. Arrows indicate data flow: a green arrow from the ALU of Cycle 1 to the ALU of Cycle 2; a red arrow from the MEM of Cycle 1 to the ALU of Cycle 2; a cyan arrow from the MEM of Cycle 1 to the ALU of Cycle 2; and a blue arrow from the MEM of Cycle 1 to the ALU of Cycle 2.