Lab Session 3
Using NC-Verilog & Verdi

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Date:2020/02/24

Outline

1. Introduction
2. Creating/Editing Verilog Source Code
3. Compiling & Simulating using NC-Verilog
4. Viewing Waveform using Verdi

Introduction (1/2)

□ NC-Verilog是Cadence公司發展的HDL Simulator tool。

□ HDL為Hardware Description Language的簡寫，顧名思義即為描述硬體的語言。

□ 主要功能:

- ➔ 檢查HDL code語法有沒有問題。
- ➔ 對HDL code模擬出真實電路的行為，同時可以產生波形以利確認與驗證電路。
- ➔ 支援Behavioral、RTL、Gate-level等階層的co-simulation。

Introduction (2/2)

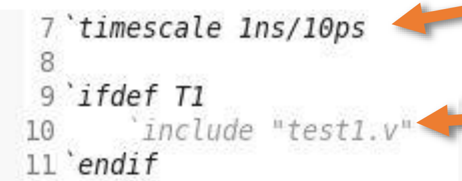
- Debussy是Spring Software公司發展的HDL Debug & Analysis tool . 現在改名為Verdi.
- 它強大的功能在：能在HDL source code、 schematic diagram、 waveform、state bubble diagram做即時的trace.
- Debussy本身沒有模擬器，所以要透過外部來模擬(如NcVerilog, VCS, ModelSim).

Copy & opening example files

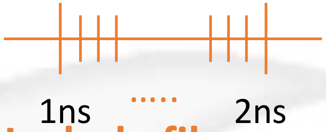
In SOC:
01~30: vlsicad6
31~60: vlsicad8
61~ : vlsicad9
In Computer classroom A
140.116.156.6/8/10

- File location :
  - Download Lab1.tar from moodle.
- Step : Key in the following command at your personal directory.
  - Open Xming
  - Login your account with Putty.
  - Change your password.(CMD:passwd)
  - Create a Lab2 directory.(CMD:mkdir Lab2)
  - Upload Lab2.tar to your Lab2 directory with FileZilla.
  - cd Lab2
  - Decompress Lab2.tar to original directory.(CMD:tar –xvf Lab2.tar)
  - ls (there should be 3 .v files(test1.v,test2.v,test_tb.v)!!)
  - CMD:gedit (filename)

Editing Verilog Source Code

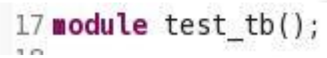


```
`timescale 1ns/10ps

`ifdef T1
    `include "test1.v"
`endif
```

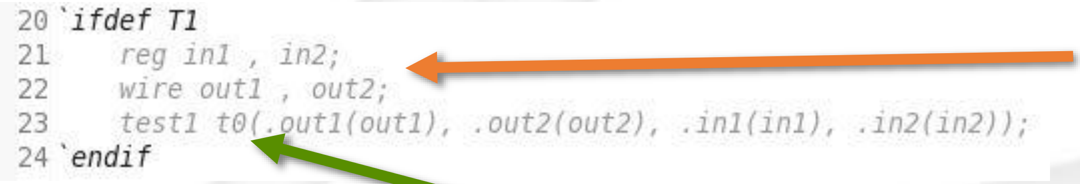


Timescale of the simulation

Include file



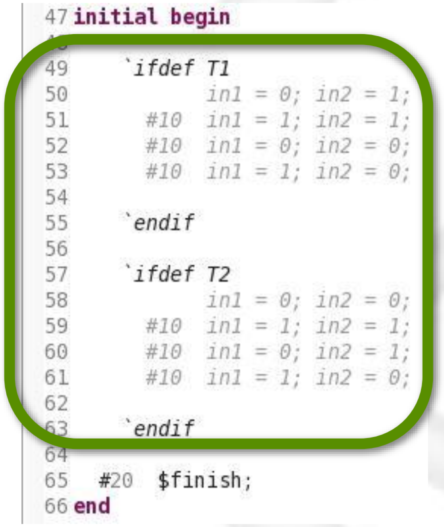
```
module test_tb();
```



```
`ifdef T1
    reg in1 , in2;
    wire out1 , out2;
    test1 t0(.out1(out1), .out2(out2), .in1(in1), .in2(in2));
`endif
```

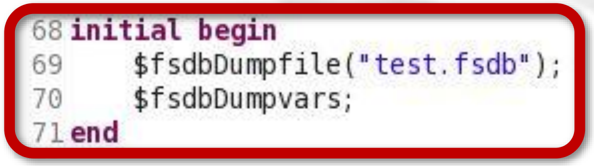
Display inputs & outputs information

Declare module instance name



```
initial begin

    `ifdef T1
            in1 = 0; in2 = 1;
        #10 in1 = 1; in2 = 1;
        #10 in1 = 0; in2 = 0;
        #10 in1 = 1; in2 = 0;

    `endif

    `ifdef T2
            in1 = 0; in2 = 0;
        #10 in1 = 1; in2 = 1;
        #10 in1 = 0; in2 = 1;
        #10 in1 = 1; in2 = 0;

    `endif

  #20  $finish;
end
```

Test Patten Setting:
Input test patterns



```
initial begin
    $fsdbDumpfile("test.fsdb");
    $fsdbDumpvars;
end
```

Simulation Env. Setting:
Create a waveform file .fsdb

Compiling & Simulating Using NC-Verilog(1/4)

□ To compile & simulate the verilog code:

Just Compile the test1.v

```
>ncverilog   test1.v
```

Compile & simulate the test1.v & test_tb.v

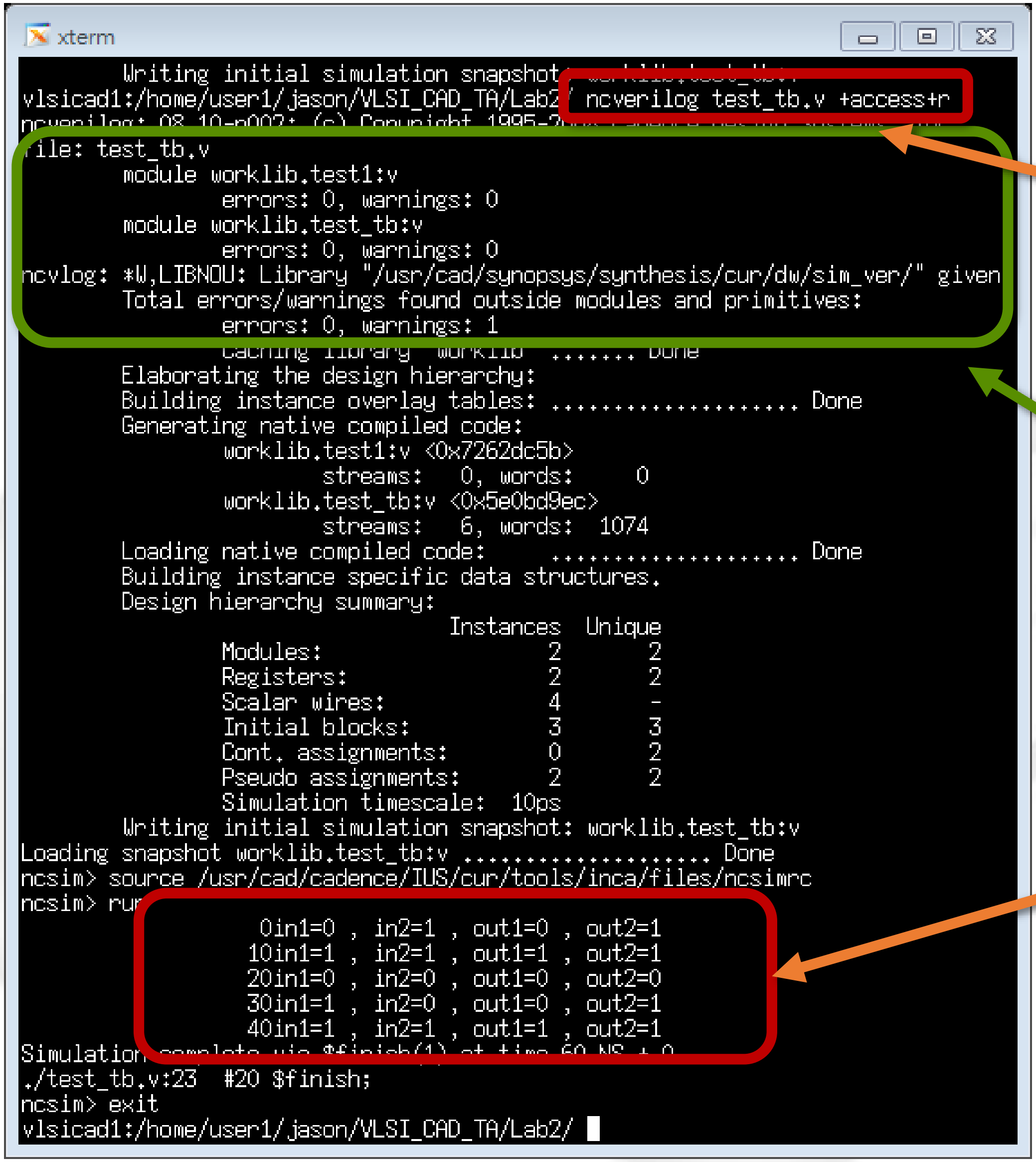
```
>ncverilog   test_tb.v     +define+T1+FSDB     +access+r
```

Dump .fsdb file

Compile & simulate the test2.v & test_tb.v

```
>ncverilog   test_tb.v     +define+T2+FSDB     +access+r
```

Compiling & Simulating Using NC-Verilog(2/4)



```
        Writing initial simulation snapshot: worklib.test_tb:v
vlsicad1:/home/user1/jason/VLSI_CAD_TA/Lab2/ ncverilog test_tb.v +access+r
ncverilog: 08.10-p002: (c) Copyright 1995-2
file: test_tb.v
        module worklib.test1:v
                errors: 0, warnings: 0
        module worklib.test_tb:v
                errors: 0, warnings: 0
ncvlog: *W,LIBNOU: Library "/usr/cad/synopsys/synthesis/cur/dw/sim_ver/" given
        Total errors/warnings found outside modules and primitives:
                errors: 0, warnings: 1
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.test1:v <0x7262dc5b>
                        streams:   0, words:     0
                worklib.test_tb:v <0x5e0bd9ec>
                        streams:   6, words:  1074
        Loading native compiled code:     .................... Done
        Building instance specific data structures.
        Design hierarchy summary:
                          Instances  Unique
                Modules:          2       2
                Registers:        2       2
                Scalar wires:     4       -
                Initial blocks:   3       3
                Cont. assignments: 0      2
                Pseudo assignments: 2     2
                Simulation timescale:  10ps
        Writing initial simulation snapshot: worklib.test_tb:v
Loading snapshot worklib.test_tb:v .................... Done
ncsim> source /usr/cad/cadence/IUS/cur/tools/inca/files/ncsimrc
ncsim> run
                  0in1=0 , in2=1 , out1=0 , out2=1
                 10in1=1 , in2=1 , out1=1 , out2=1
                 20in1=0 , in2=0 , out1=0 , out2=0
                 30in1=1 , in2=0 , out1=0 , out2=1
                 40in1=1 , in2=1 , out1=1 , out2=1
Simulation complete via $finish(1) at time 60 NS + 0
./test_tb.v:23  #20 $finish;
ncsim> exit
vlsicad1:/home/user1/jason/VLSI_CAD_TA/Lab2/ █
```

Command

Compiling results & error messages

Simulation results

Compiling & Simulating Using NC-Verilog(3/4)

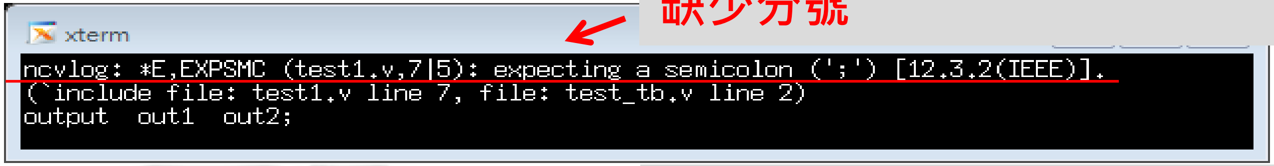
- Three NC-Verilog message levels
  - *Warning message - indicate that there may be something wrong with the model and continue to run*
  - *Error message - indicate that a user error has occurred at compile time or at run time*
  - Information message - provide information about your source description

Compiling & Simulating Using NC-Verilog(4/4)

- Some common syntax error messages

1.

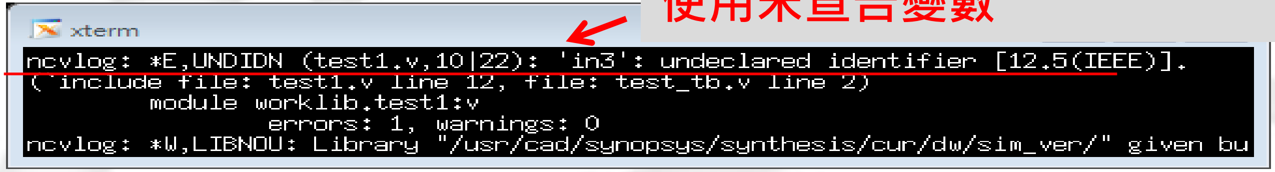
缺少分號



```
ncvlog: *E,EXPSMC (test1.v,7|5): expecting a semicolon (';') [12.3.2(IEEE)].
(`include file: test1.v line 7, file: test_tb.v line 2)
output  out1  out2;
```

2.

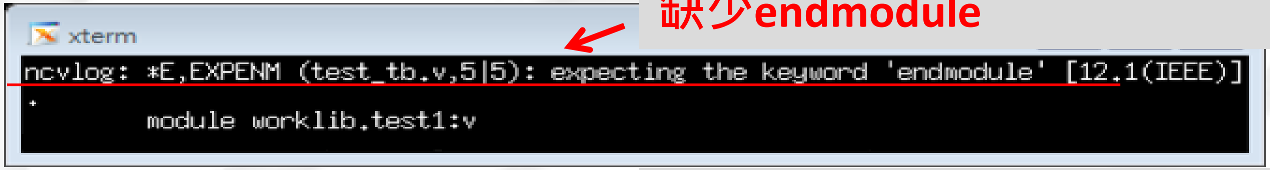
使用未宣告變數



```
ncvlog: *E,UNDIDN (test1.v,10|22): 'in3': undeclared identifier [12.5(IEEE)].
(`include file: test1.v line 12, file: test_tb.v line 2)
        module worklib.test1:v
                errors: 1, warnings: 0
ncvlog: *W,LIBNOU: Library "/usr/cad/synopsys/synthesis/cur/dw/sim_ver/" given bu
```

3.

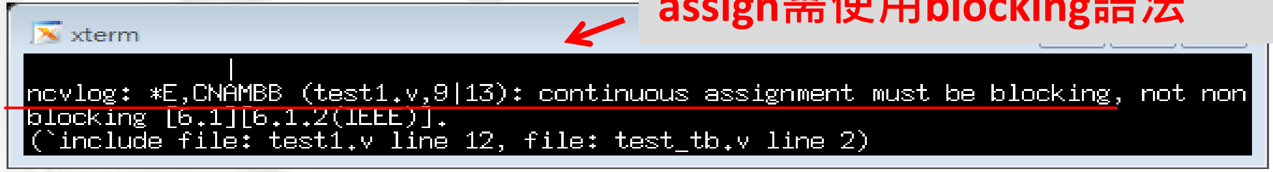
缺少endmodule



```
ncvlog: *E,EXPENM (test_tb.v,5|5): expecting the keyword 'endmodule' [12.1(IEEE)]
.
        module worklib.test1:v
```

4.

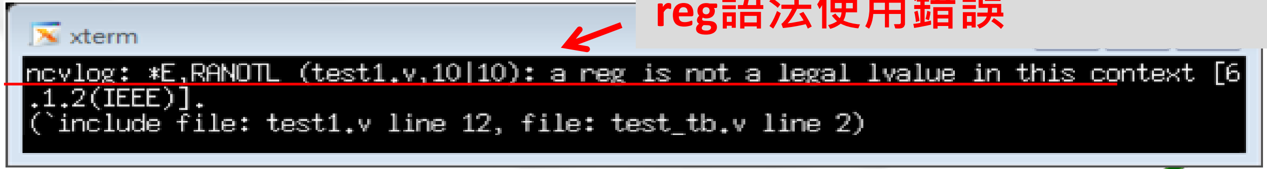
assign需使用blocking語法



```
                      |
ncvlog: *E,CNAMBB (test1.v,9|13): continuous assignment must be blocking, not non
blocking [6.1][6.1.2(IEEE)].
(`include file: test1.v line 12, file: test_tb.v line 2)
```

5.

reg語法使用錯誤



```
ncvlog: *E,RANOTL (test1.v,10|10): a reg is not a legal lvalue in this context [6
.1.2(IEEE)].
(`include file: test1.v line 12, file: test_tb.v line 2)
```

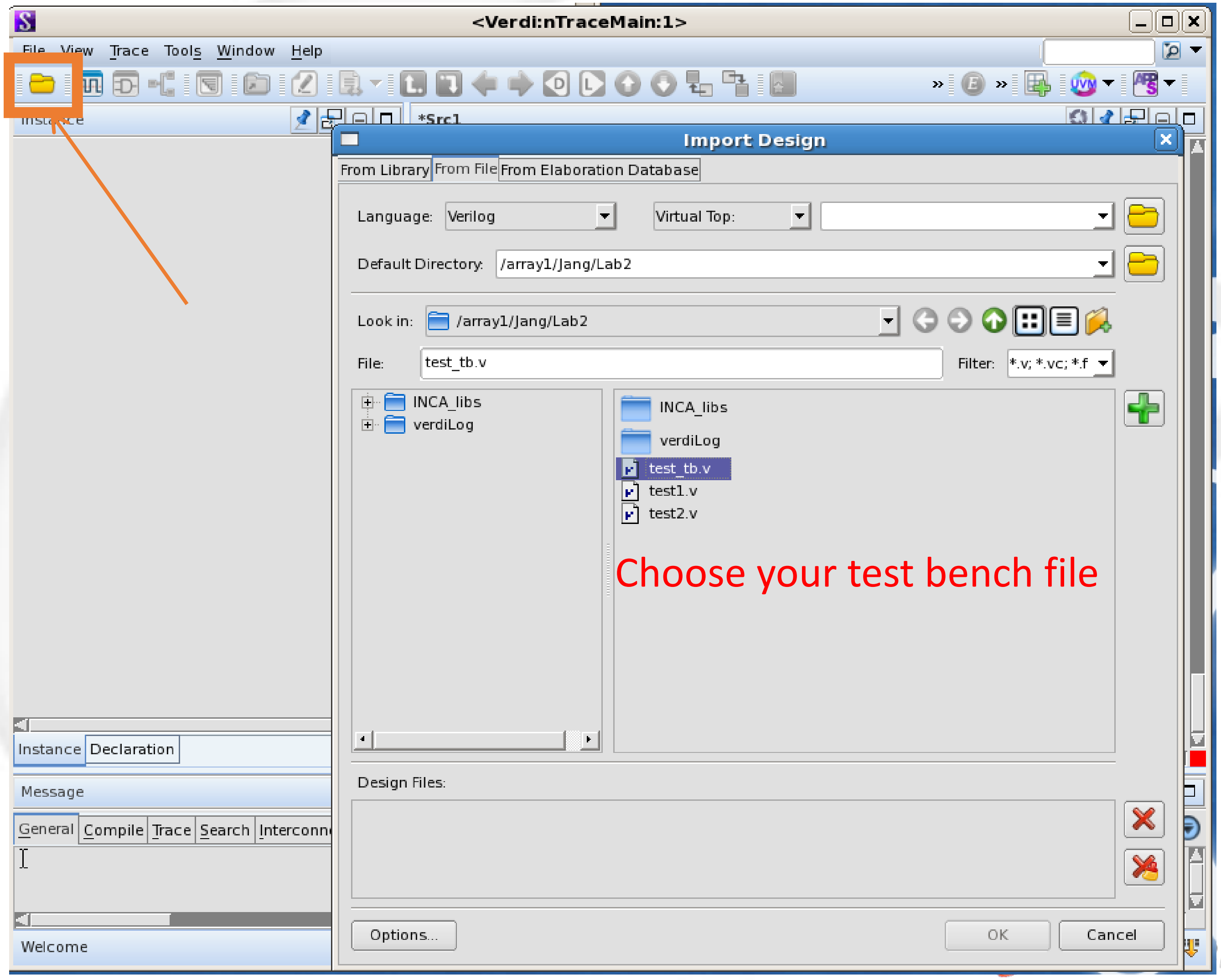
Viewing Waveform using Verdi (0/6)

□ Debussy four components:
nTrace、nWave、nSchema、nState

- nTrace -- Hypertext source code analysis and browse tool (為Debussy &所開啟的主畫面).
- nWave -- Waveform analysis tool (看波形, 可由nTrace內開啟).
- nSchema -- Hierarchy schematic generator (看方塊圖, 可由nTrace內開啟).
- nState -- Finite State Machine Extraction and analysis tool (看FSM流程圖,可由nTrace內開啟).

Viewing Waveform using Verdi (1/6)

啟動： 鍵入verdi &開啟nTrace window如下



Language: Verilog

Virtual Top:

Default Directory: /array1/Jang/Lab2

Look in: /array1/Jang/Lab2

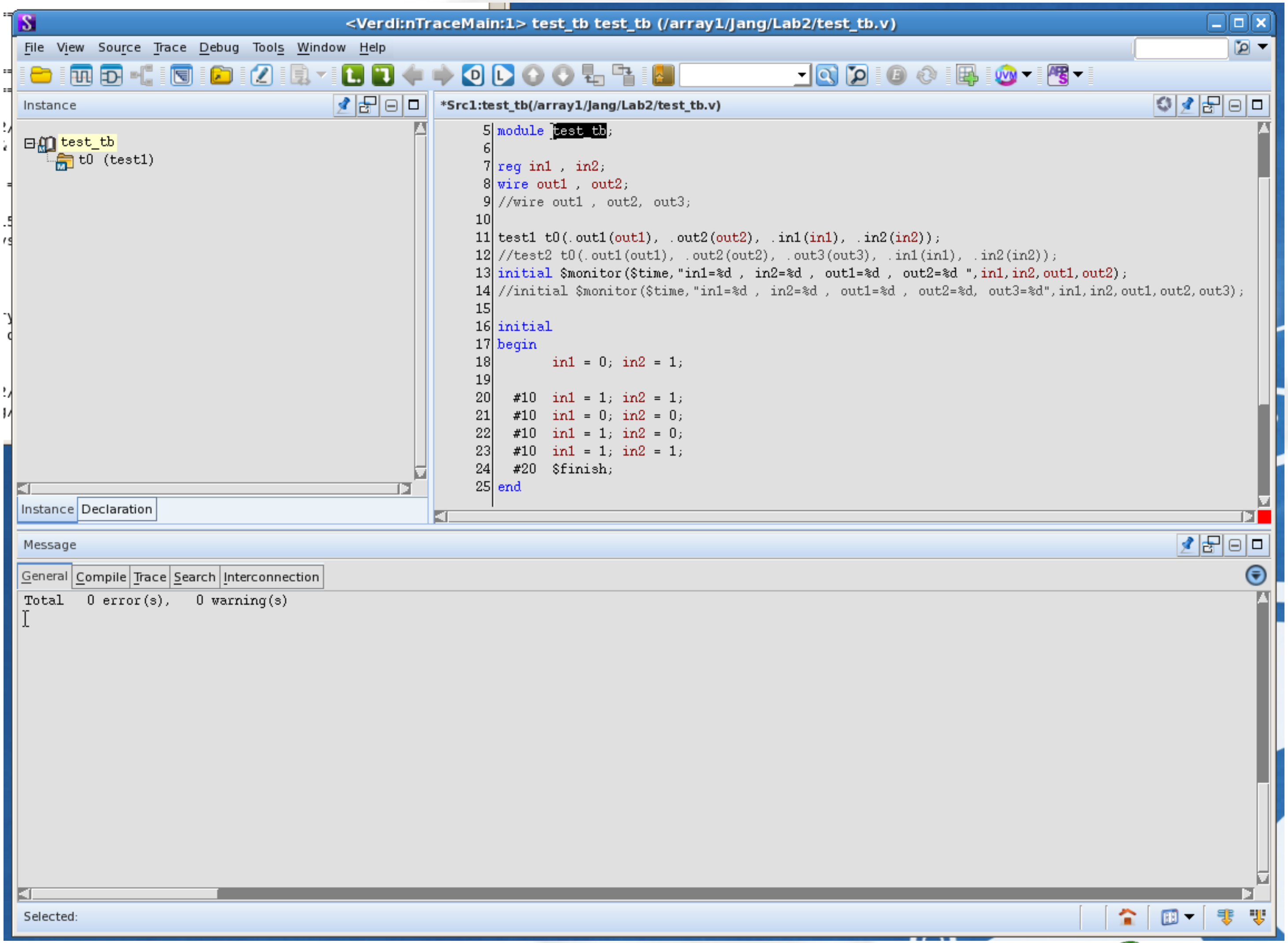
File: test_tb.v

Filter: *.v; *.vc; *.f

Design Files:

Choose your test bench file

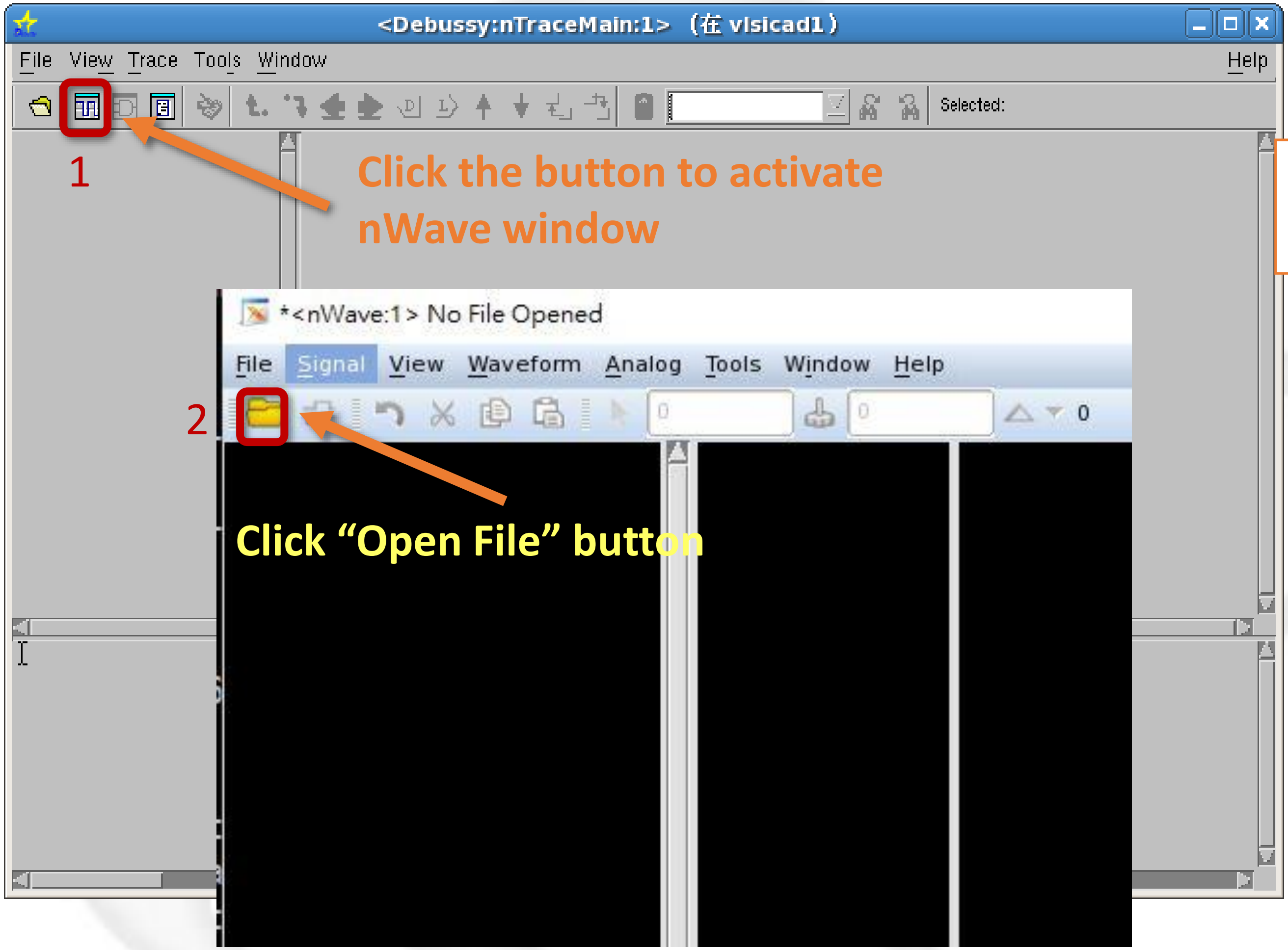
Viewing Waveform using Verdi (2/6)



```
module test_tb;

reg in1 , in2;
wire out1 , out2;
//wire out1 , out2, out3;

test1 t0(.out1(out1), .out2(out2), .in1(in1), .in2(in2));
//test2 t0(.out1(out1), .out2(out2), .out3(out3), .in1(in1), .in2(in2));
initial $monitor($time,"in1=%d , in2=%d , out1=%d , out2=%d ",in1,in2,out1,out2);
//initial $monitor($time,"in1=%d , in2=%d , out1=%d , out2=%d, out3=%d",in1,in2,out1,out2,out3);

initial
begin
        in1 = 0; in2 = 1;

  #10  in1 = 1; in2 = 1;
  #10  in1 = 0; in2 = 0;
  #10  in1 = 1; in2 = 0;
  #10  in1 = 1; in2 = 1;
  #20  $finish;
end
```

```
Total   0 error(s),    0 warning(s)
```

Viewing Waveform using Verdi (3/6)

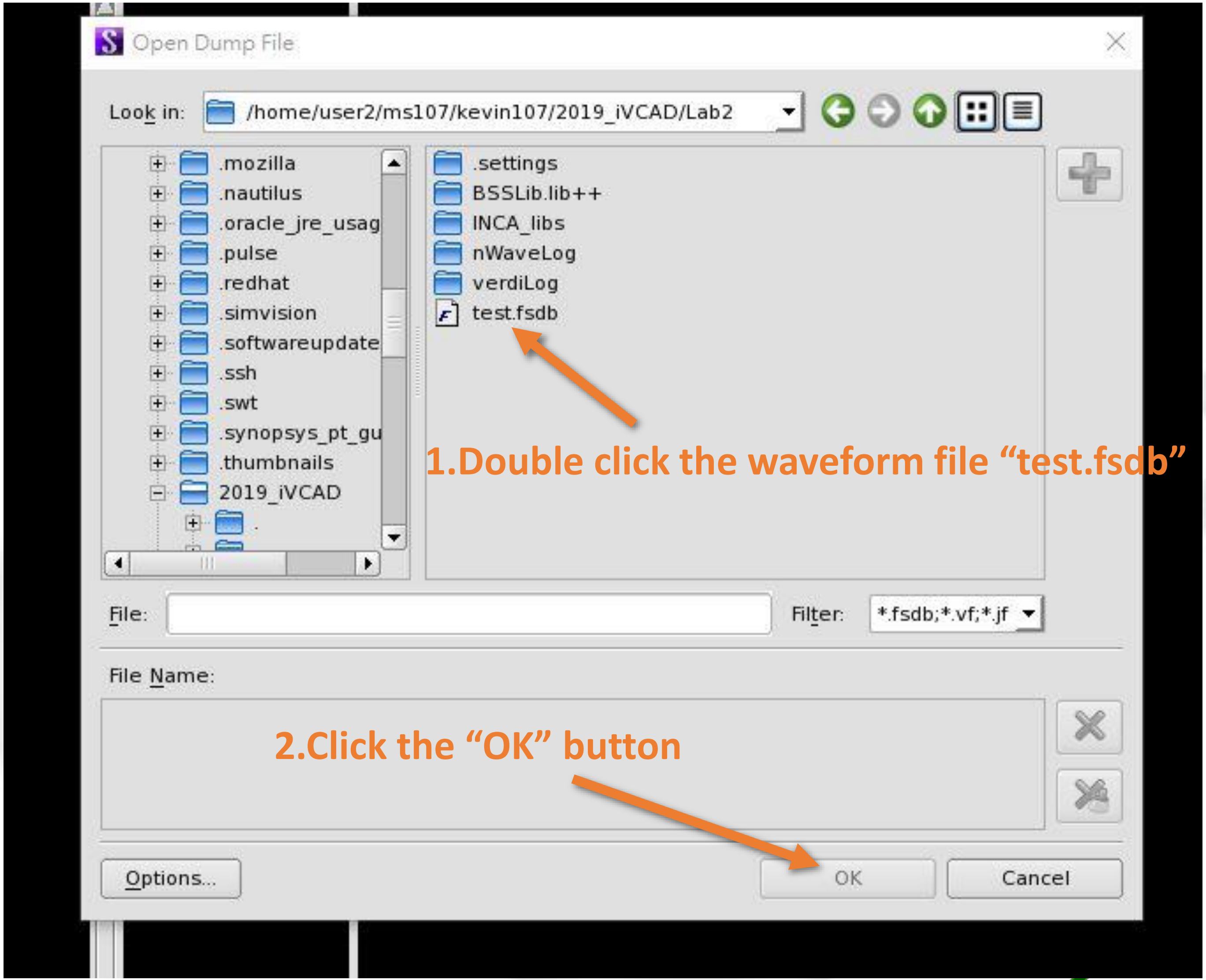

<Debussy:nTraceMain:1> (在 vlsicad1)
File View Trace Tools Window Help
Selected:
1
*<nWave:1> No File Opened
File Signal View Waveform Analog Tools Window Help
2

Click the button to activate nWave window

Click "Open File" button

OR:
CMD:nWave &

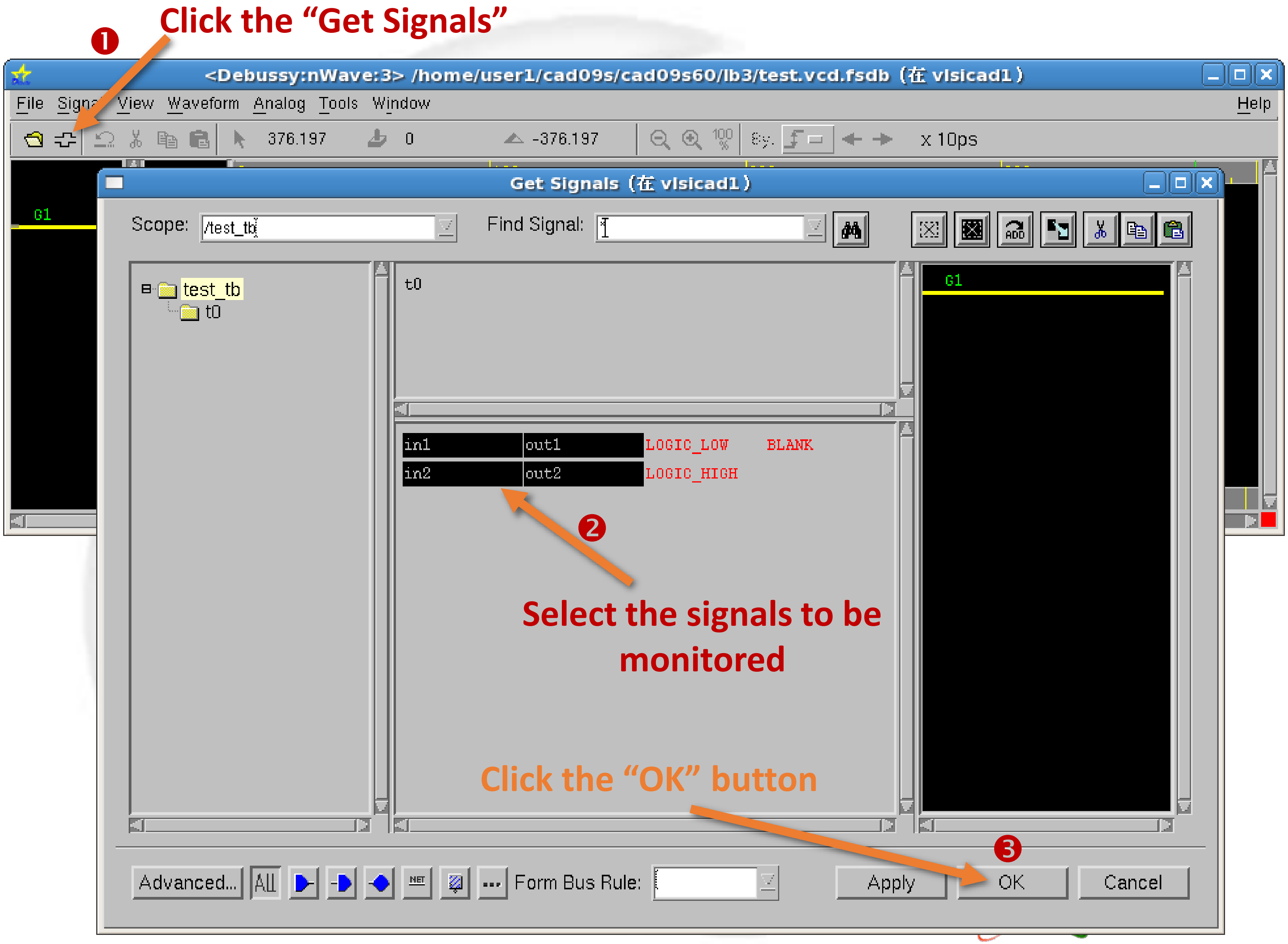
Viewing Waveform using Verdi (4/6)



1.Double click the waveform file “test.fsdb”

2.Click the “OK” button

Viewing Waveform using Verdi (5/6)



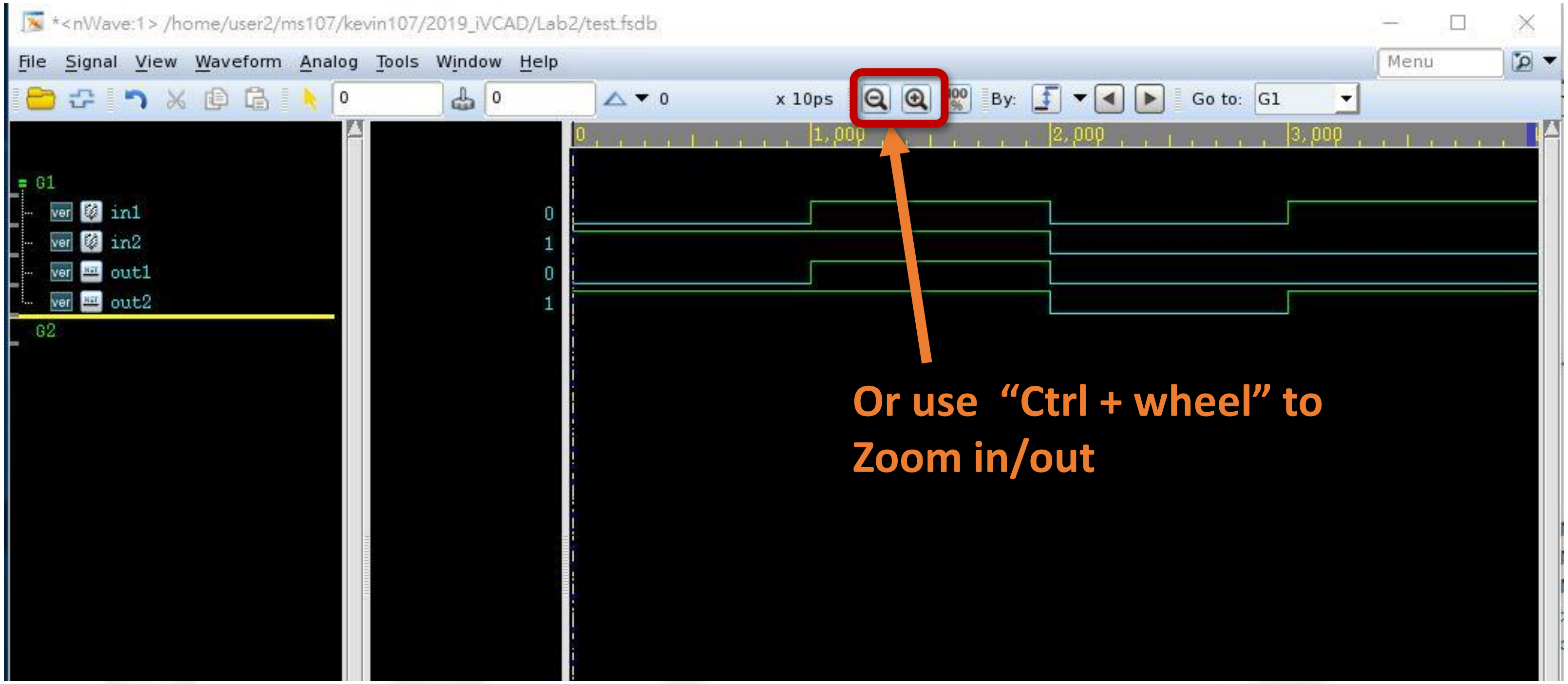
❶ Click the “Get Signals”

❷ Select the signals to be monitored

❸ Click the “OK” button

<Debussy:nWave:3> /home/user1/cad09s/cad09s60/lb3/test.vcd.fsdb (在 vlsicad1)
File Signal View Waveform Analog Tools Window Help
376.197 0 -376.197 x 10ps
G1
Get Signals (在 vlsicad1)
Scope: /test_tb
Find Signal:
test_tb
t0
t0
in1 out1 LOGIC_LOW BLANK
in2 out2 LOGIC_HIGH
G1
Advanced... All Form Bus Rule: Apply OK Cancel

Viewing Waveform using Verdi (6/6)

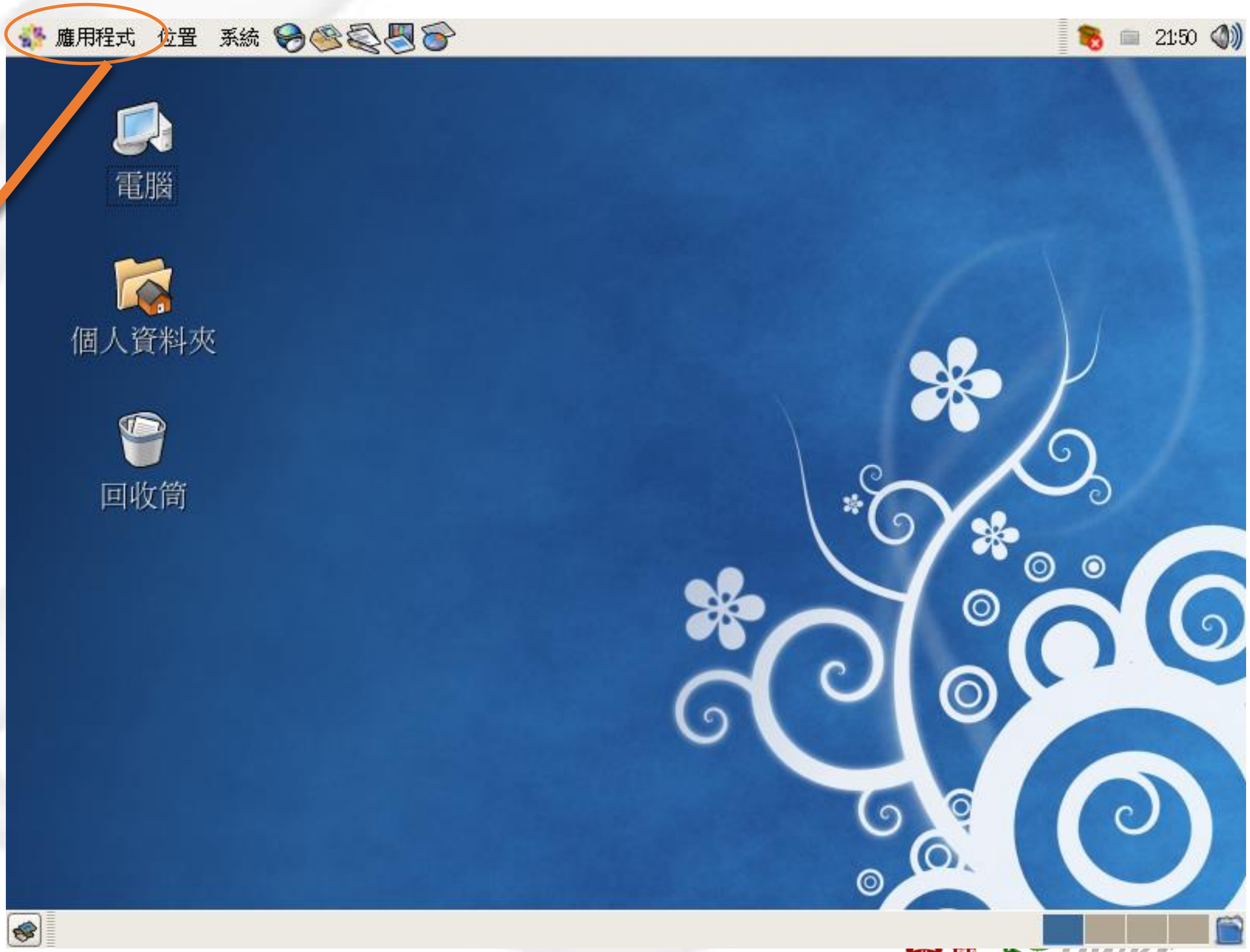

*<nWave:1> /home/user2/ms107/kevin107/2019_iVCAD/Lab2/test.fsdb
File Signal View Waveform Analog Tools Window Help
Menu
x 10ps
By:
Go to: G1
0
1,000
2,000
3,000
G1
in1
in2
out1
out2
G2
0
1
0
1

Or use “Ctrl + wheel” to Zoom in/out

in1	0	1	0	1
in2	1	1	0	0
out1	0	1	0	0
out2	1	1	0	1

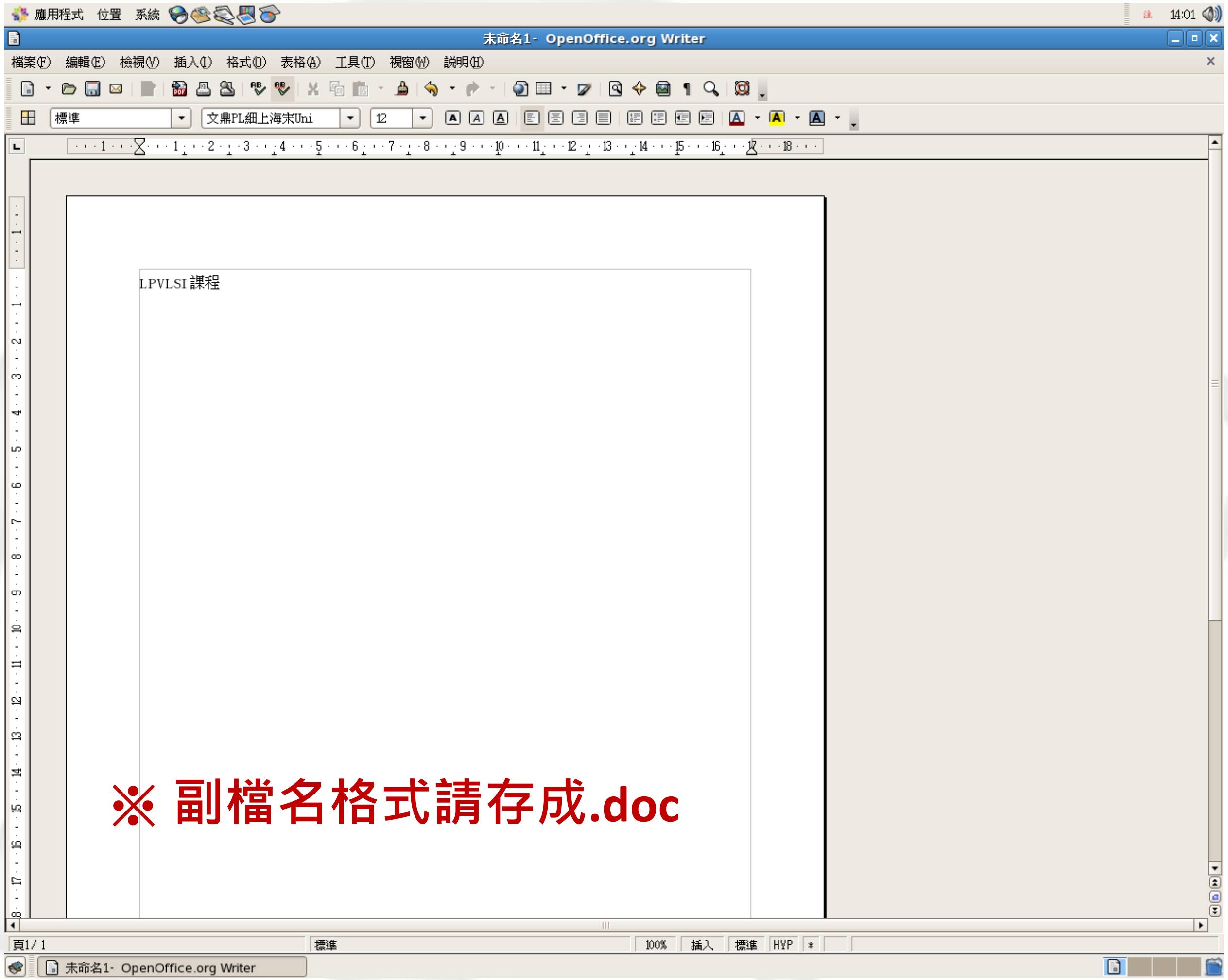
Libre writer(1)

- Libre writer類似windows的office word，同學打報告時可使用本程式。(新電腦請從應用程式裡找Office)



點下

Libre writer(2)


應用程式 位置 系統
14:01
未命名1 - OpenOffice.org Writer
檔案(F) 編輯(E) 檢視(V) 插入(I) 格式(O) 表格(A) 工具(T) 視窗(W) 說明(H)
標準
文鼎PL細上海宋Uni
12
頁1 / 1
標準
100%
插入
標準
HYP
*
未命名1 - OpenOffice.org Writer

LPVLSI 課程

※ 副檔名格式請存成.doc

Lab1 mini lab:

1. 改用test2.v並以NC-Verilog進行模擬.
2. 將test2.v的error全部修正完畢.
3. 利用nWave看結果波形.

Thank you for your attention!!