



# Lab Session 4 Synthesis

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Date: 2021/03/17



# Outline

- Introduction
- Synthesis flow
- Appendix



# Introduction



# Introduction

- ❑ Three levels of design and the information that we can get
  - ➔ RTL Design & Simulation
    - ◆ Logical operations on signals
  - ➔ Synthesis
    - ◆ Wiring (without placing and routing information), timing
  - ➔ Layout
    - ◆ Place and route, timing(clock tree synthesis)
- ❑ We **transform the RTL code into the gate-level code**, so we know how the design is implemented with those cells.
- ❑ To make the simulation more realistic, we **use cells that contains timing information**.

# Introduction

## ❑ Tool : Design Compiler

- ➔ Company : Synopsys
- ➔ Version : 2018.06

## ❑ Before synthesis, you need to prepare...

- ➔ Your RTL code
- ➔ tsmc13\_neg.v
- ➔ [synopsys\\_dc.setup](#)

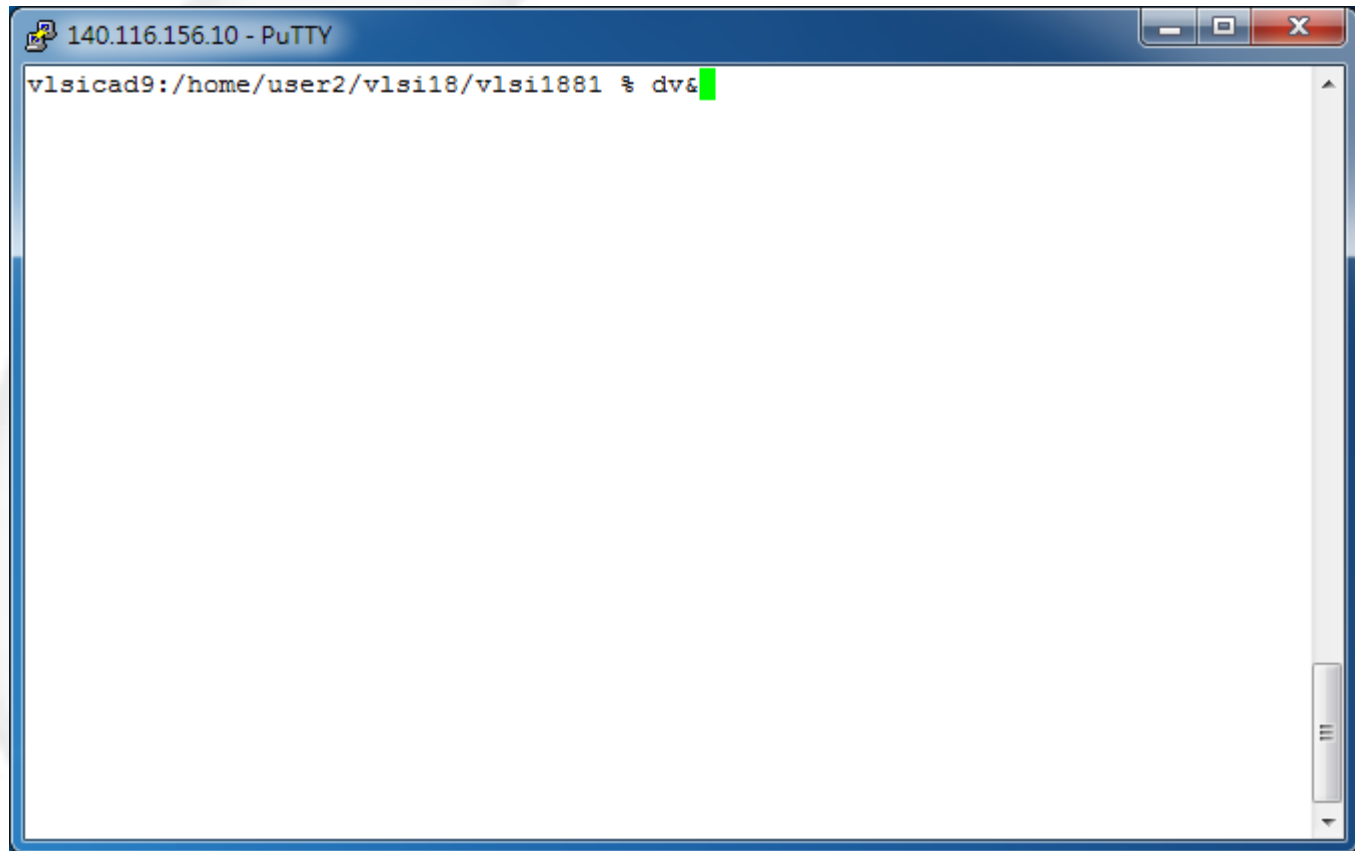
# Synthesis flow

# Synthesis flow

- ❑ Setup library
- ❑ Read file
- ❑ Define clock specification
- ❑ Define operating environment
- ❑ Compile
- ❑ Report & Analysis
- ❑ Save design

# Design Compiler

- ❑ In the terminal, Enter dv.

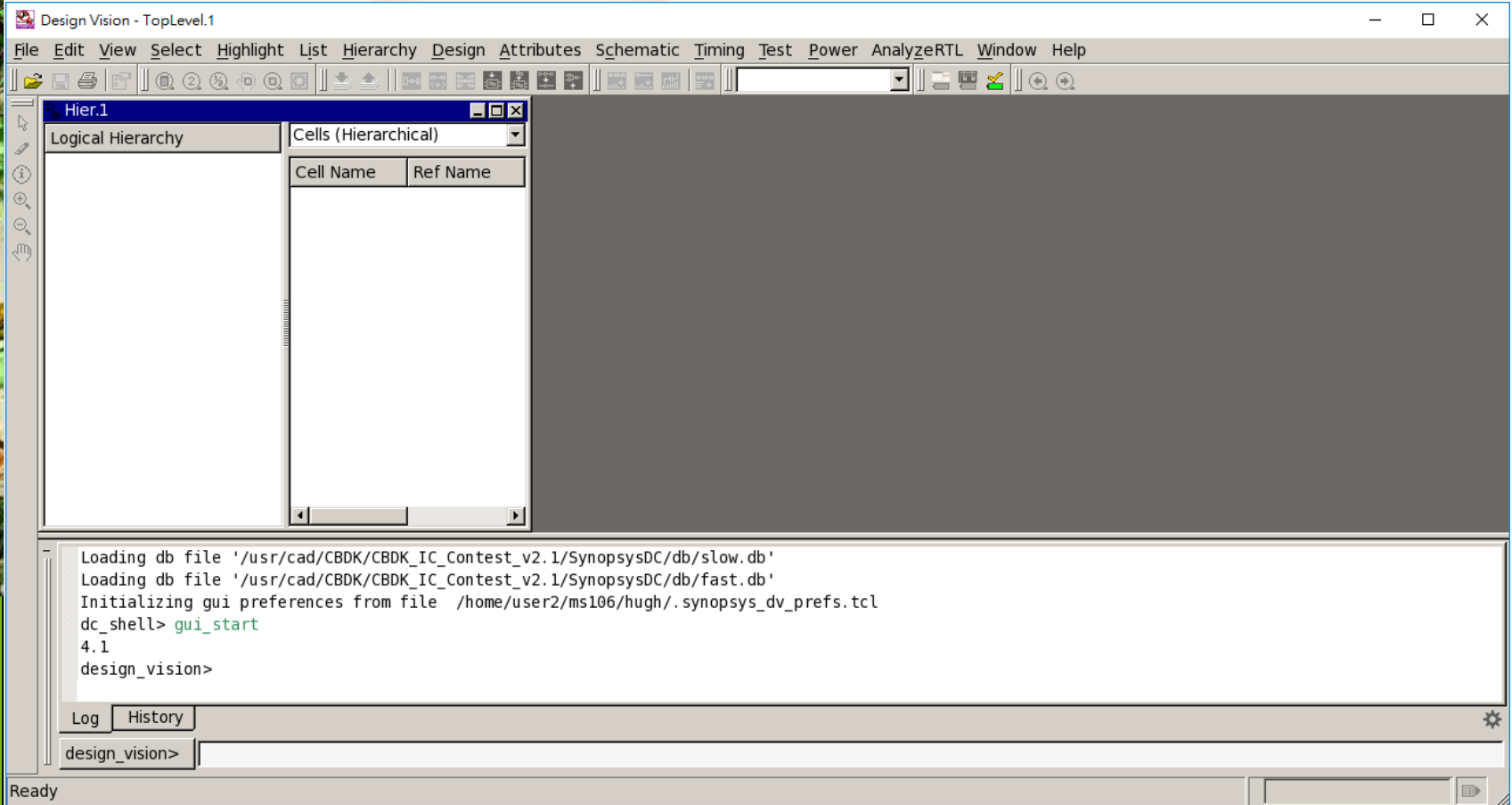


A screenshot of a PuTTY terminal window. The title bar reads "140.116.156.10 - PuTTY". The terminal text shows the prompt "vlsicad9:/home/user2/vlsi18/vlsi1881 % dv&" with a green cursor at the end of the command. The terminal window has a blue border and standard window controls (minimize, maximize, close) in the top right corner.

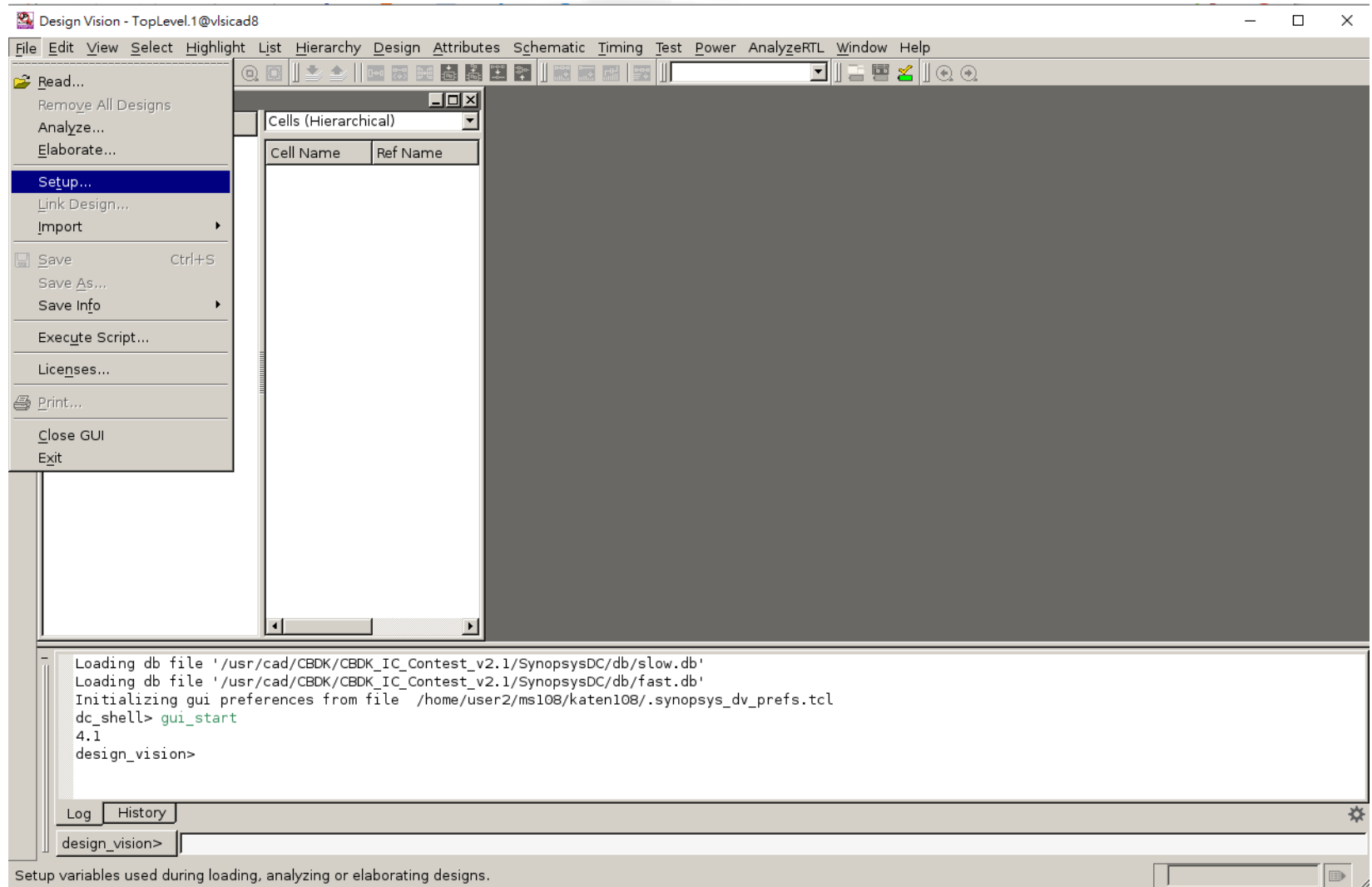


# Open DC

- ❑ Check if there is any error.

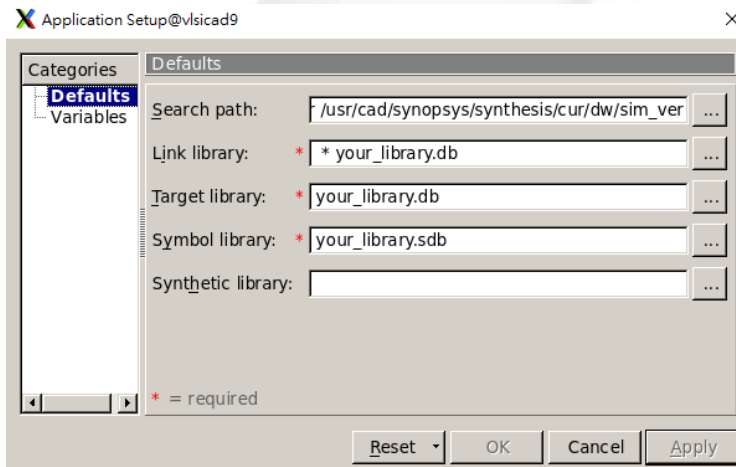


# Check library

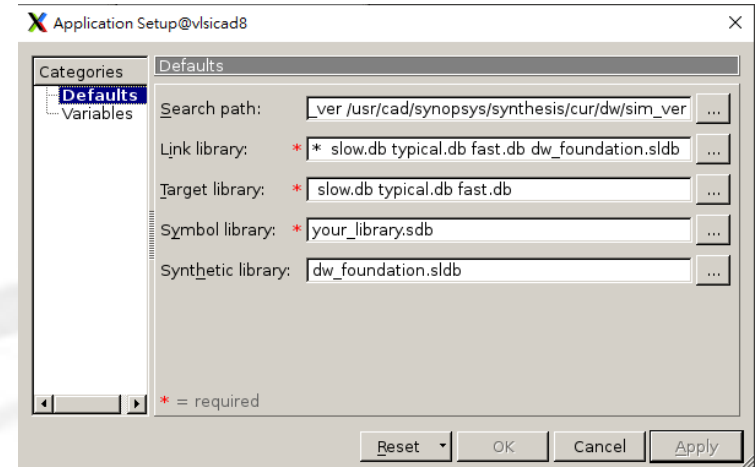


# Check library

- Check whether library setup correctly



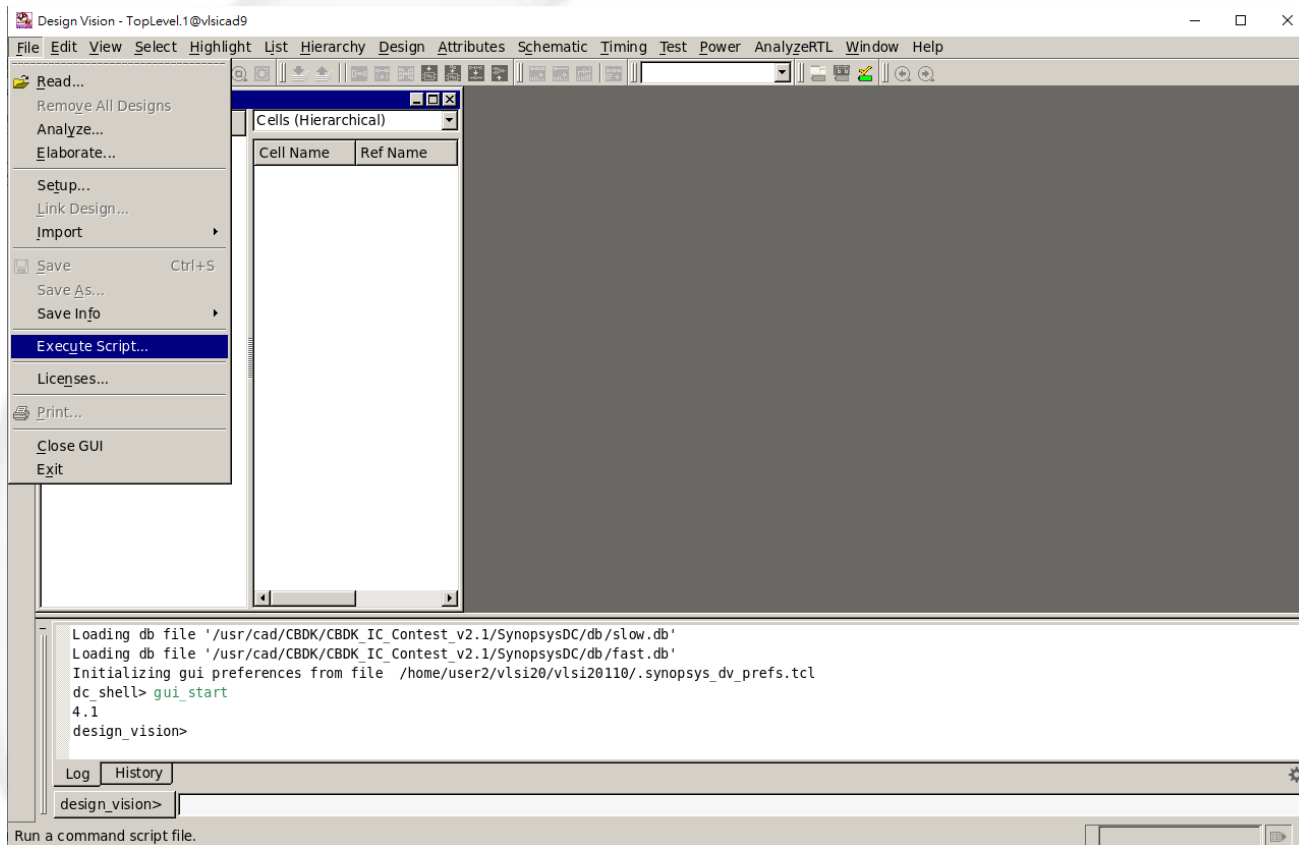
fail



success

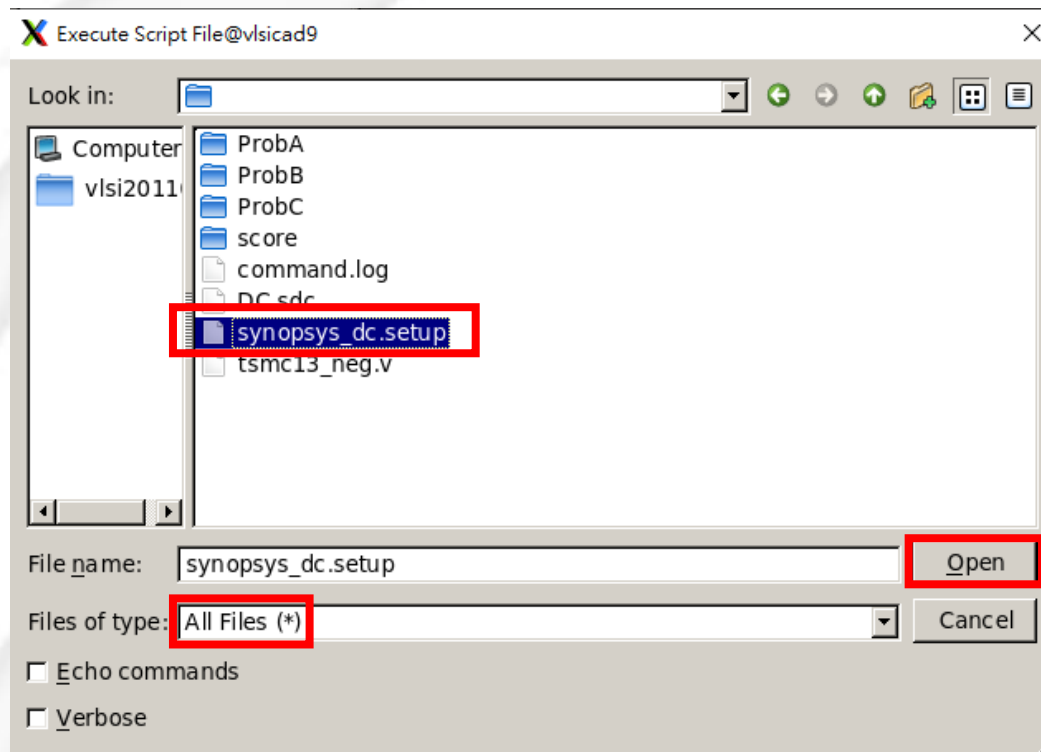
# Check library

- ❑ If fail, read dc setup file



# Check library

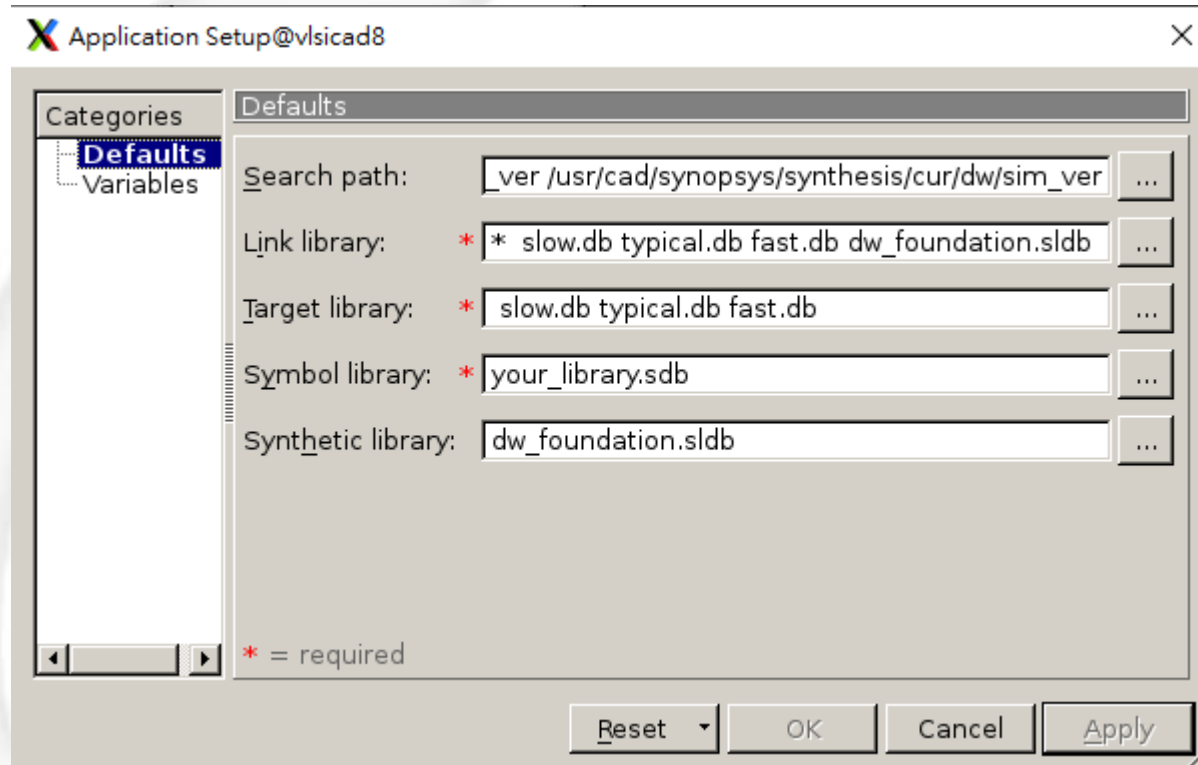
- ❑ If fail, read dc setup file





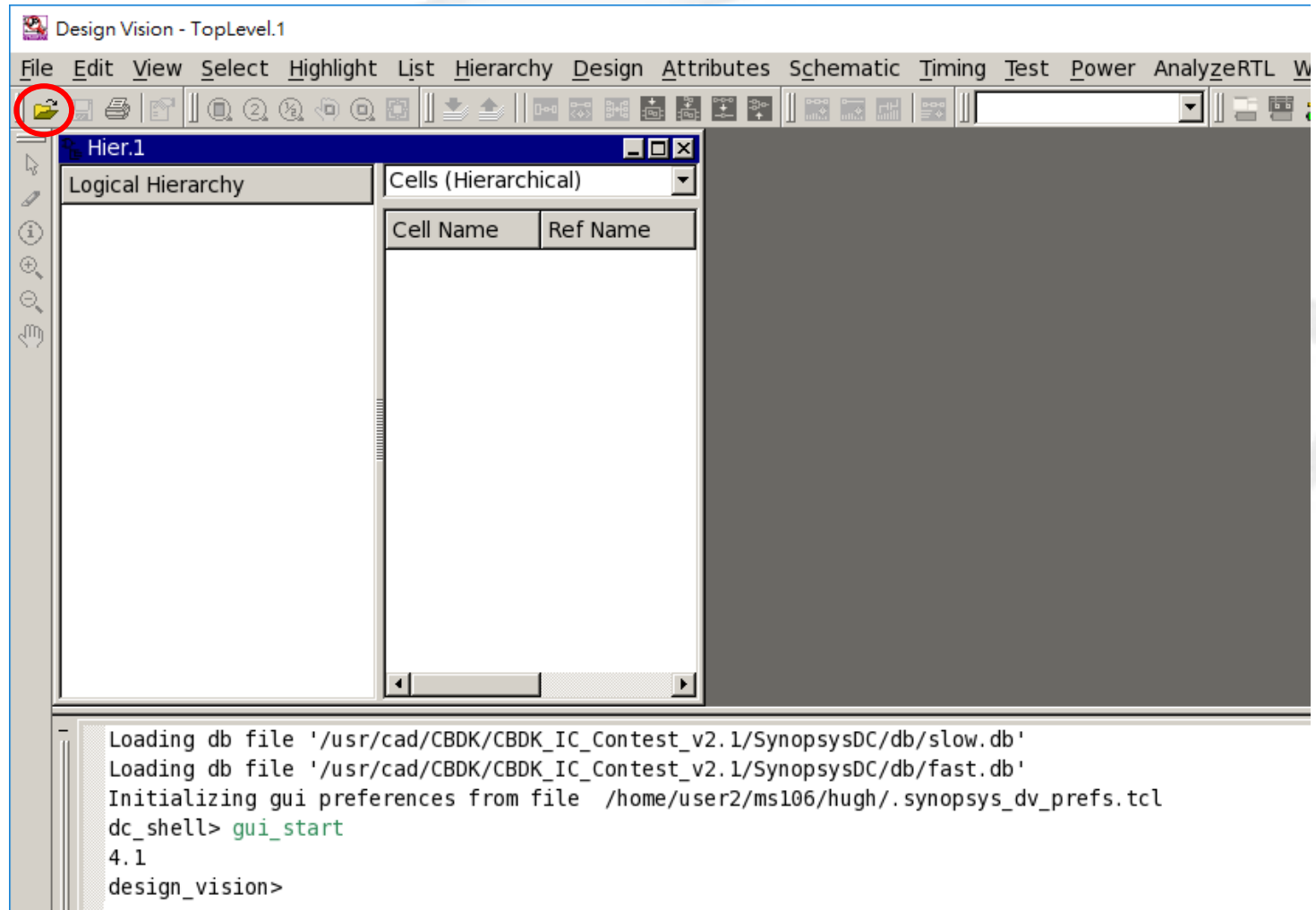
# Check library

## □ Check library again



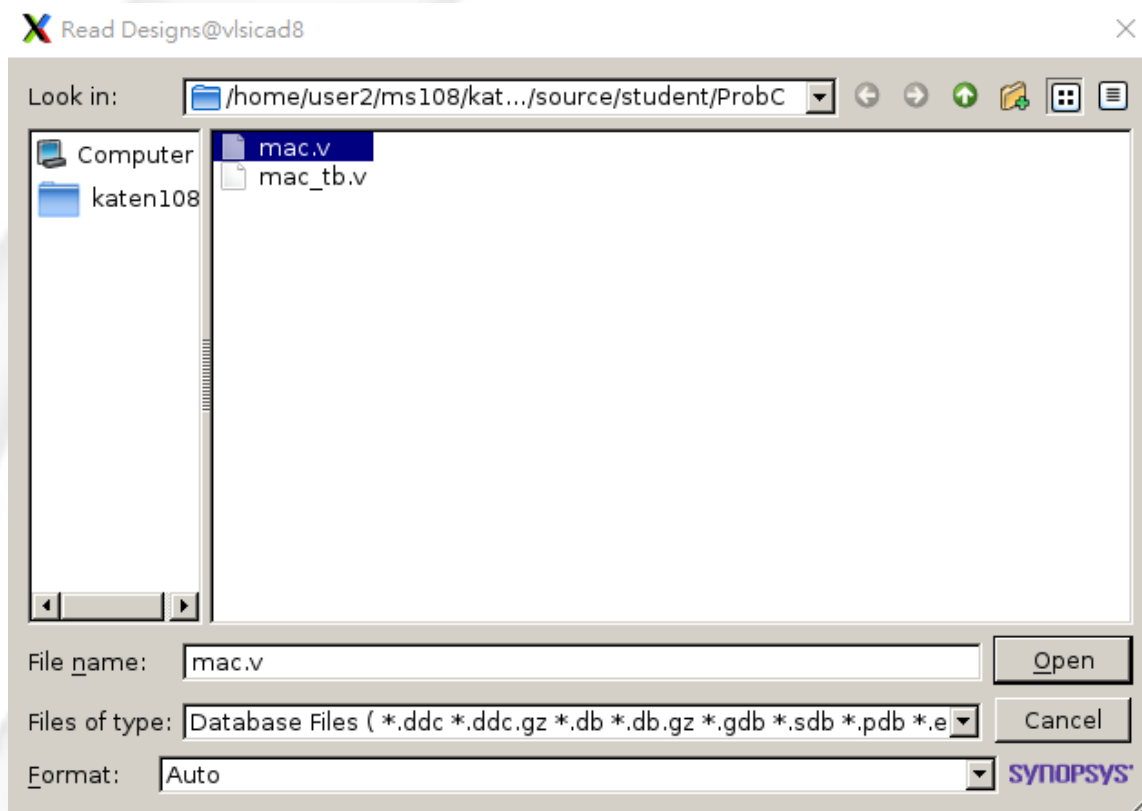
# Read Files (1)

## File >> Read...



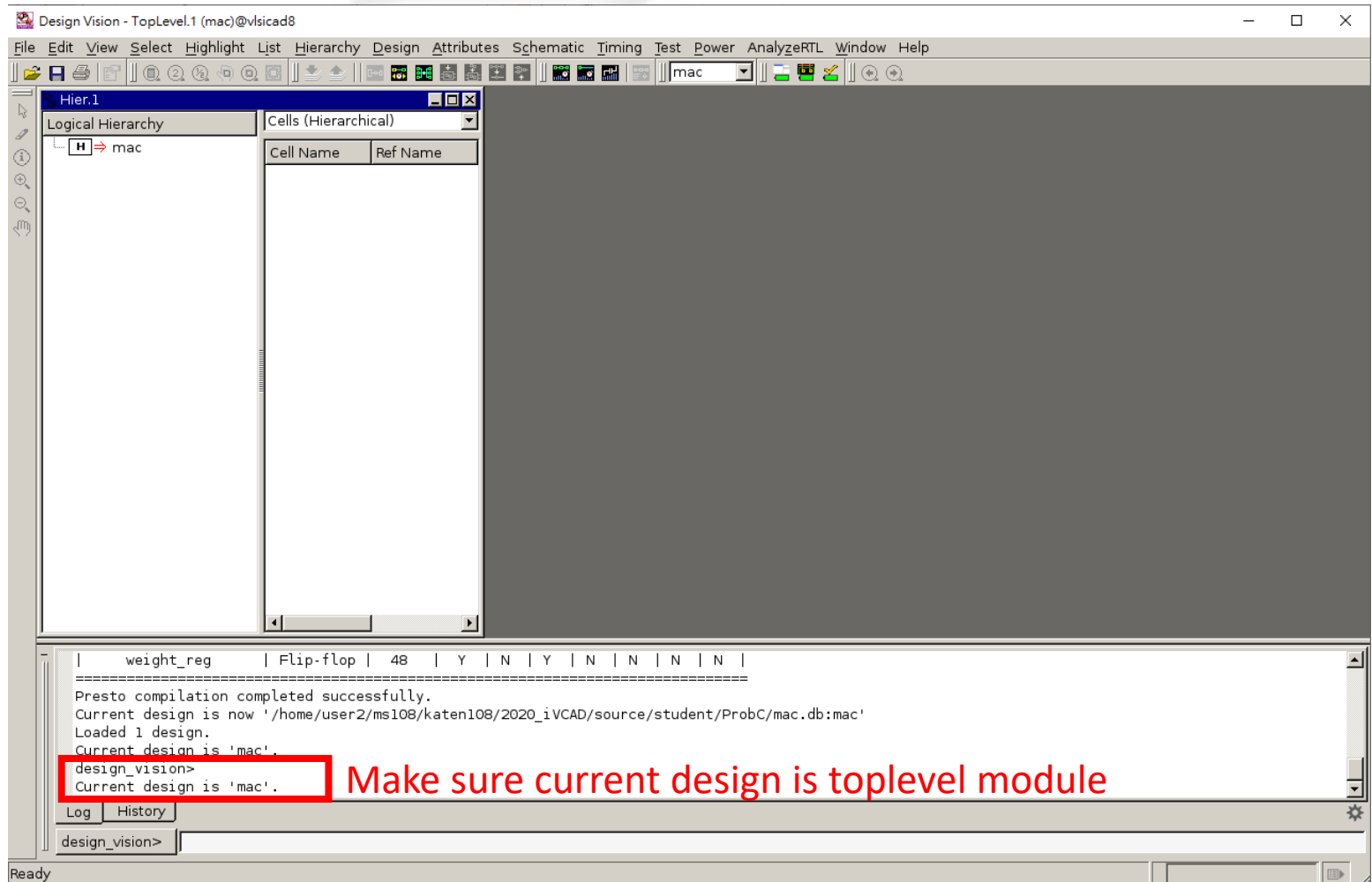
## Read Files (2)

- ❑ Choose toplevel design



# Read Files (3)

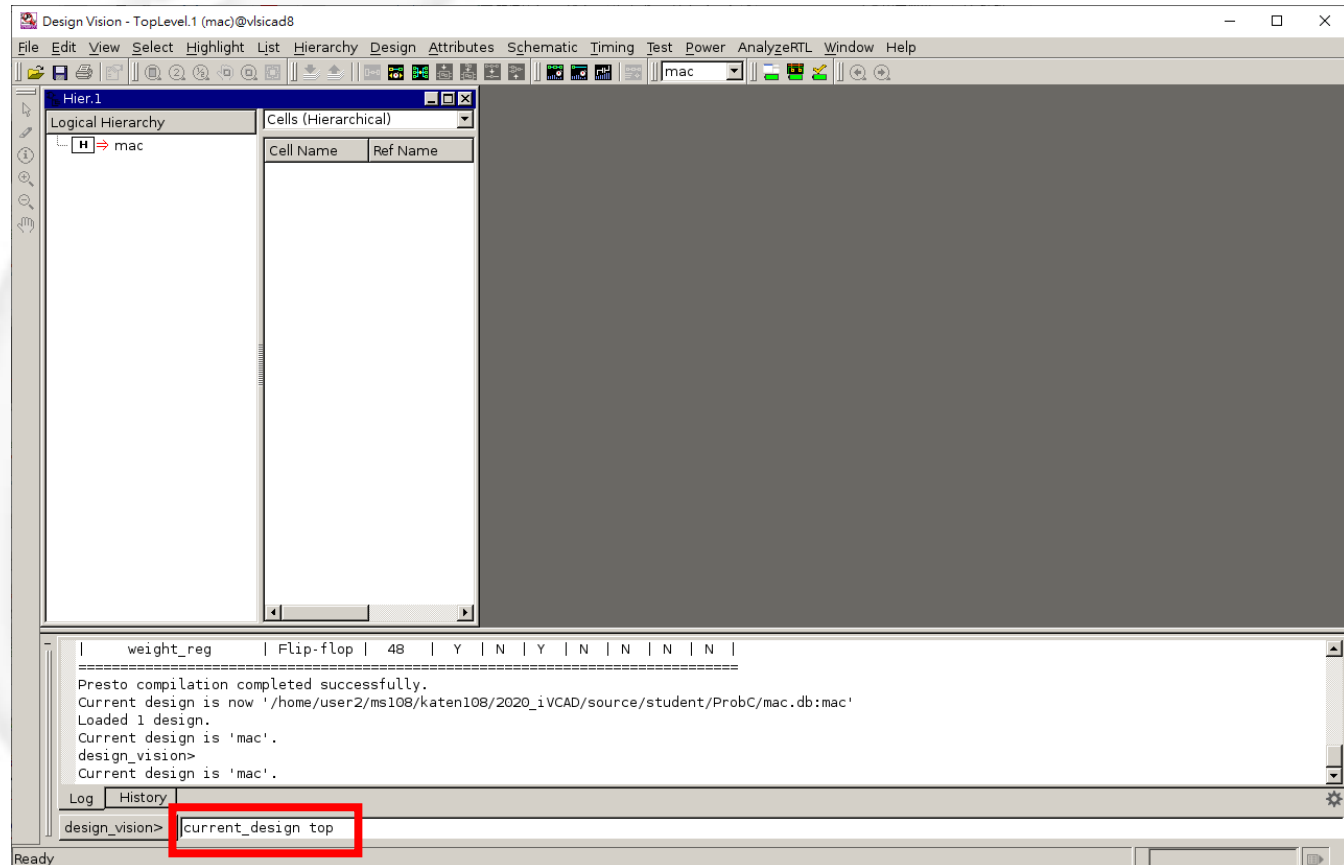
- Check if there is any error



Make sure current design is toplevel module

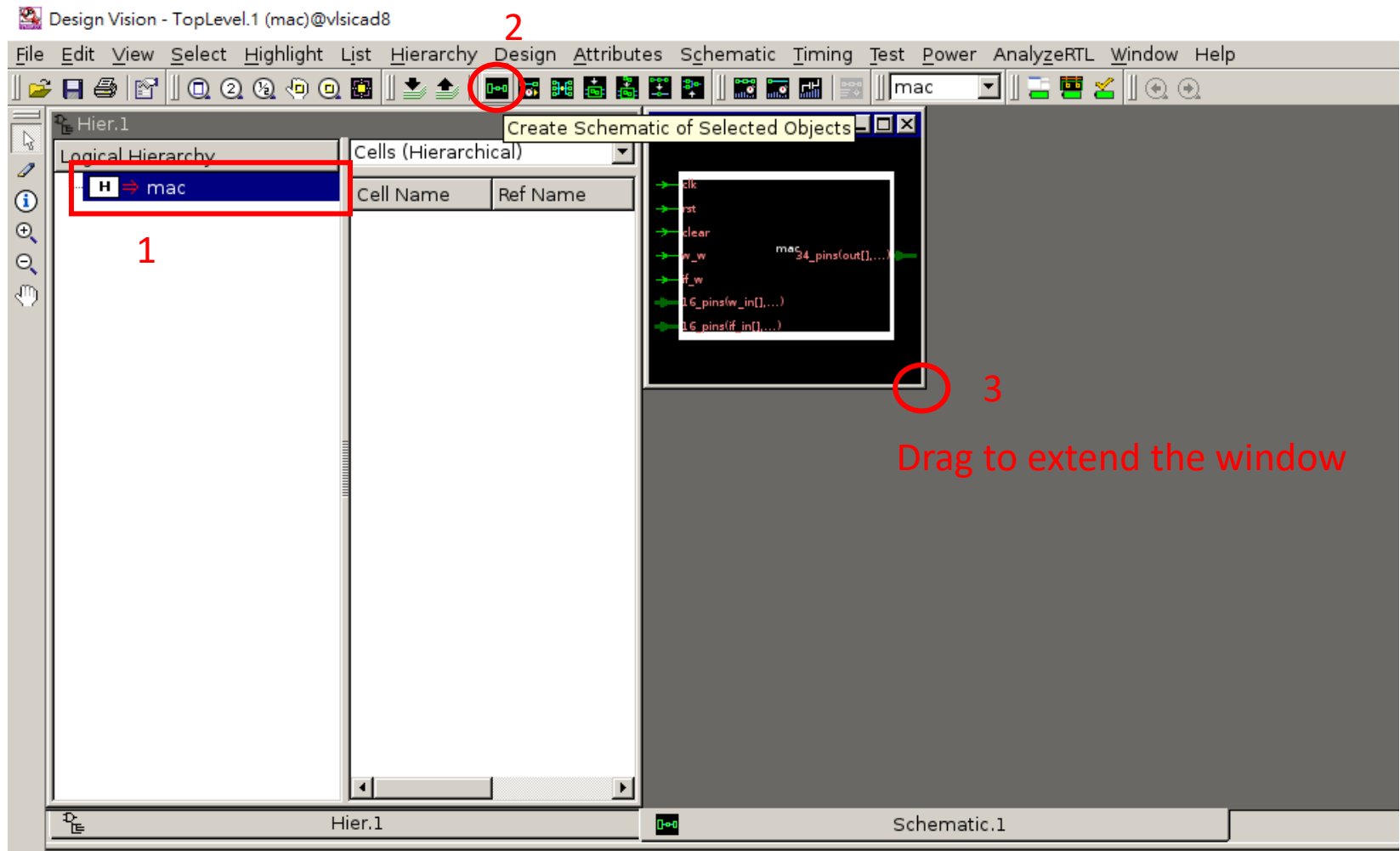
## Read Files (4)

- If current design is not toplevel module , use command **current\_deign module\_name** to change current design to toplevel module





# Open Schematic



# Define Clock Specification

- ❑ **Period**
- ❑ **Waveform**
- ❑ **Uncertainty**
  - ➔ Skew
- ❑ **Latency**
  - ➔ Source latency (option)
  - ➔ Network latency
- ❑ **Transition**
  - ➔ Input transition
  - ➔ Clock transition



# Clock Specification (1/2)

**Specify Clock**

Clock name: **clk**

Port name: **clk**

☐ Remove clock

Clock creation

Period: **10** unit: **ns**

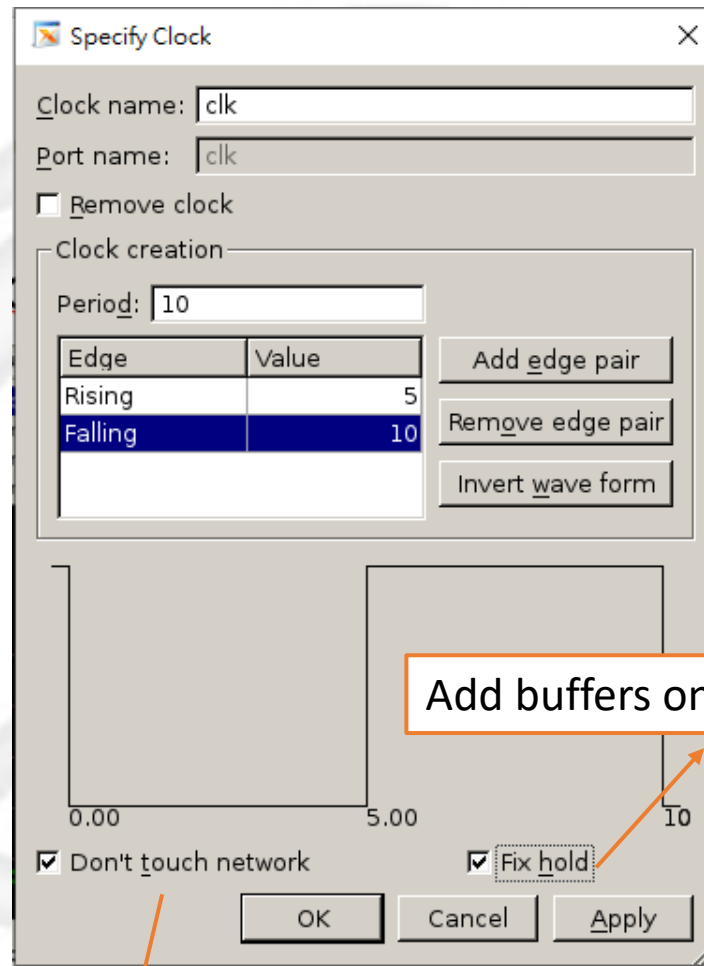
Edge	Value
Rising	5
Falling	10

☒ Don't touch network

☒ Fix hold



# Clock Specification (2/2)



The 'Specify Clock' dialog box is shown with the following settings:

- Clock name: `clk`
- Port name: `clk`
- ☐ Remove clock
- Clock creation:
  - Period: `10`
  - Table:

Edge	Value
Rising	5
Falling	10
  - 
  - 
  -
- ☒ Don't touch network
- ☒ Fix hold
- 

At the bottom, there is a graph area with a horizontal axis labeled 0.00, 5.00, and 10. An orange arrow points from the 'Fix hold' checkbox to the '10' mark on the axis.

Add buffers on data path to satisfy hold time

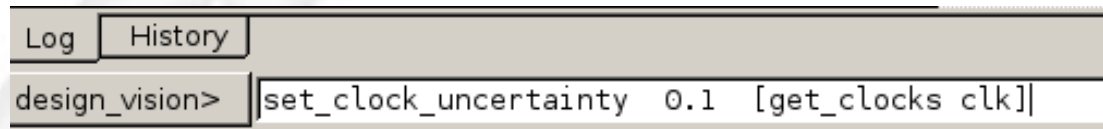
Don't add buffers on clock path

[Why fix hold?](#)

# Set clock uncertainty & clock latency

## □ Set clock uncertainty

→ `set_clock_uncertainty 0.1 [get_clocks clock_name]`

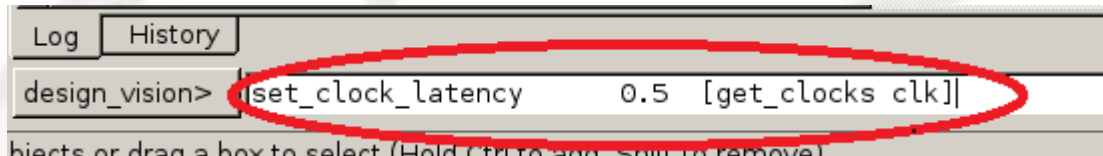


```
Log History  
design_vision> set_clock_uncertainty 0.1 [get_clocks clk]
```

[What is clock uncertainty ?](#)

## □ Set clock latency

→ `set_clock_latency 0.5 [get_clocks clock_name]`



```
Log History  
design_vision> set_clock_latency 0.5 [get_clocks clk]  
biects or drag a box to select (Hold Ctrl to add, Shift to remove)
```

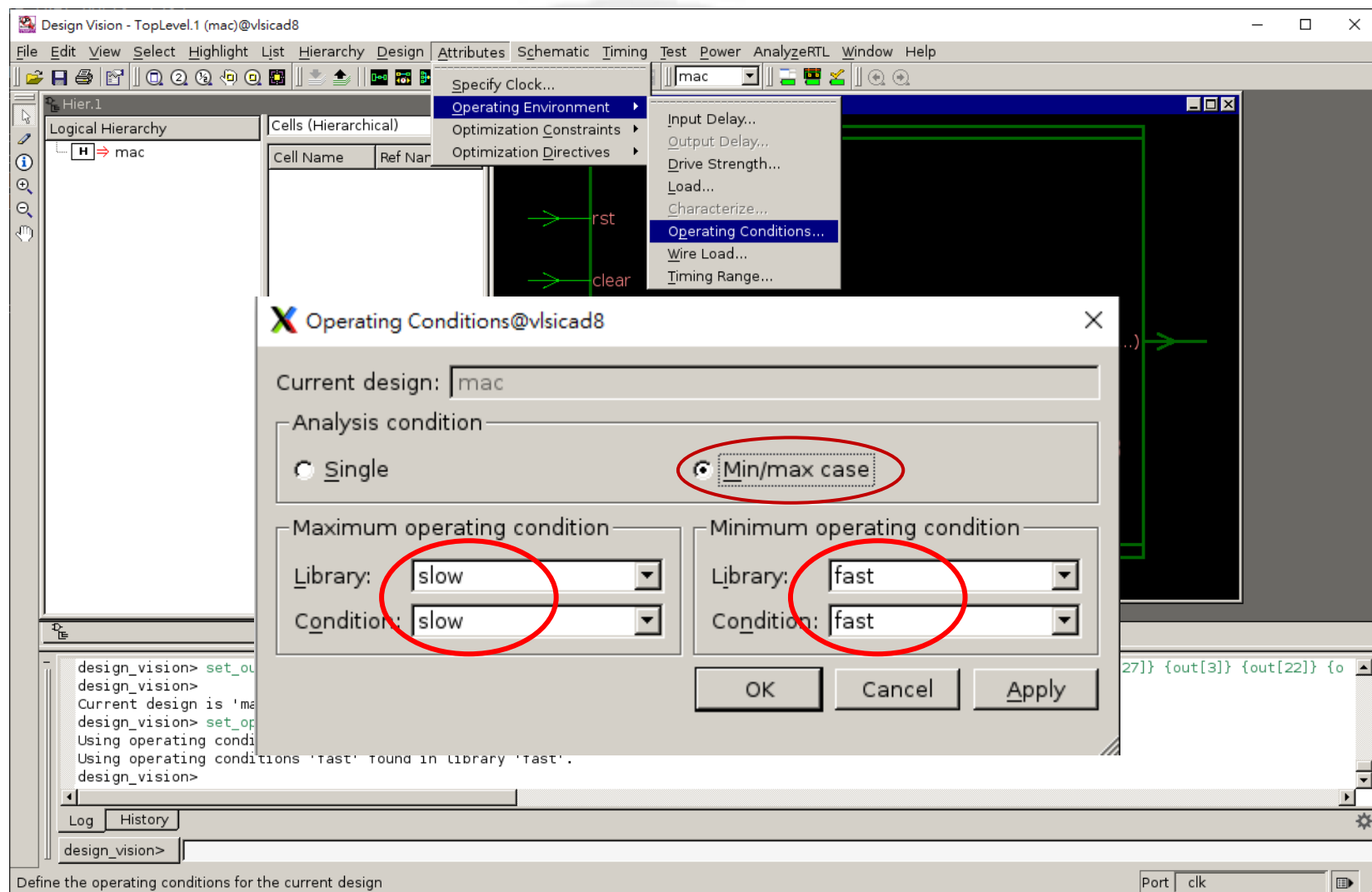
[What is clock latency ?](#)



# Define operating environment

- ❑ Set operating conditions
- ❑ Set driving cell
- ❑ Set load
- ❑ Set input delay
- ❑ Set output delay
- ❑ Set wire load model

# Operating Conditions



# Input delay

Design Vision - TopLevel.1 (mac)@vlsicad8

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help

Hier.1

Logical Hierarchy

Cells (Hierarchical)

Cell Name Ref Name

mac

Specify Clock...

Operating Environment

Optimization Constraints

Optimization Directives

Input Delay...

Output Delay...

Drive Strength...

Load...

Characterize...

Operating Conditions...

Wire Load...

Timing Range...

Input Delay@vlsicad8

Name: <Multiple Selected>

Relative to clock: clk

☒ Rising edge ☐ Falling edge

☒ Same rise and fall

Max rise: 5 Max fall: 5

Min rise: Min fall:

☐ Add delay

OK Cancel Apply

Hier.1 Schematic.1

Loaded 1 design.  
Current design is 'mac'.  
design\_vision>  
Current design is 'mac'.  
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/generic.sdb'  
design\_vision> create\_clock -name "clk" -period 10 -waveform { 5 10 } { clk }  
1  
design\_vision>

Log History

design\_vision>

Set input delay

Port 36

# Output delay

The screenshot shows the Design Vision software interface. The 'Output Delay@vlsicad8' dialog box is open, displaying the following settings:

- Name: <Multiple Selected>
- Relative to clock: clk
- ☒ Rising edge ☐ Falling edge
- ☒ Same rise and fall
  - Max rise: 0.5 Max fall: 0.5
  - Min rise: Min fall:
- ☐ Add delay

The background schematic shows a block labeled 'mac' with inputs 'w\_w', 'if\_w', '16\_pins(w\_in[,...])', and '16\_pins(if\_in[,...])'. The output is labeled '34\_pins(out[,...])'. A red oval highlights the output signal.

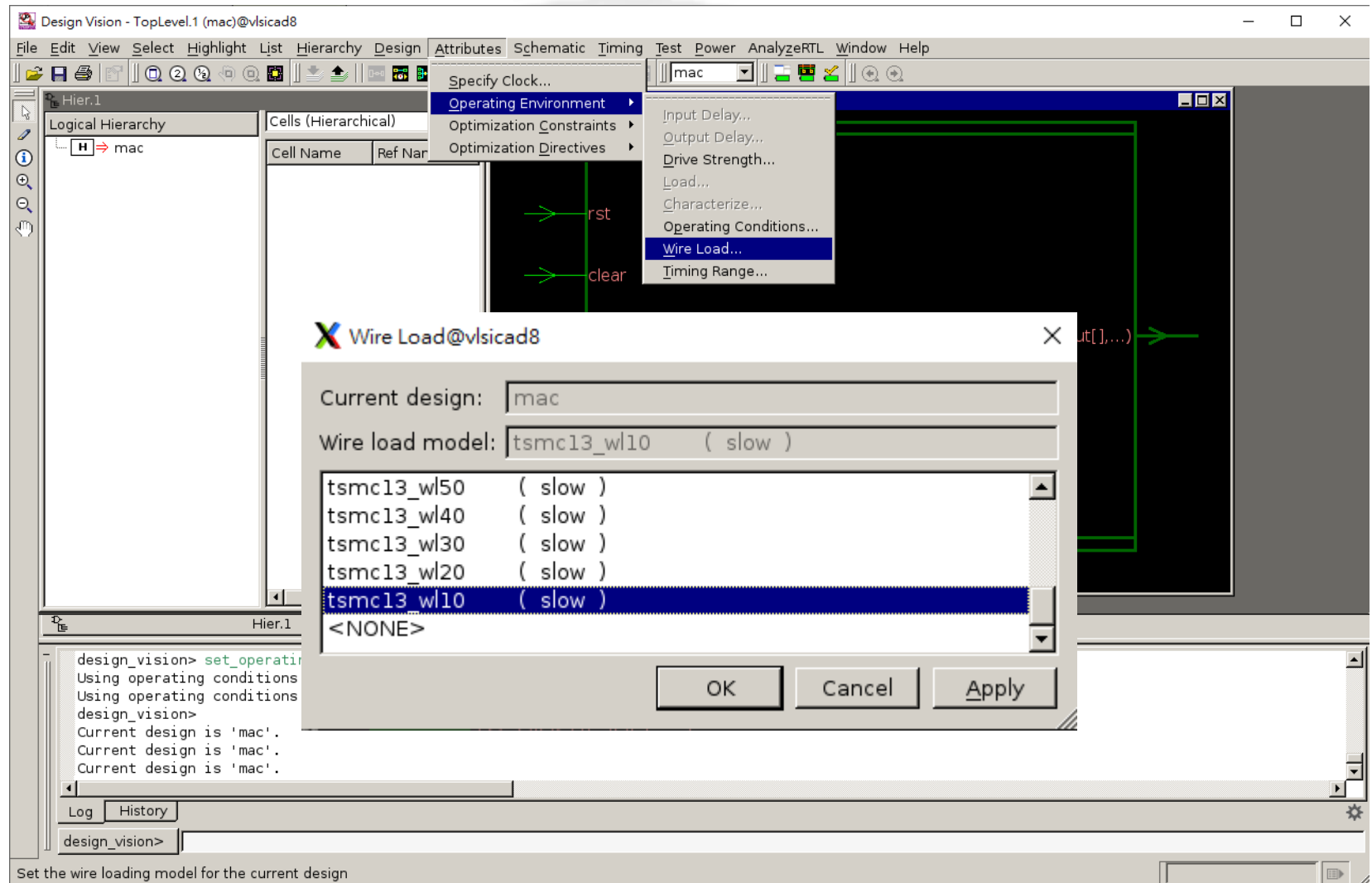
The command window at the bottom shows the following commands:

```

design_vision> set_input_delay -clock clk -max -rise 5 "{w_in[7]} {w_in[2]} {if_in[8]} {w_in[10]} {w_in[9]} {w_in[4]} {w_in[12]} {if_in[1]} {w_in[6]}
design_vision> set_input_delay -clock clk -max -fall 5 "{w_in[7]} {w_in[2]} {if_in[8]} {w_in[10]} {w_in[9]} {w_in[4]} {w_in[12]} {if_in[1]} {w_in[6]}
design_vision> set_input_delay -clock clk -min -rise 0 "{w_in[7]} {w_in[2]} {if_in[8]} {w_in[10]} {w_in[9]} {w_in[4]} {w_in[12]} {if_in[1]} {w_in[6]}
design_vision> set_input_delay -clock clk -min -fall 0 "{w_in[7]} {w_in[2]} {if_in[8]} {w_in[10]} {w_in[9]} {w_in[4]} {w_in[12]} {if_in[1]} {w_in[6]}
  
```

The status bar at the bottom indicates 'Set output delay' and 'Port 34'.

# Wire load





# Compile Design

The screenshot shows the Design Vision software interface. The 'Design' menu is open, and the 'Compile Design...' option is highlighted with a red circle and the number 1. The 'Compile (on vlsicad9)' dialog box is also open, showing various compilation options. The 'Map design' checkbox is checked, and the 'Exact map' sub-option is also checked. The 'Ma&p effort', 'Ar&ea effort', and 'Po&wer effort' are all set to 'medium'. The 'Fix design rules and optimize mapping' radio button is selected. The 'OK' button is highlighted with a red circle and the number 2.

Design Vision - TopLevel.1 (error\_diffusion) (on vlsicad9)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Win

Hier.1

Logical Hierarchy

H ⇒ error\_diffusion

Cells (Hierarchical)

Cell Name R

Compile Design... 1

Compile Ultra...

Check Design...

Report Design...

Report Design Hierarchy...

Report Design Resources...

Report Constraints...

Report Reference...

Report Ports...

Report Cells...

Report Nets...

Report Clocks...

Report Area...

Report Compile Options...

Report Power...

Analyze Datapath Extract...

Reset Current Design

Compile (on vlsicad9)

☒ Map design

☒ Exact map

Ma&p effort: medium

Ar&ea effort: medium

Po&wer effort: medium

☐ Top level ☐ Incremental mapping

☐ Ungroup ☐ Allow boundary condition

☐ Scan ☐ Auto ungroup

☐ Gate CI

☒ Area

☐ Delay

☒ Fix design rules and optimize mapping

☐ Optimize mapping only

☐ Fix design rules only

☐ Fix hold time only

OK 2 Cancel Apply

design\_vision> source DC.sdc

Information: Setting sdc\_version outside of an SDC file has no effect.

Using operating conditions 'slow' found in library 'slow'.

Using operating conditions 'fast' found in library 'fast'.

1

design\_vision>

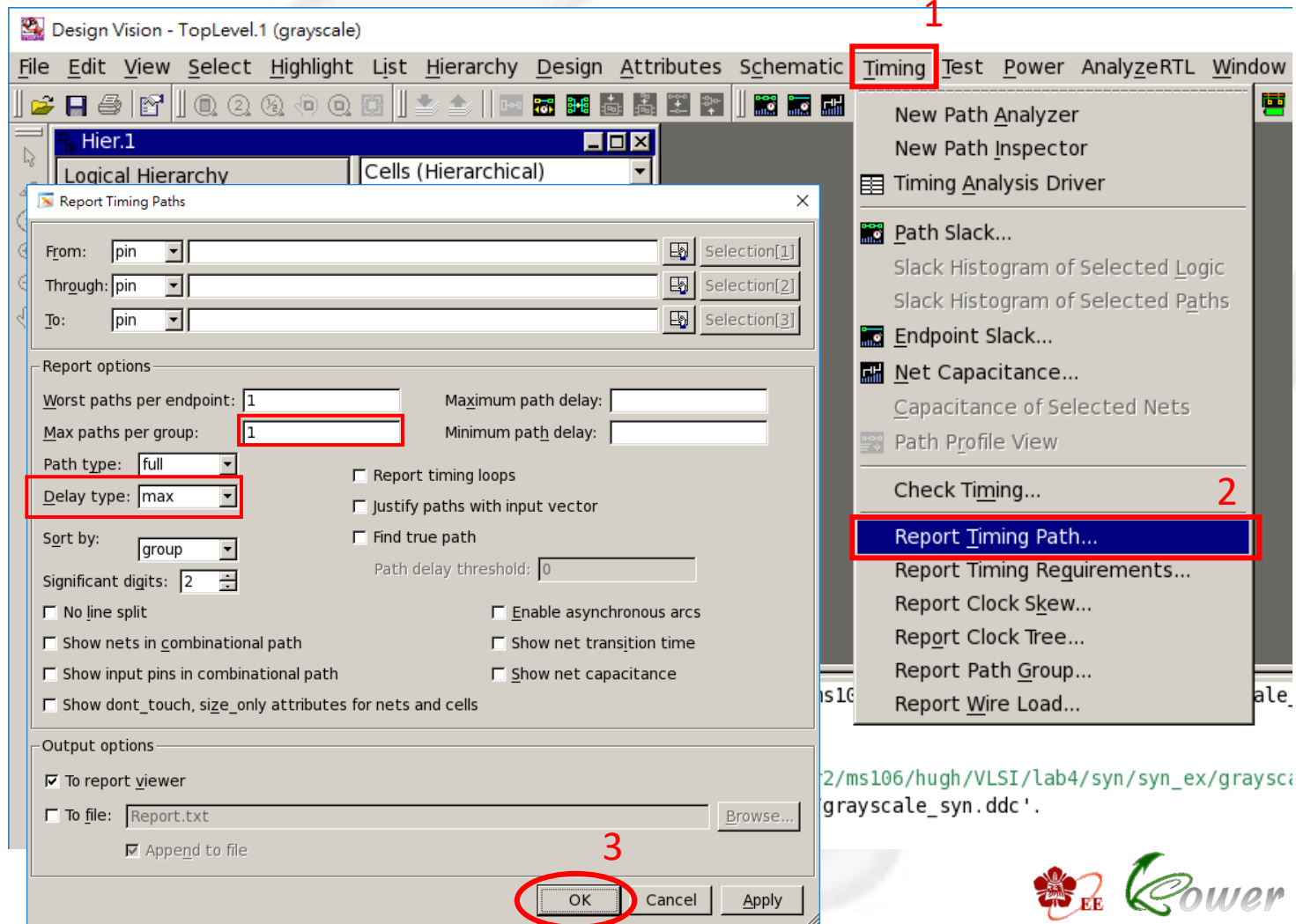
Log History

design\_vision>

Ready

# Report Timing (1/2)

## □ Command: report\_timing



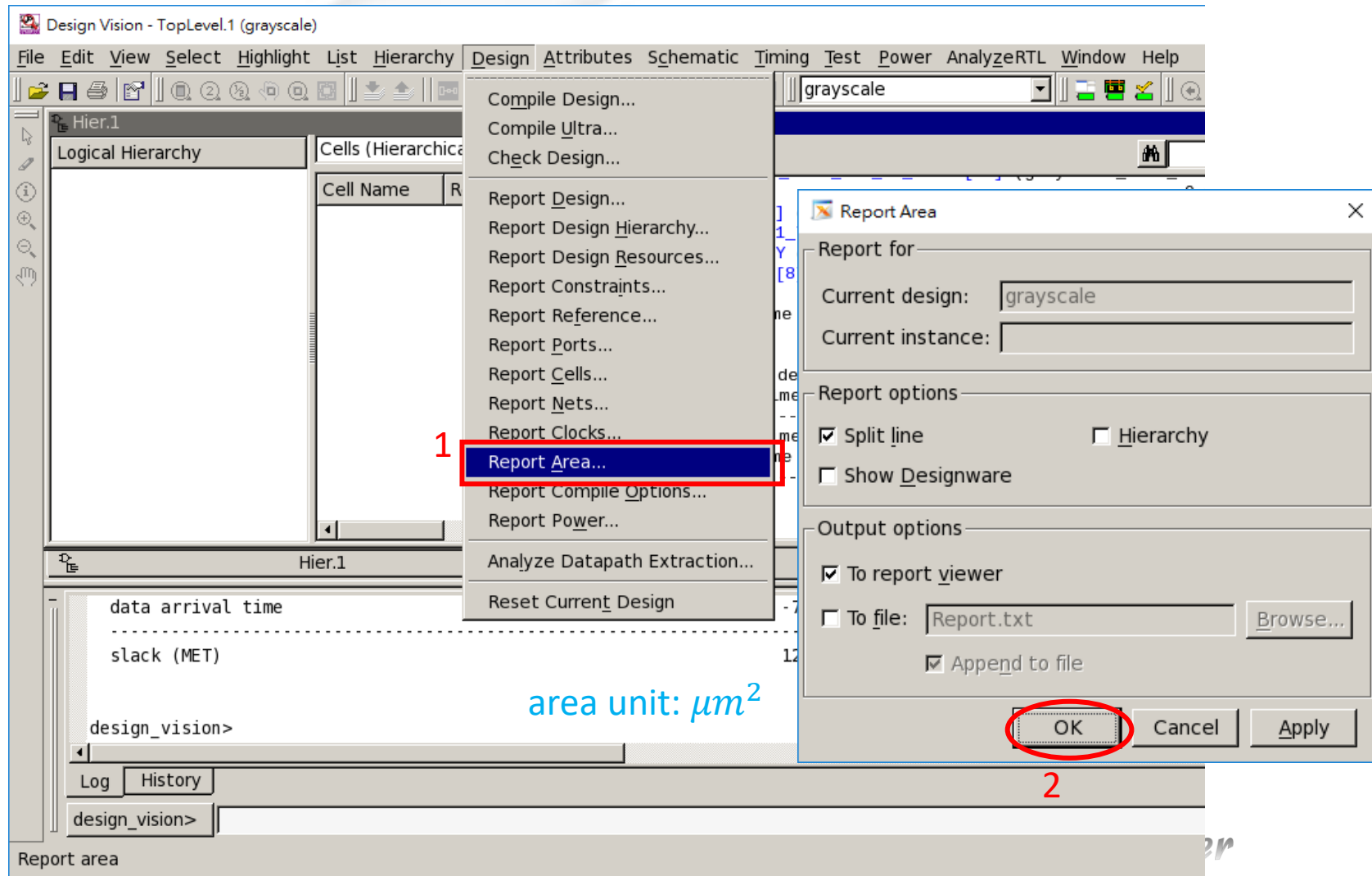
## Report Timing (2/2)

Slack must no less than 0, or it will lead to timing violation

Point	Incr	Path
-----		
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.50	0.50
input external delay	5.00	5.50 f
d[1] (in)	0.06	5.56 f
U78/Y (XOR2X1)	0.31	5.87 r
add_0_root_add_0_root_add_31_2/A[2] (grayscale_DW01_add_0)		
	0.00	5.87 r
add_0_root_add_0_root_add_31_2/U8/Y (OA21X4)	0.22	6.09 r
add_0_root_add_0_root_add_31_2/U9/Y (AO21XL)	0.47	6.56 r
add_0_root_add_0_root_add_31_2/U3/Y (NOR2X1)	0.21	6.77 f
add_0_root_add_0_root_add_31_2/U2/Y (OR2X1)	0.33	7.10 f
add_0_root_add_0_root_add_31_2/U12/Y (OA12BB1X2)	0.13	7.23 r
add_0_root_add_0_root_add_31_2/U1_4/C0 (ADDFHX2)	0.21	7.44 r
add_0_root_add_0_root_add_31_2/U1_5/C0 (ADDFHX2)	0.22	7.66 r
add_0_root_add_0_root_add_31_2/U1_6/C0 (ADDFHX4)	0.22	7.88 r
add_0_root_add_0_root_add_31_2/U4/Y (XOR2X1)	0.24	8.12 r
add_0_root_add_0_root_add_31_2/U1/Y (XOR2X2)	0.31	8.43 f
add_0_root_add_0_root_add_31_2/SUM[7] (grayscale_DW01_add_0)		
	0.00	8.43 f
add_39/A[2] (grayscale_DW01_inc_0)	0.00	8.43 f
add_39/U1_1_2/C0 (ADDHX1)	0.34	8.77 f
add_39/U3/Y (AND2X2)	0.28	9.06 f
add_39/U6/Y (AND2X4)	0.20	9.26 f
add_39/U2/Y (AND2X2)	0.25	9.50 f
add_39/U13/Y (NAND2X1)	0.20	9.70 r
add_39/U1/Y (XOR2X2)	0.20	9.90 r
add_39/SUM[7] (grayscale_DW01_inc_0)	0.00	9.90 r
U40/Y (AO122X2)	0.17	10.07 f
U39/Y (OA121X2)	0.15	10.22 r
q_reg[7]/D (DFFRX2)	0.00	10.22 r
data arrival time		10.22
clock clk (rise edge)	10.00	10.00
clock network delay (ideal)	0.50	10.50
clock uncertainty	-0.10	10.40
q_reg[7]/CK (DFFRX2)	0.00	10.40 r
library setup time	-0.18	10.22
data required time		10.22
-----		
data required time		10.22
data arrival time		-10.22
-----		
slack (MET)		0.00

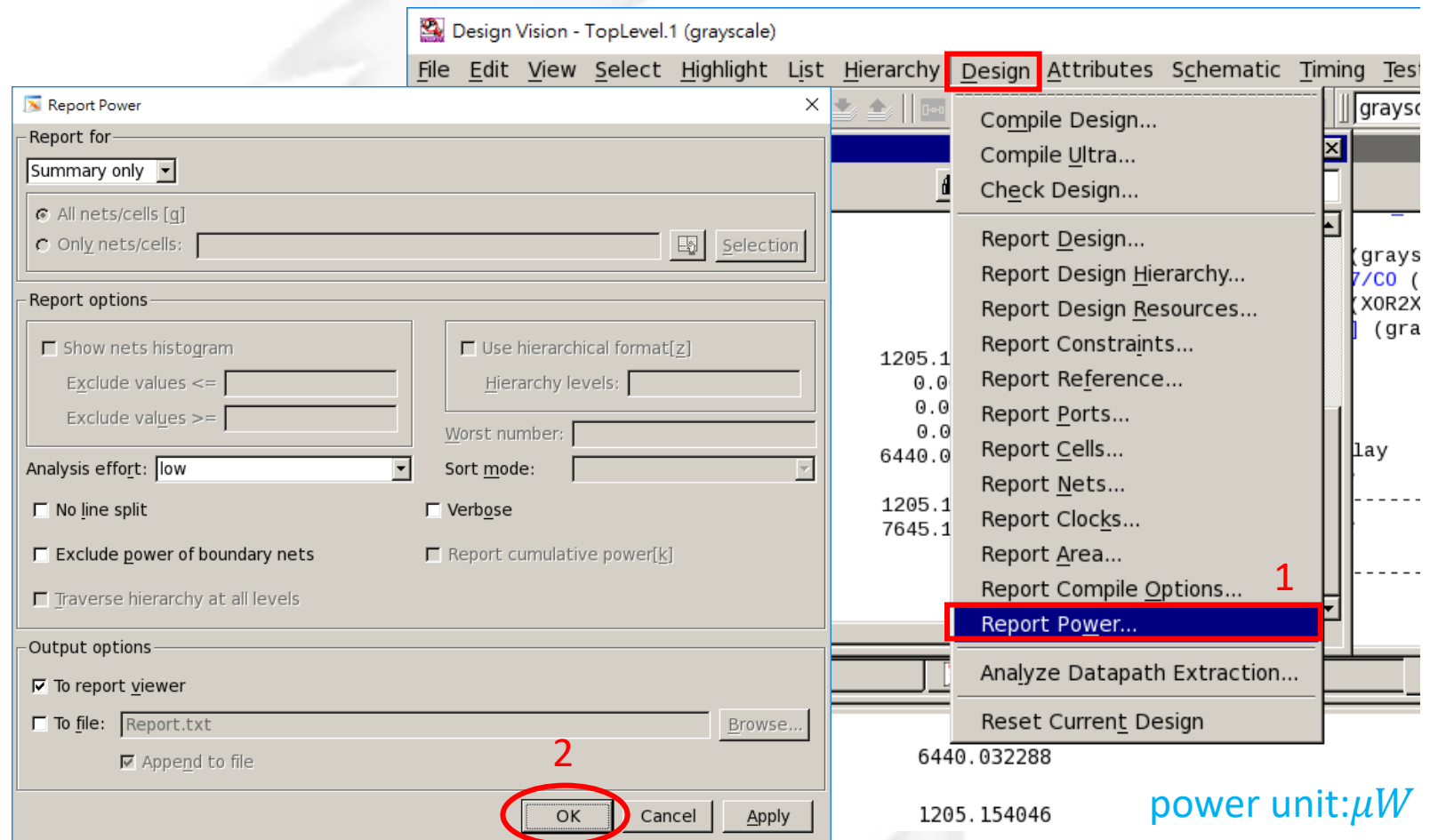
# Report Area

□ Command: report\_area



# Report Power

□ Command: report\_power

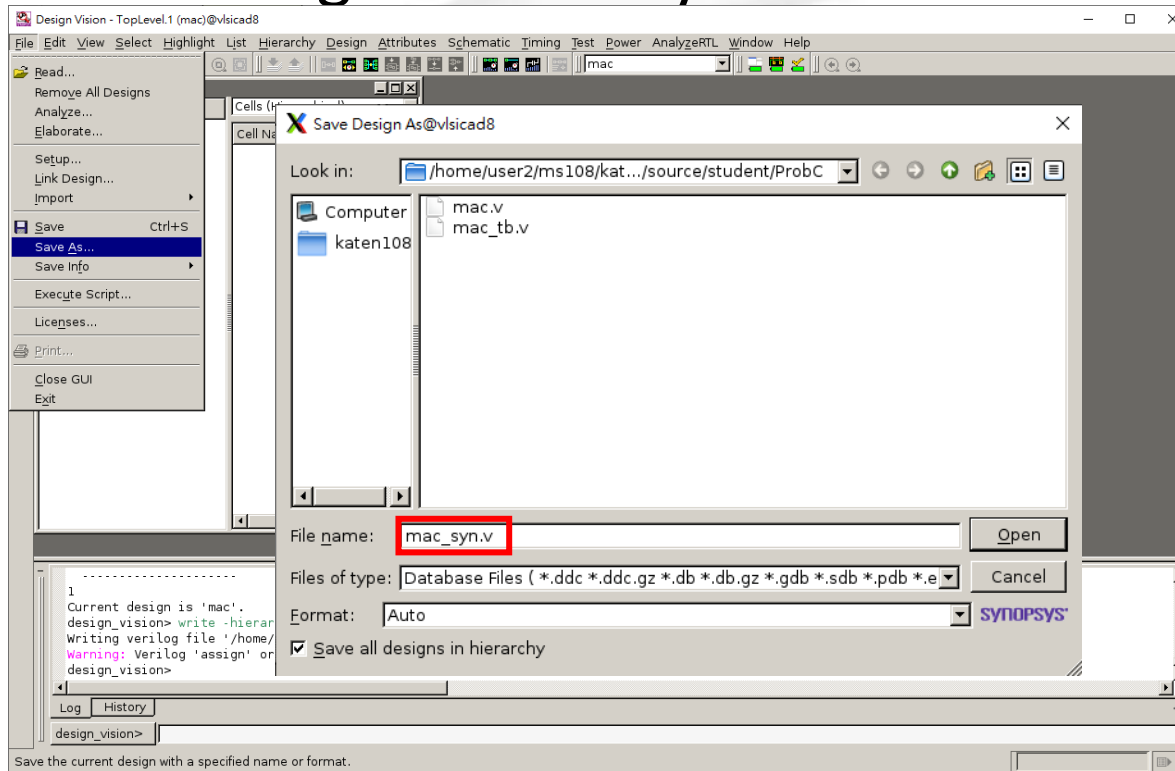


power unit:  $\mu W$



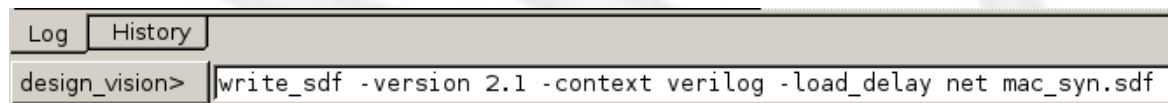
# Save File

## □ The Verilog file after synthesis



## □ SDF File:

write\_sdf -version 2.1 -context verilog -load\_delay net filename.sdf



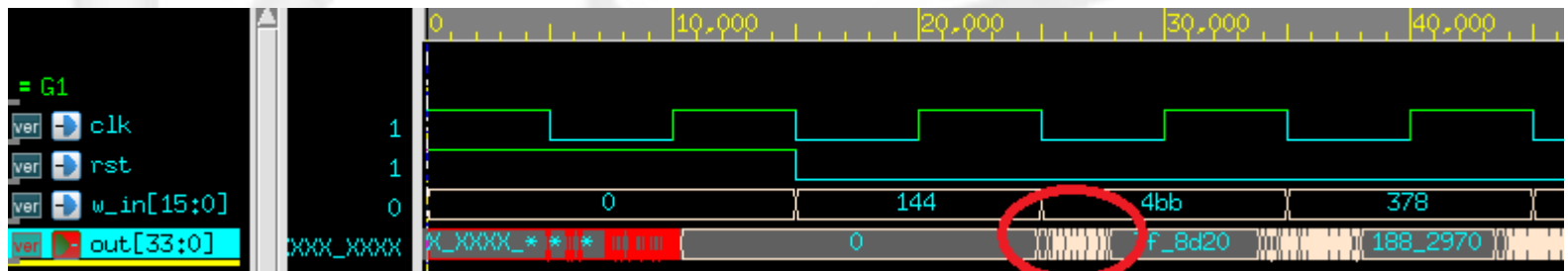


# Post Simulation

- ❑ In your test bench
  - ➔ Apply delay in your design use command :
  - ➔ `$sdf_annotate("sdf_file_name", module_instance_name)`

```
mac m1(.clk(clk),.rst(rst),.clear(clear),.w_w(w_w),.w_in(w_in),.if_w(if_w),.if_in(if_in),.out(out));
`ifdef syn
initial $sdf_annotate("mac_syn.sdf",m1);
`endif
```

- ❑ Post sim waveform



# Work with tcl

```
DC.sdc x
1 # operating conditions and boundary conditions #
2
3 set cycle 10.0 ;#clock period defined by designer
4
5 create_clock -period $cycle [get_ports clk]
6 set_fix_hold [get_clocks clk]
7 set_dont_touch_network [get_clocks clk]
8 set_clock_uncertainty 0.1 [get_clocks clk]
9 set_clock_latency 0.5 [get_clocks clk]
10
11 set_input_delay 5 -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
12 set_output_delay 0.5 -clock clk [all_outputs]
13 set_load 0.1 [all_outputs]
14 set_drive 0.1 [all_inputs]
15
16 set_operating_conditions -max slow -min fast
17 set_wire_load_model -name tsmc13_wl10 -library slow
18
19 set_max_fanout 20 [all_inputs]
```

# Work with tcl

- ☐ Setup library
- ☐ Read file
- ☐ Read script
- ☐ Compile
- ☐ Check report
- ☐ Save design

**UPHCLAB**  
VLSI Design LAB

**UHP LAB**  
VLSI Design LAB



## Reference

- (C104) Logic Synthesis with Design Compiler training manual



# Appendix



# The DC Setup File

```

synopsys_dc.setup
1 set company "CIC"
2 set designer "Student"
3
4 set CellLibraryPath /usr/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db
5
6 set search_path ". $CellLibraryPath $search_path"
7 set target_library "slow.db typical.db fast.db"
8 set synthetic_library "dw_foundation.sldb"
9 set link_library "* $target_library $synthetic_library"
10
11 set_min_lib slow.db -min fast.db ; #for core lib
12
13 set verilayout_no_tri true
14 set hdlin_enable_presto_for_vhdl "TRUE"
15 set sh_enable_line_editing true
16 history keep 100
17 alias h history
18

```

Name	Temperature	Voltage
Slow	125	1.62
Typical	25	1.8
Fast	-40	1.98

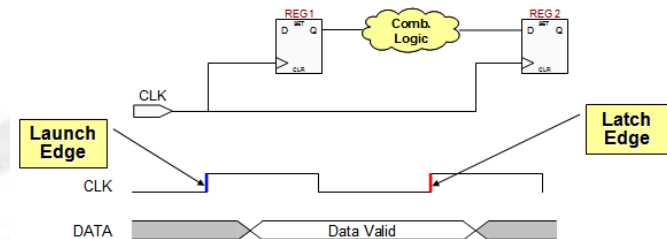

 Back

# Timing violation

## □ Setup time & hold time

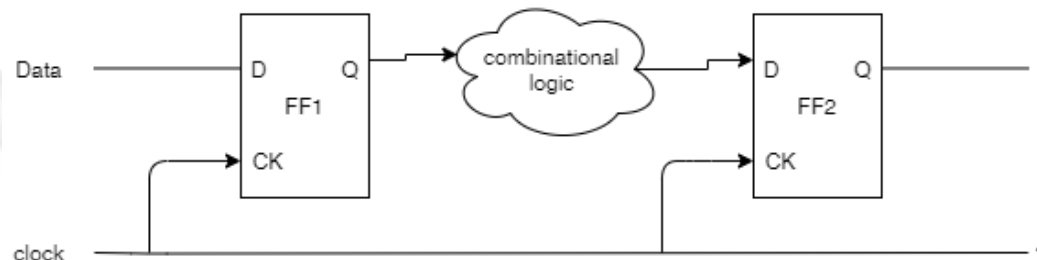
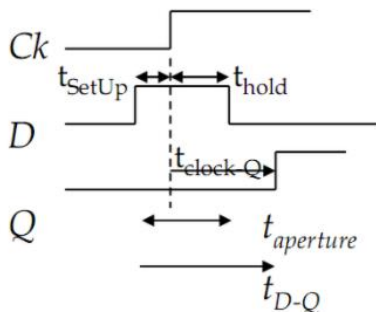
- ➔ Setup time : the amount of time the data at the synchronous input (D) must be stable before the active edge of clock.
- ➔ Hold time : the amount of time the data at the synchronous input (D) must be stable after the active edge of clock.

## □ Launch edge & latch edge :



## □ Arrival time

- ➔ Data arrival time (launch edge + clock source  $\rightarrow$  FF1/CK + FF1/CK  $\rightarrow$  FF1/Q + FF1/Q  $\rightarrow$  FF2/D)
- ➔ Clock arrival time (latch edge + clock source  $\rightarrow$  FF2/CK)



# Timing violation

## □ Setup time violation (data path too long)

➔ **Clock arrival time < Data arrival time + setup time**

➔ How to fix ?

◆ Add clock period

◆ Add flip-flops in longest clock path

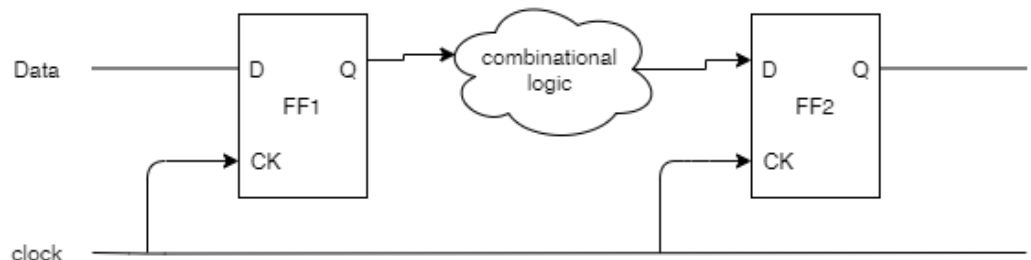
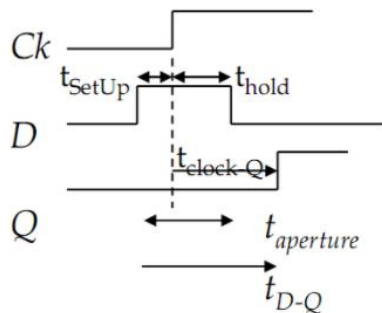
## □ Hold time violation (data path too short)

➔ **Clock arrival time + hold time > Data arrival time**

➔ How to fix ?

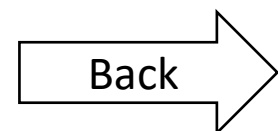
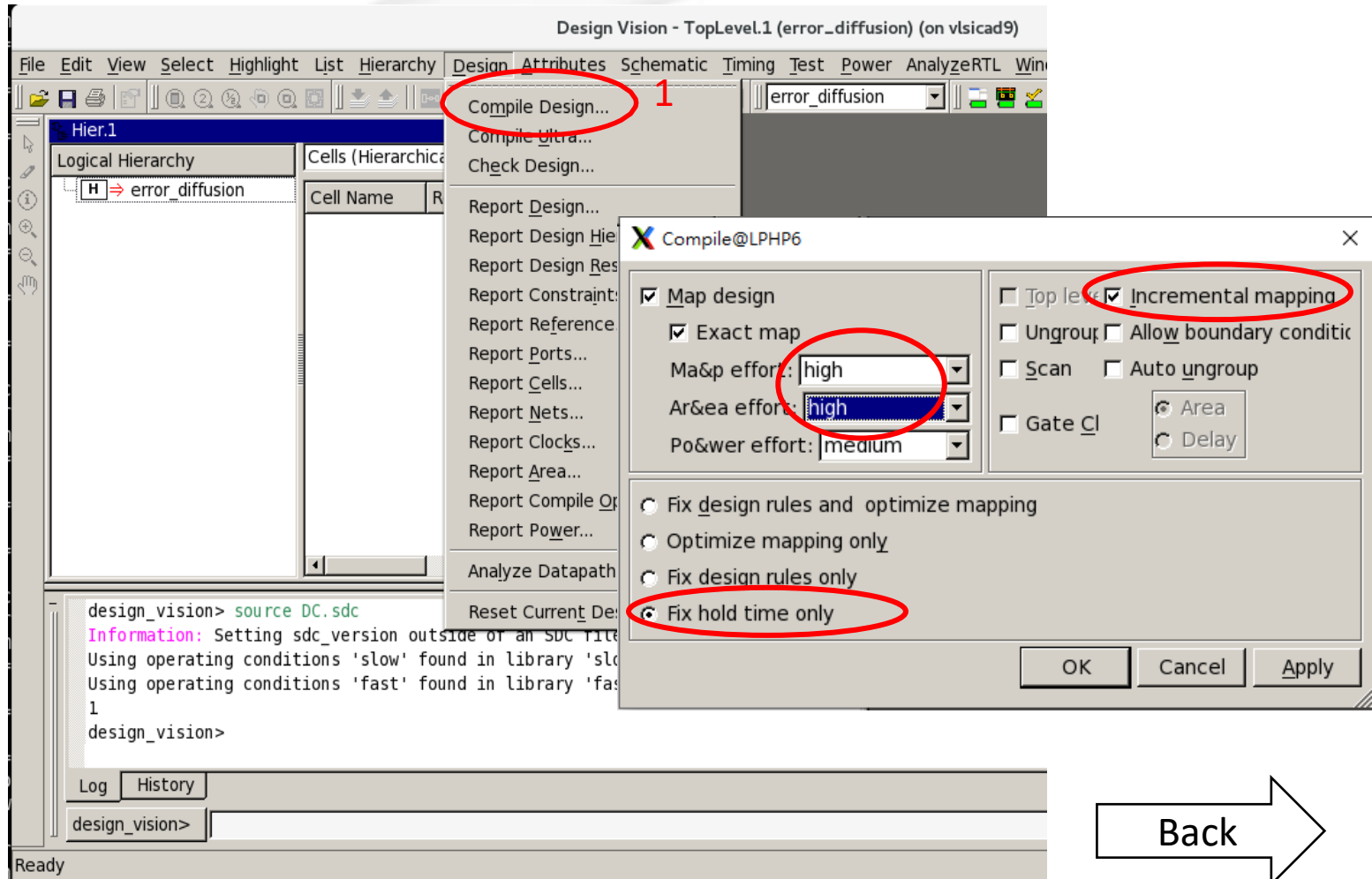
◆ Fix hold (add buffers in data path)

◆ Incremental compile



# Timing violation

## Incremental compile

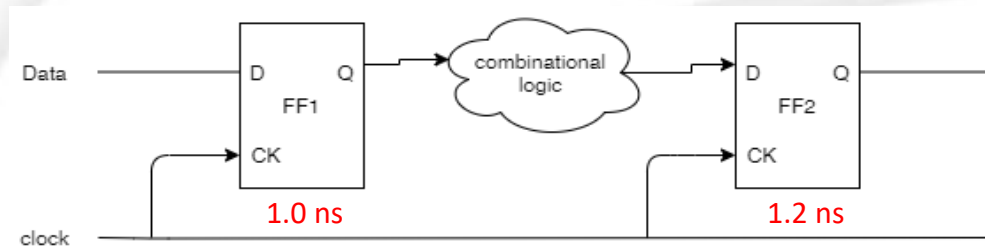


# Clock uncertainty

□ Clock uncertainty  $\approx$  clock skew + clock jitter

□ Clock skew

➔ The maximum difference between the arrival of clock signals at sequential cells in one clock domain or between domains



$$\text{Clock skew} = 1.2 - 1.0 = 0.2 \text{ (ns)}$$

□ Clock jitter

➔ the timing variations of a set of signal edges from their ideal values

Back

# Clock latency

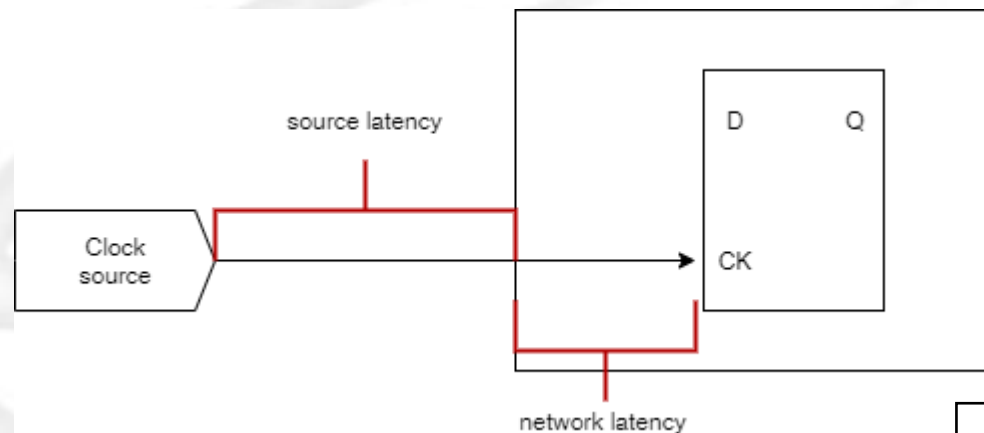
## □ What is clock latency

### → Source latency

- ◆ Propagation time from the actual clock origin to the clock definition point in the design

### → Network latency

- ◆ Propagation time from the clock definition point in the design to the register's clock pin



Back





**Thank you  
For your attention!!**