EE309 Microprocessors Project - Multicycle RISC Design - IITB-RISC

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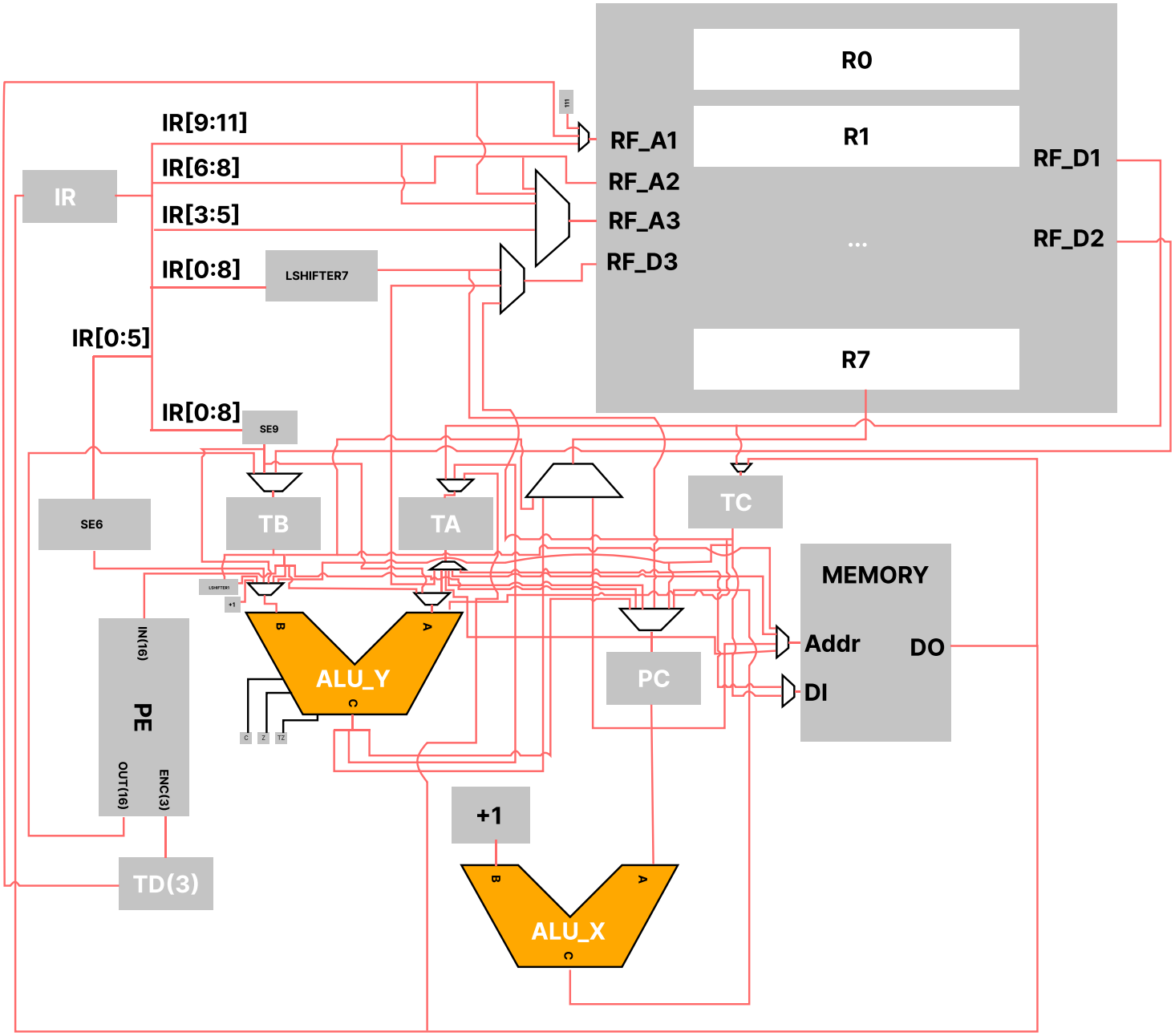
The datapath consists of Two 16 bit ALUs, One 16 bit priority encoder that gives a 16 bit output and 3bit register address. There are two Sign Extenders SE6 and SE9 for 6 and 9 bit inputs giving 16 bit outputs. There are two left bit shifters Lshifter7 and Lshifter1 which respectively shift the input by 7 and 1 bit (s) to the left appending 0s to the right giving a 16 bit output. There are four temporary registers TA, TB, TC, TD, where TA, TB and TC are 16bit and TD is 3bit.

The instructions and information regarding the 26 states of the FSM can be found in the file `States.pdf` and the state flow diagram can be found in the file `State Flow.pdf`. The control decode logic for each instruction can be found in the file `Decoding Logic.pdf`. The control words can be found in the file `Control Words.pdf`

The project folder also has attached the hardware descriptions of the various components in VHDL. The toplevel entity contains the Datapath and the FSM.

The next page has the datapath schematic, showing all the components of the datapath and their connections. The pages following the datapath schematic contain the RTL view of the compiled project folder in Intel Quartus


R0
R1
...
R7
RF_A1
RF_A2
RF_A3
RF_D3
RF_D1
RF_D2
IR
IR[9:11]
IR[6:8]
IR[3:5]
IR[0:8]
IR[0:5]
IR[0:8]
LSHIFTER7
SE9
SE6
TB
TA
TC
MEMORY
Addr
DO
DI
PC
ALU_Y
ALU_X
PE
IN(16)
OUT(16)
ENC(3)
TD(3)
+1

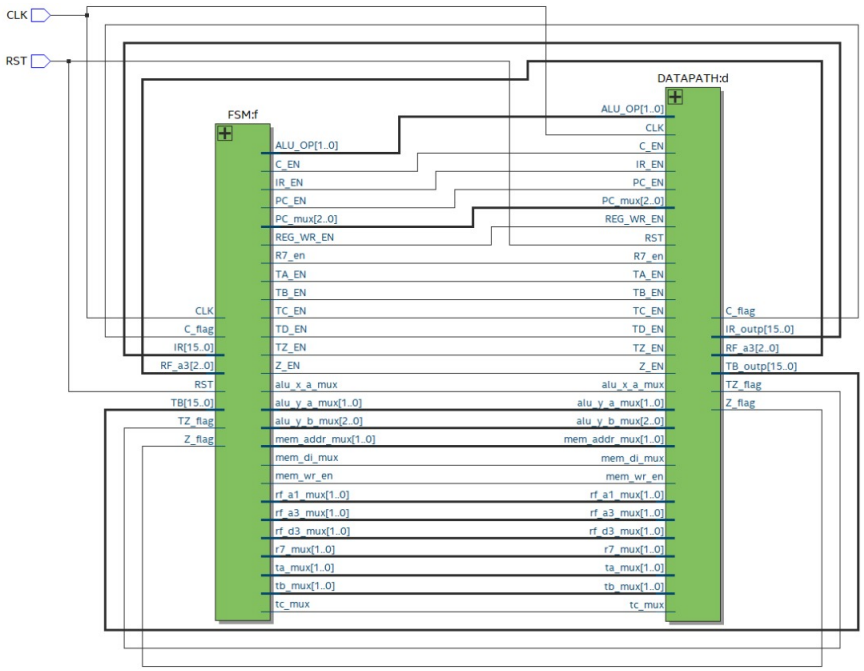


Figure 1: RTL View of the toplevel entity

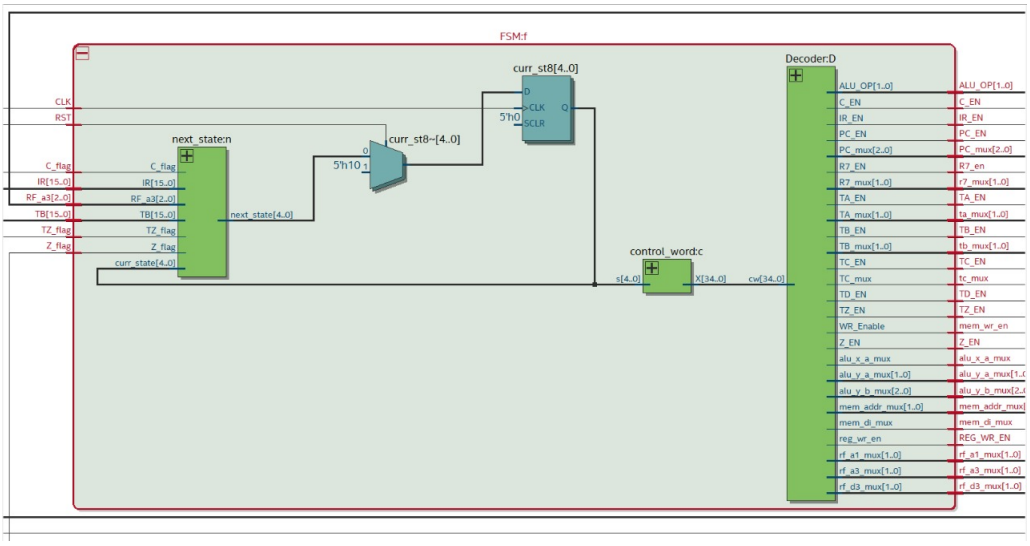


Figure 2: RTL View of FSM

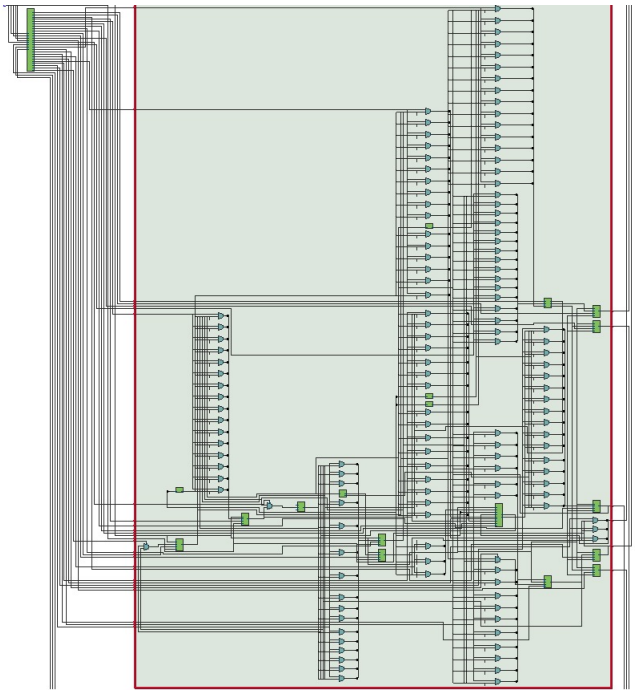


Figure 3: RTL View of Datapath

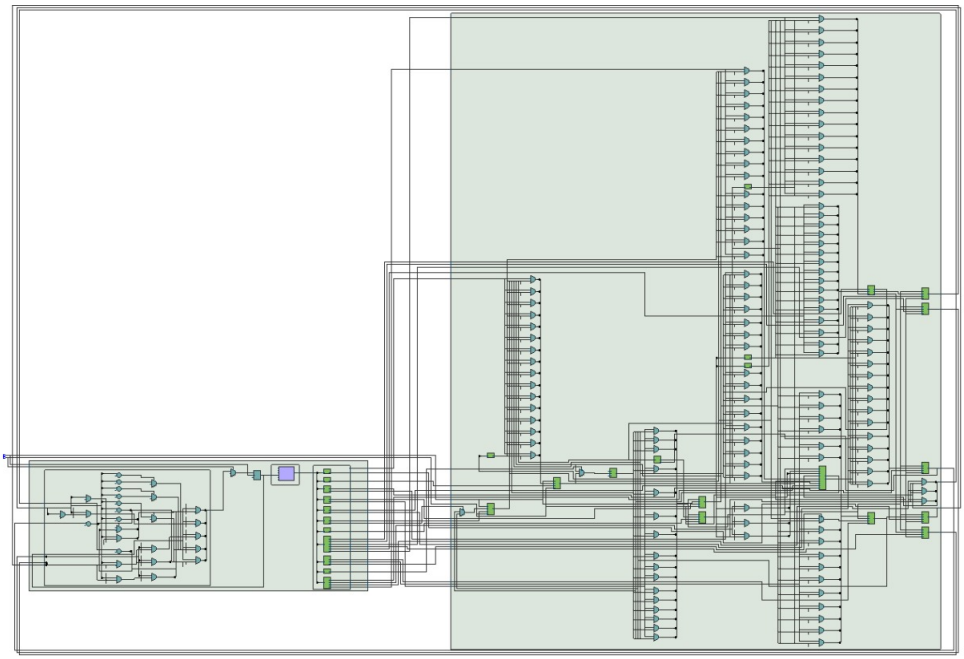


Figure 4: Expanded RTL View of the toplevel entity