1. ADD(R)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2
	S3
ta → aluy_a tb → aluy_b aluy_c →ta	ADD
	NA

	mod c and z
	S3
	S4
ta → rf_d3 ir[3:5] → rf_a3 if(rf_a3 == 111){ta → PC} else{PC → R7}	NOP
	NA
	NM
	S4
	IB

2. ADC(R)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)

	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb if(c == 0){PC → R7}	NOP
	NA
	NM
	S2
	S3
ta → aluy_a tb → aluy_b aluy_c →ta	ADD
	mod c and z
	NA
	S3
	S4

ta → rf_d3 ir[3:5] → rf_a3 if(rf_a3 == 111){ta → PC} else{PC → R7}	NOP
	NM
	NA
	S4
	IB

3. ADZ(R)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta	NOP
	NM

rf_d2 → tb if(z == 0){PC → R7}	NA
	S2
	S3
ta → aluy_a tb → aluy_b aluy_c →ta	ADD
	mod c and z
	NA
	S3
	S4

ta → rf_d3
ir[3:5] → rf_a3
if(rf_a3 == 111){ta → PC}
else{
PC → R7}
	NOP

	NM
	NA
	S4

	IB

4. ADI (I)

PC → mem_addr/ alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	NM
	IR
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NM
	NA
	S2
	S5
	ADD

ta → aluy_a ir[0:5] → SE6 → aluy_b aluy_c → ta	NM
	NA
	S5
	S4
ta → rf_d3 ir[6:8] → rf_a3 if(rf_a3 == 111){ta→PC}else{PC→ R7}	NOP
	NM
	NA
	S4
	IB

5. ADL(R)

PC → mem_addr/ alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2
	S6
ta → aluy_a tb → Lshifter_1 → aluy_b aluy_c → ta	ADD
	mod c and z

	NA
	S6
	S4
ta → rf_d3 ir[3:5] → rf_a3 if(rf_a3 == 111){ta → PC}else{PC → R7}	NOP
	NM
	NA
	S4
	IB

6. NDU(R) (replace (S3, S5, S6) OP of ADD with NAND and mod c and z to mod z)
7. NDC(R) (replace (S3, S5, S6) OP of ADD with NAND and mod c and z to mod z)
8. NDZ(R) (replace (S3, S5, S6) OP of ADD with NAND and mod c and z to mod z)

9. LHI (J)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	NM
	IR
	S1(HKT)
	S7
ir[0:8] → Lshifter_7 → rf_d3 ir[9:11] → rf_a3 if(rf_a3 == 111){ir[0:8] → Lshifter_7 → PC} else{PC → R7}	NOP
	NA
	NM
	S7
	IB

10. LW(I)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2
	S8
ir[0:5] → SE6 → aluy_b tb → aluy_a aluy_c → ta	ADD
	NA

	NM
	S8
	S9
ta → mem_addr mem_do → ta	NOP
	DR
	NM
	S9
	S10
ta → rf_d3 ir[9:11] → rf_a3 if(rf_a3 == R7){ta → PC} else{PC → R7}	NOP
	NA
	NM
	S10

	IB

11. SW(I)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2
	S8

ir[0:5] → SE6 → aluy_b tb → aluy_a aluy_c → ta	ADD
	NA
	NM
	S8
	S11
ta → mem_di tb → mem_addr PC → R7	NA
	DW
	NM
	S11
	IB

12. LM(J)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2
	S12
ir[0:8] → SE9 → tb	NOP
	NA

	NM
	S12
	S13
tb → PE_in PE_out → tb PE_enc → td ta → mem_addr mem_do → tc	NOP
	DR
	NM
	S13
	S14
td → rf_a3 tc → rf_d3 ta → aluy_a +1 → aluy_b aluy_c → ta if(rf_a3 == 111){tc->PC}else{PC-> R7}	ADD
	NA
	NM
	S14

	BC if(tb=0x0000){IB}else{S13}

13. SM(J)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2

	S13
ir[0:8] → SE9 → tb	NOP
	NA
	NM
	S13
	S15
tb → PE_in PE_enc → td PE_out → tb	NOP
	NA
	NM
	S15
	S16

td → rf_a1 rf_d1 → tc	NOP
	NA
	NM
	S16
	S17
ta → mem_addr tc → mem_di ta → alux_a +1 → alux_b alux_c → ta PC → R7	ADD
	DW
	NM
	S17
	BC if(tb=0x0000){IB}else{S15}

14. BEQ(I)

PC → mem_addr/alux_a mem_do → ir	ADD

+1 → alux_b alux_c → PC	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2
	S18
ta → aluy_a tb → aluy_b	XOR
	NA
111 → rf_a1 rf_d1 → ta	mod tz

	S18
	S19

if (tz == 1){
ta → aluy_a
ir[0:8] → SE9 → aluy_b
aluy_c → PC, R7
}
else{
nop
}
	ADD

	NA
	NM
	S19
	IB

15. JAL(J)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2
	S20
111 → rf_a1 rf_d1 → tc	NOP
	NA

	NM
	S20
	S21
ir[0:8] → SE9 → aluy_a tc → aluy_b, rf_d3 aluy_c → PC,R7 ir[9:11] → rf_a3	ADD
	NA
	NM
	S21
	IB

16. JLR(I)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)

	S2
ir[9:11] → rf_a1 ir[6:8] → rf_a2 rf_d1 → ta rf_d2 → tb	NOP
	NA
	NM
	S2
	S20
111 → rf_a1 rf_d1 → tc	NOP
	NA
	NM
	S20
	S22

tc → rf_d3 tb → PC,R7 ir[9:11] → rf_a3	NOP
	NA
	NM
	S22
	IB

17. JRI(J)

PC → mem_addr/alux_a mem_do → ir +1 → alux_b alux_c → PC	ADD
	IR
	NM
	S1(HKT)
	S23

ir[9:11] → rf_a1 rf_d1 → ta Ir[0:8] → SE9 → tb	NOP
	NA
	NM
	S23
	S3
ta → aluy_a tb → aluy_b aluy_c →ta	ADD
	mod c and z
	NA
	S3
	IB