EE309 Microprocessors Project - Multicycle RISC Design - IITB-RISC

Asif Shaikh - Roll: 20D070017
Jujhaar Singh - Roll: 200110052
Rohan Kalbag - Roll: 20D170033
Sankalp Bhamare - Roll: 200110096

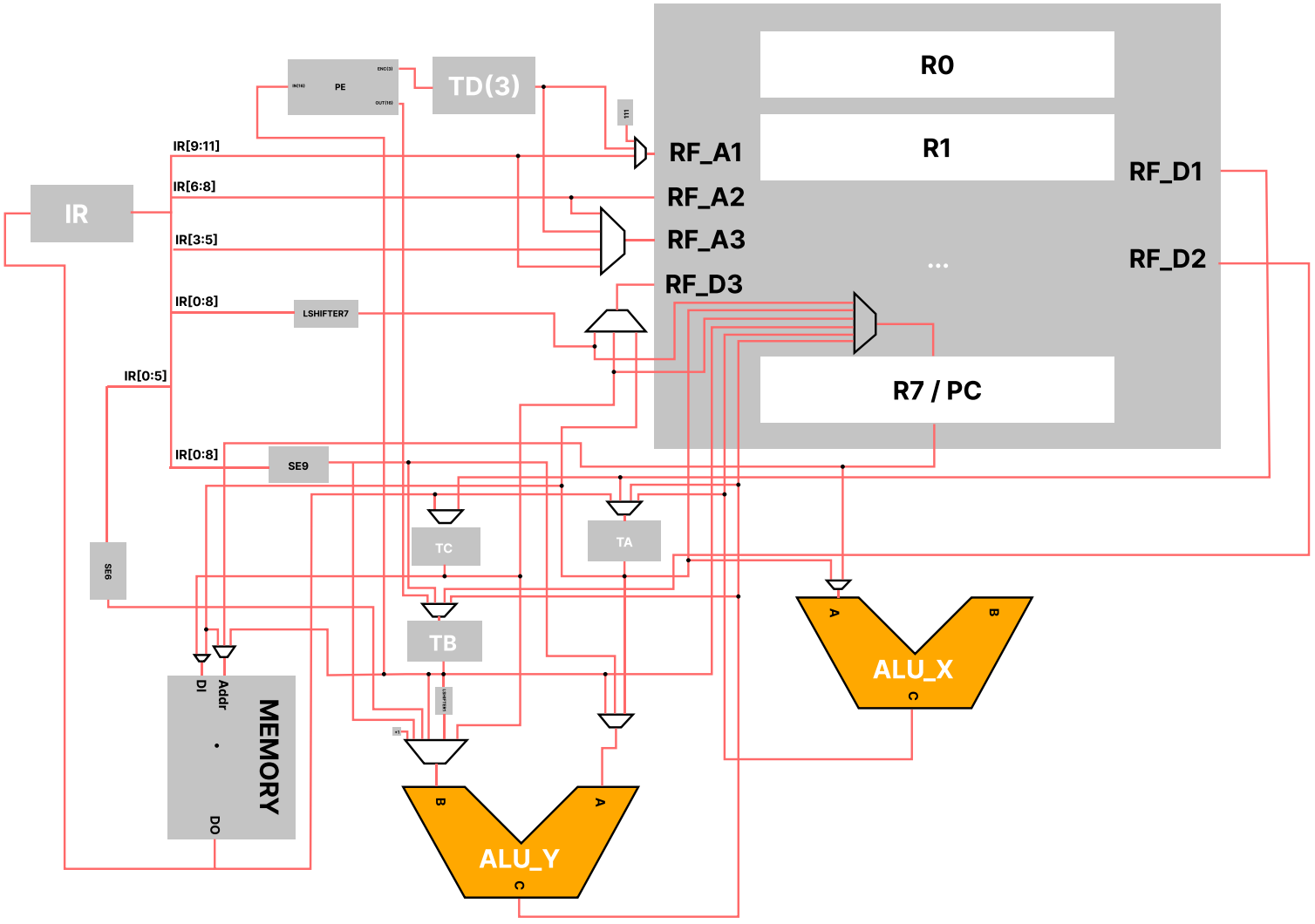
April 2022

The problem statement can be found in `Multicycle Problem Statement.pdf`.

The datapath consists of Two 16 bit ALUs, One 16 bit priority encoder that gives a 16 bit output and 3bit register address. There are two Sign Extenders SE6 and SE9 for 6 and 9 bit inputs giving 16 bit outputs. There are two left bit shifters Lshifter7 and Lshifter1 which respectively shift the input by 7 and 1 bit (s) to the left appending 0s to the right giving a 16 bit output. There are four temporary registers TA, TB, TC, TD, where TA, TB and TC are 16bit and TD is 3bit.

The instructions and information regarding the 27 states of the FSM can be found in the file `FSM States.pdf` and the state transition flows of the Finite State Machine can be found in the file `State Transition Diagram.pdf`. The control decode logic for each instruction can be found in the file `Decoding Logic.pdf`. The control words for each of the states can be found in the file `Control Words.pdf`

The project folder also has attached the hardware descriptions of the various components in VHDL. The toplevel entity contains the Datapath and the FSM. *GHDL* and *GTKWave* were used to test and debug all the various instructions. Screenshots of the wave viewer(GTKWave) are placed in the `waveforms` folder. The instructions listed in `waves.txt` were run by placing them in memory and the waveforms were captured.


R0
R1
...
R7 / PC
RF_A1
RF_A2
RF_A3
RF_D3
RF_D1
RF_D2
IR
IR[9:11]
IR[6:8]
IR[3:5]
IR[0:8]
IR[0:5]
IR[0:8]
PE
TD(3)
LSHIFTER7
SE9
SE6
TC
TA
TB
MEMORY
Addr
DI
DO
ALU_X
ALU_Y
A
B
C