Component	Instructions	No of Bits Needed	Encoding
TB_EN	Disable Write	1	0
	Enable Write		1
Memory	Ta -> mem_di	1	0
	Tc -> mem_di		1
	Ta -> mem_addr	2	00
	pc -> mem_addr, alux_a		01
	Tb -> mem_addr		10
	NA	2	00
	DR		01
	DW		10
RB	NA	2	00
	ir[9:11] -> rf_a1		01
	Td -> rf_a1		10
	111 -> rf_a1		11
	ir[6:8] -> rf_a3	2	00
	Td -> rf_a3		01
	ir[3:5] -> rf_a3		10
	ir[9:11] -> rf_a3		11
	ir[6:8] -> rf_a2	0	
	None	2	00
	Ta -> rf_d3		01
	Tc -> rf_d3		10
	LS7 -> rf_d3		11
aluy	NA	2	00
	Ta -> aluy_a		01
	Tb -> aluy_a		10
	SE9 -> aluy_a		11
	SE6 -> aluy_b	3	000
	LS1 -> aluy_b		001
	SE9 -> aluy_b		010
	Tc -> aluy_b, rf_d3		011
	Tb -> aluy_b		100

	+1->aluy_b		101
	add op	2	00
	xor op		01
	nand op		10
	jmp op		11
	NM	2	00
	Z,C		01
	TZ		10
	Z		11
alux	Ta -> alux_a	1	0
	pc -> mem_addr, alux_a		1
PC	NA	3	000
	Ta -> pc		001
	LS7 -> pc		010
	Tc -> pc		011
	alux_c -> pc		100
	Tb -> pc		101
	aluy_c -> pc		110
TA	NA	3	000
	mem_do -> Ta		001
	rf_d1 -> Ta		010
	aluy_c -> Ta		011
	alux_c -> Ta		100
TB	aluy_c -> Tb	2	00
	rf_d2 -> Tb		01
	pe_out -> Tb		10
	SE9 -> Tb		11
TC	NA	2	00
	rf_d1 -> Tc		01
	mem_do -> Tc		10
TD	NA	1	0
	pe_enc -> Td		1
IR	NA	1	0
	mem_do -> ir		1

	NA: No Operation		