

by Andi

**INO-CNR / LENS**

Sheet: /bus connection/

File: bus\_connection.sch

**Title: FPGA buffer board**

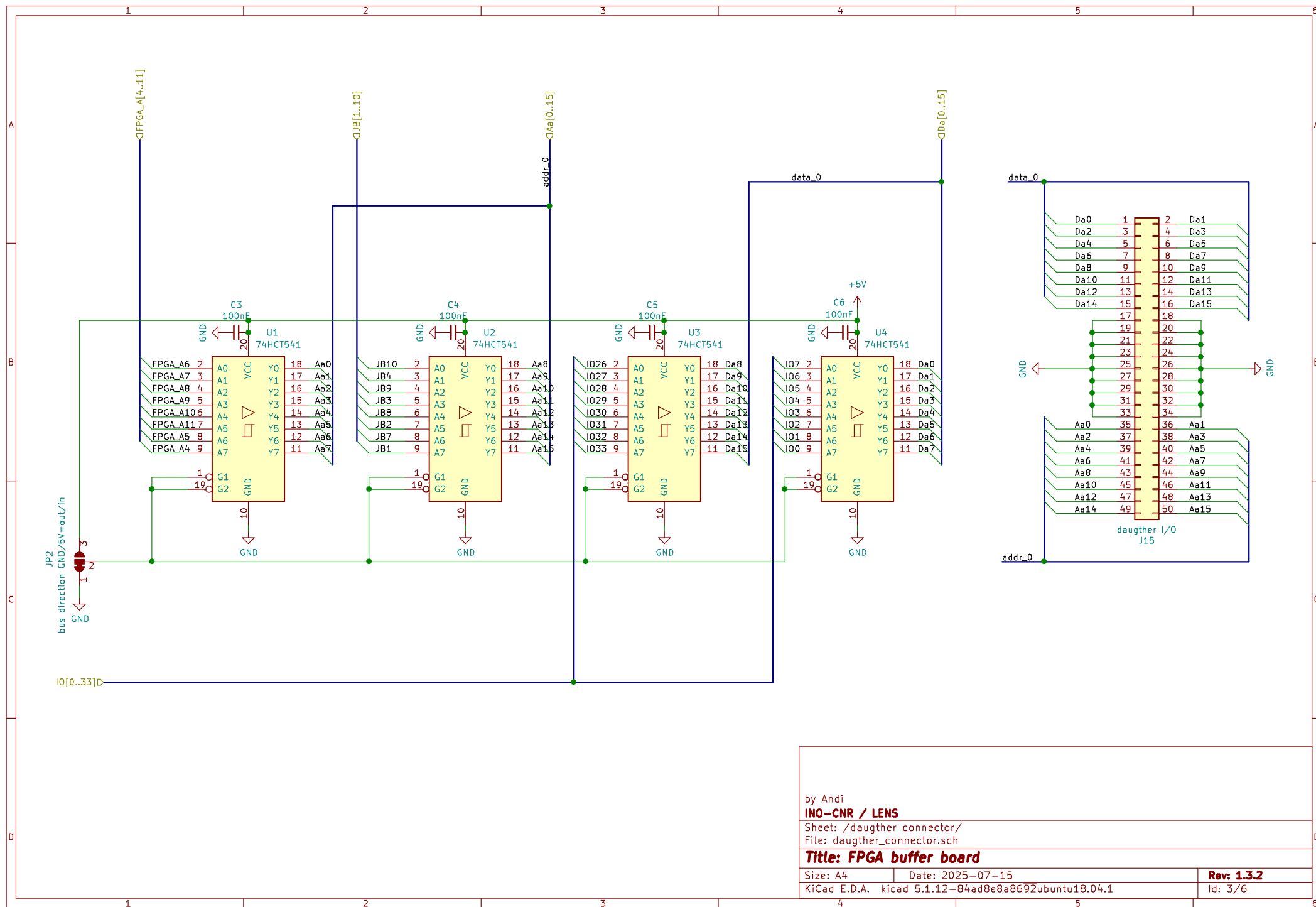
Size: A4

Date: 2025-07-15

**Rev: 1.3.2**

KiCad E.D.A. kicad 5.1.12-84ad8e8a8692ubuntu18.04.1

Id: 2/6



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**INO-CNR / LENS**

Sheet: /daughter connector/

File: daughter\_connector.sch

**Title: FPGA buffer board**

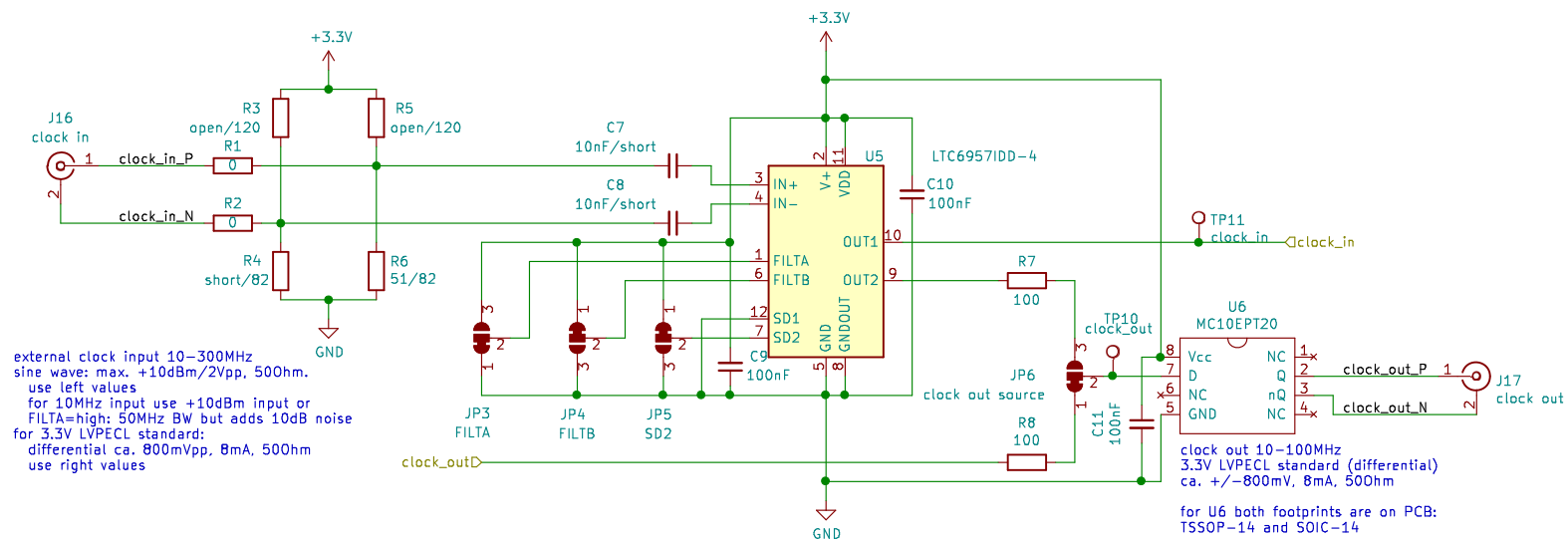
Size: A4

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KiCad E.D.A. kicad 5.1.12-84ad8e8a8692ubuntu18.04.1

**Rev: 1.3.2**

Id: 3/6



this design v1.3.2 uses CMOS output with DFN package:  
LTC6957IDD-3: 2x CMOS in-phase output)  
LTC6957IDD-4: 2x CMOS complementary output

design v1.3 uses CMOS output with MSOP package:  
LTC6957xMS-3: 2x CMOS in-phase output)  
LTC6957xMS-4: 2x CMOS complementary output

design v1.4 uses LVDS output with MSOP package:  
LTC6957xMS-2: 1x LVDS output

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Sheet: /external clock and triggers/

File: ext\_clock\_trigger.sch

**Title: FPGA buffer board**

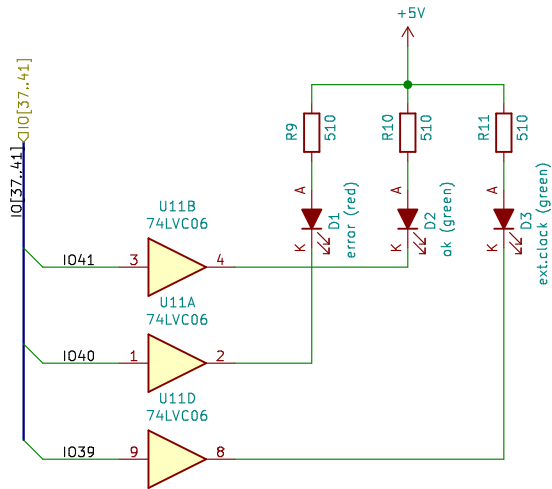
Size: A4

Date: 2025-07-15

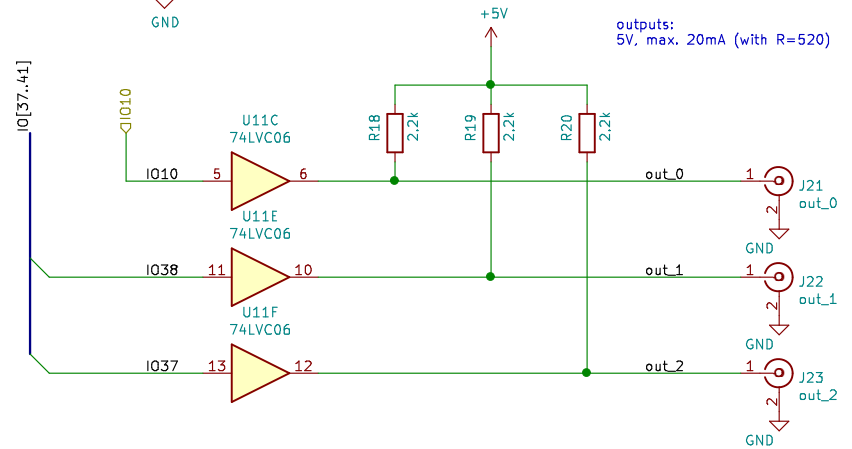
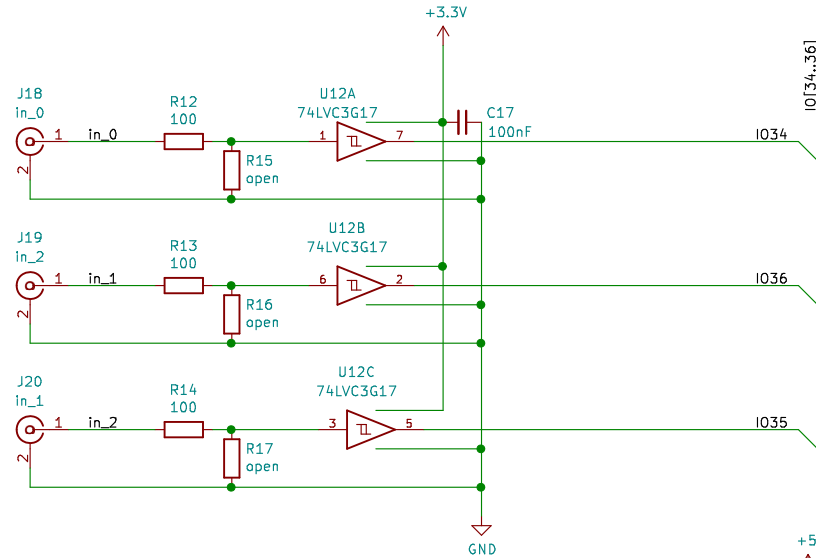
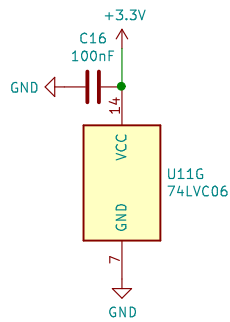
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external inputs:  
with Schmidt-Trigger  
3,2–5.5V, 1MΩhm  
high >1.9V, low <0.8V  
hysteresis 0.6–0.9V  
prop. delay 4–7ns



outputs:  
5V, max. 20mA (with R=520)

optional pin compatible output buffers  
74LVC06 is inverting  
74LCV07 is non-inverting

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Sheet: /IO\_buffer/

File: IO\_buffer.sch

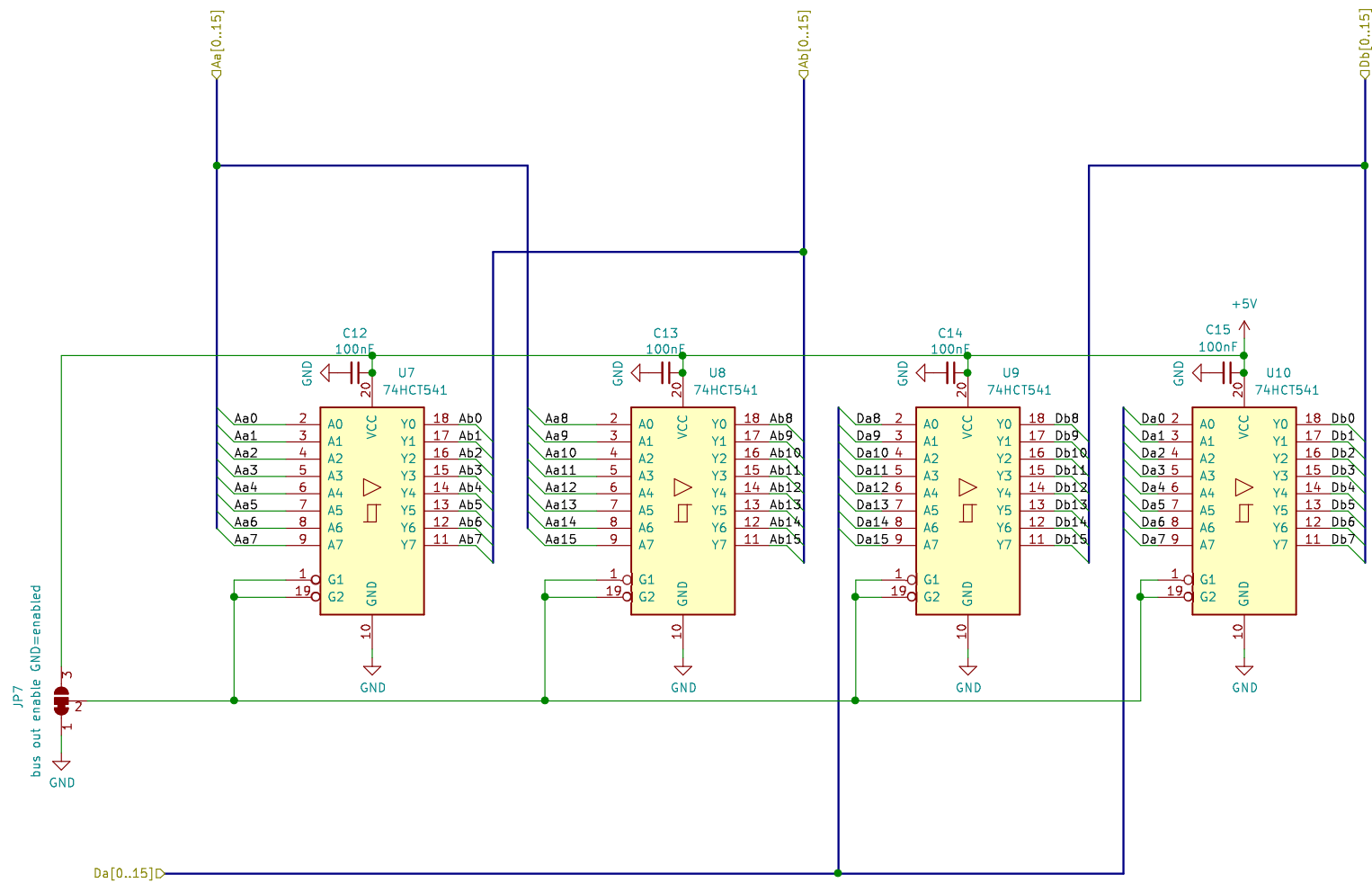
**Title: FPGA buffer board**

Size: A4 Date: 2025-07-15

KiCad E.D.A. kicad 5.1.12-84ad8e8a8692ubuntu18.04.1

**Rev: 1.3.2**

Id: 5/6



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**INO-CNR / LENS**

Sheet: /bus\_buffer/

File: bus\_buffer.sch

**Title: FPGA buffer board**

Size: A4

Date: 2025-07-15

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