Conception Electronique pour le Traitement de l'Information Julien VILLEMEJANE / LEnsE / Institut d'Optique Graduate School

5N-027-SCI / CéTI

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200.1

BLOC 1 / CAPTEURS ET MISE EN FORME

Mission 1 - Abaisser une tension

Proposer un circuit permettant d'abaisser une tension d'un facteur k. 0 < k < 1

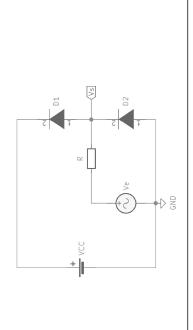
Iission 2 - Élever une tension

Proposer un circuit permettant d'élever une tension d'un facteur k.

Mission 3 - Limiter une tension

Rappeler le fonctionnement d'une diode.

Décrire le fonctionnement du montage suivant :



Mission 4 - Amplifier un signal

Proposer un circuit permettant d'amplifier un signal de 27dB, tout en garantissant une bande-passante de 400kHz.

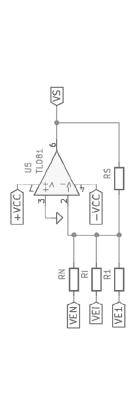
On utilisera des amplificateurs linéaires intégrés de type TL071 (documentation partielle donnée en annexe).

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Bloc 1 / Capteurs et mise en forme

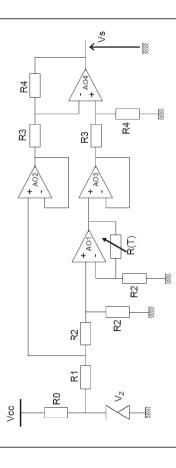
Mission 5 - Additionner des signaux

On se propose d'étudier le circuit suivant :



ssion 6 - Mettre en forme un capteur de températur

On se propose d'étudier le circuit suivant :



La thermistance utilisée est de type PT100. La relation entre sa résistance (en Ohms) et la température (en $^{\circ}$ C) est la suivante :

$$R(T) = 100\ (1 + 3.90810^{-3}T - 5.80210^{-7}T^2)$$

Une partie de la documentation de diodes Zener est fournie en annexe.





Tools & Software

Support & Community

SLOS0811-FEBRUARY 1977-REVISED MAY 2015

TL081, TL081A, TL081B, TL082, TL082A TL082B, TL084, TL084A, TL084B

TL08xx JFET-Input Operational Amplifiers

3 Description

Features

TEXAS INSTRUMENTS

- Low Power Consumption: 1.4 mA/ch Typical
- Wide Common-Mode and Differential Voltage

designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and

The devices feature high slew rates, low input bias

offset-voltage

and low

and offset currents, temperature coefficient.

bipolar transistors in a monolithic integrated circuit.

The TL08xx JFET-input operational amplifier family is

- Low Input Bias Current: 30 pA Typical
- Low Input Offset Current: 5 pA Typical
- Low Total Harmonic Distortion: 0.003% Typical Output Short-Circuit Protection
- High Input Impedance: JFET Input Stage
- Latch-Up-Free Operation
- Common-Mode Input Voltage Range High Slew Rate: 13 V/µs Typical Includes V_{CC+}

Applications 2

- Tablets
- White goods
- Personal electronics
- Computers

19.56 mm × 6.92 mm

19.3 mm × 6.35 mm 10.3 mm × 5.3 mm 5.0 mm × 4.4 mm

BODY SIZE (NOM) 8.89 mm × 8.89 mm 8.65 mm × 3.91 mm

PACKAGE

PART NUMBER

SOIC (14) LCCC (20) CDIP (14) PDIP (14) SO (14)

TL08xxFK

TL084xD TL084xJ TL084xN

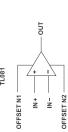
Device Information⁽¹⁾

For all available packages, see the orderable addendum at the end of the data sheet.

TSSOP (14)

TL084xPW

TL084xNS



(EACH AMPLIFIER)	(EACH AMPLIFIER)	
TL082 (TL084 (

Schematic Symbol

OUT

± ½

P



TL081, TL081A, TL081B, TL082, TL082A TL082B, TL084, TL084A, TL084B

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

				MIN	MAX	UNIT
^ ^	0				18	>
Voc	Supply voltage				-18	>
VID	Differential input voltage ⁽³⁾				∓30	>
>	Input voltage ⁽²⁾⁽⁴⁾				±15	>
	Duration of output short circuit®			Unlimited		
	Continuous total power dissipation			See Dissipation Rating Table	ng Table	
			TL08_C TL08_AC TL08_BC	0	02	
[∠]	Operating free-air temperature		TL08_I	-40	85	ပ္
			TL084Q	-40	125	
			TL08_M	-55	125	
	Operating virtual junction temperature	Ire			150	ပ္
Tc	Case temperature for 60 seconds	FK package	TL08_M		260	ပ္
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	J or JG package	TL08_M		300	ပ္
Tstg	Storage temperature			-65	150	၁

- (1) Stresses beyond those isted under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functionate operation of the device at these or any other conditions beyond those and indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

 All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC}.

 (3) Differential voltages are at IN+, with respect to IN
 (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

 (5) The output may be abrinded to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ESD Ratings 6.2

TINO		>
VALUE	1000	1500
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Charged-device model (CDM), per JEDEC specification JESD22-C101 $^{(2)}$
		Electrostatic discharge
		V(ESD)

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. £8

Recommended Operating Conditions 6.3

over operating free-air temperature range (unless otherwise noted)

MAX UNIT

Z

V _{CC+}	Supply voltage		2	15	>
V _{CC} -	Supply voltage		9-	-15	>
V _{CM}	Common-mode voltage		V _{CC} + 4 V _{CC+} - 4	V _{CC+} - 4	>
		TL08xM	99-	125	
H	A see the second second the second se	TL08xQ	04-	125	ç
∢	Ambient temperature	TL08xI	04-	85	ט
		TL08xC	0	70	

A IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications,

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Product Folder Links: 7L081 7L081A 7L081B 7L082 7L082A 7L082B 7L084 7L084B



TL081, TL081A, TL081B, TL082, TL082A TL082B, TL084, TL084A, TL084B

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Electrical Characteristics for TL08xC, TL08xC, and TL08xI (continued)

 $V_{\text{CC}\pm} = \pm 15 \text{ V}$ (unless otherwise noted)

PARAMETER	TEST	T _A (1)	TL08	L081C, TL082C, TL084C	32C,	TL081/	TL081AC, TL082AC, TL084AC	32AC,	TL081B TL	TL081BC, TL082BC, TL084BC	2BC,	TL08	L0811, TL0821, TL0841	21,	FIND
	CONDITIONS		N	ТУР	MAX		MIN TYP MAX	MAX	MIN TYP MAX	TYP	MAX	M	ΤΥP	MAX	
	$V_{O} = 0$, No load	25°C		4.1	2.8		4.1	2.8		1.4	2.8		4.1	2.8	mA
	A _{VD} = 100	25°C		120			120			120			120		eg B

Electrical Characteristics for TL08xM and TL084x 9.9

V_{CC±} = ±15 V (unless otherwise noted)

				TI 00	TI DOUR TI DOOM	W	- I	MANOUIT CANONIT	-	
	DARAMETER	TEST CONDITIONS(1)	F	- Loc) IIVI, I L'002	IAI	IFOO	+€, 1 L004F		HNI
	NATI AMERICA		٧.	N	TYP	MAX	N	TYP	MAX	
,	land office to the sea	0	25°C		3	9		3	6	/*
01^	input oilset vorlage	Vo = 0, Ns = 30 12	Full range			6			15	È
Q/NO	Temperature coefficient of input offset voltage	V _O = 0, R _S = 50 Ω	Full range		18			18		hW°C
	(2)	0 -	25°C		2	100		2	100	ρĄ
Q	input oilset current	0=0	125°C			20			20	ΡV
_	learnt bion or monet (2)	0	25°C		30	200		30	200	ΡĄ
9	input plas cuitent	0 - 0	125°C			20			20	ΡV
VICR	Common-mode input voltage range		25°C	±11	-12 to 15		±11	-12 to 15		>
		$R_L = 10 \text{ k}\Omega$	25°C	±12	±13.5		±12	±13.5		
VoM	Maximum peak	R _L ≥ 10 kΩ	17.0	±12			±12			>
	0	R _L ≥ 2 kΩ	ruii range	±10	±12		±10	±12		
<	Large-signal differential	V = +40 V = × 2 V	25°C	25	200		25	200		//ma///
Q/v	voltage amplification	VO = ± 10 V, NL = 2 NS	Full range	15			15			A
B ₁	Unity-gain bandwidth		25°C		3			3		MHz
_	Input resistance		25°C		1012			1012		а
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR} min$, $V_O = 0$, $R_S = 50 \Omega$	25°C	80	98		80	98		В
Ksvr	Supply-voltage rejection ratio (∆V _{CC±} /∆V _{IO})	V_{CC} = ±15 V to ±9 V, V_{O} = 0, R_{S} = 50 Ω	25°C	80	98		80	98		용
8	Supply current (each amplifier)	$V_{O} = 0$, No load	25°C		1.4	2.8		4.1	2.8	mA
Vo ₁ No ₂	Crosstalk attenuation	A _{VD} = 100	25°C		120			120		В

All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified input bias currents of a FET-input operational manifiler are normal jurction revere currents, which are temperature sastitive, as shown in Figure 1.3. Pulse techniques must be used that maintain the jurdion remperatures as close to the ambient temperature as possible.

Operating Characteristics 6.7

= ±15 V. T_A= 25°C (unless otherw

*CC± = ±10 *, 1A ≥0 0 (alloco outolwice iloco)	Owice Head					
PARAMETER	TEST CONDITIONS	NΕ	ТҮР	MAX	LIND	
	$V_I = 10 \text{ V}$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Figure 19	8(1)	13			
Slew rate at unity gain	$V_1 = 10 \text{ V}$, $R_L = 2 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, $T_A = -55^{\circ}\text{C}$ to 125°C , S_{con} Final 10	5(1)			N/us	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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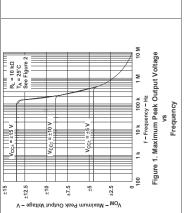
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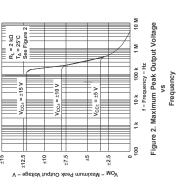
6.9 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in Parameter Measurement Information.

Table 1. Table of Graphs

			Figure
Vom	Maximum peak output voltage	versus Frequency versus Freear fremperature versus Load resistance versus Supply voltage	Figure 1, Figure 2, Figure 3 Figure 4 Figure 5 Figure 6
<	Large-signal differential voltage amplification	versus Free-air temperature versus Load resistance	Figure 7 Figure 8
Q _V	Differential voltage amplification	versus Frequency with feed-forward compensation	Figure 9
P_D	Total power dissipation	versus Free-air temperature	Figure 10
lcc	Supply current	versus Free-air temperature versus Supply voltage	Figure 11 Figure 12
l _B	Input bias current	versus Free-air temperature	Figure 13
	Large-signal pulse response	versus Time	Figure 14
Vo	Output voltage	versus Elapsed time	Figure 15
CMRR	Common-mode rejection ratio	versus Free-air temperature	Figure 16
\ v	Equivalent input noise voltage	versus Frequency	Figure 17
THD	Total harmonic distortion	versus Frequency	Figure 18





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1N4728A to 1N4761A

Vishay Semiconductors

Zener Diodes



FEATURES

Silicon planar power Zener diodes

Z

- · For use in stabilizing and clipping circuits with high power rating
- Standard Zener voltage tolerance is \pm 5 %
- for definitions of compliance please see Material categorization:

ROHS COMPLIANT HALOGEN

LINKS TO ADDITIONAL RESOURCES

www.vishay.com/doc?99912

APPLICATIONS

Voltage stabilization

PRIMARY CHARACTERISTICS	CTERISTICS	
PARAMETER	VALUE	TINO
V _z range nom.	3.3 to 75	>
Test current IzT	3.3 to 76	mA
V ₂ specification	Thermal equilibrium	
Circuit configuration	Single	

ORDERING INFORMATION	MATION		
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL	MINIMUM ORDER QUANTITY
1N4728A to 1N4761A	1N4728A to 1N4761A -series-TR	5000 per 13" reel	25 000/box
1N4728A to 1N4761A	1N4728A to 1N4761A-series-TAP	5000 per ammopack (52 mm tape)	25 000/box

			(52 IIIII tape)	
PACKAGE				
PACKAGE NAME	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
DO-41 (DO-204AL)	310 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATING	ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25$ °C, unless otherwise specified)	cified)		
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Power dissipation	Valid provided that leads at a distance of 4 mm from case are kept at ambient temperature	P _{tot}	1300	wm
Zener current		ZI	P _v /V _z	mA
Thermal resistance junction to ambient air	Thermal resistance junction to ambient air from case are kept at ambient temperature	RthJA	110	K/W
Junction temperature		T _j	175	ပ္
Storage temperature range		Tstg	-65 to +175	၁့
Forward voltage (max.)	I _F = 200 mA	VF	1.2	^

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1N4728A to 1N4761A

Vishay Semiconductors

ELECTRIC/	ELECTRICAL CHARACTERISTICS ($I_{amb} = 25 {}^{\circ}\mathrm{C}$, unless otherwise specified)	35	amp =	5	000	1			
FOAG	ZENER VOLTAGE RANGE (1)	CUR	TEST	REVERSE	REVERSE LEAKAGE CURRENT	DYN. RESIS	DYNAMIC RESISTANCE f = 1 kHz	SURGE CURRENT (3)	REGULATOR CURRENT (2)
NUMBER	V ₂ at I _{2T1}	ZT	ZTZ	l a	I _R at V _R	Zzr at Izrı	Zzr at Izrı Zzk at Izr2	<u>"</u>	MZ
	>	ш	mA	γr	>	, ,	g	mA	mA
	NOM.			MAX.		TYP.	MAX.		MAX.
1N4728A	3.3	9/	-	100	-	10	400	1380	276
1N4729A	3.6	69	-	100	-	10	400	1260	252
1N4730A	3.9	64	-	20	-	6	400	1190	234
1N4731A	4.3	28	-	10	-	0	400	1070	217
1N4732A	4.7	53	-	10	-	∞	200	970	193
1N4733A	5.1	49	-	10	-	7	550	890	178
1N4734A	5.6	45	-	10	2	22	009	810	162
1N4735A	6.2	41	-	10	က	2	700	730	146
1N4736A	6.8	37	-	10	4	3.5	700	099	133
1N4737A	7.5	34	0.5	10	5	4	700	909	121
1N4738A	8.2	31	0.5	10	9	4.5	700	550	110
1N4739A	9.1	28	0.5	10	7	5	700	200	100
1N4740A	10	25	0.25	10	9.7	7	700	454	91
1N4741A	11	23	0.25	2	8.4	80	700	414	83
1N4742A	12	21	0.25	2	9.1	6	700	380	92
1N4743A	13	19	0.25	2	6.6	10	700	344	69
1N4744A	15	17	0.25	2	11.4	14	200	304	61
1N4745A	16	15.5	0.25	2	12.2	16	200	285	57
1N4746A	18	14	0.25	2	13.7	20	750	250	90
1N4747A	20	12.5	0.25	2	15.2	22	750	225	45
1N4748A	22	11.5	0.25	2	16.7	23	750	205	41
1N4749A	24	10.5	0.25	2	18.2	25	750	190	38
1N4750A	27	9.5	0.25	2	20.6	35	750	170	34
1N4751A	30	8.5	0.25	2	22.8	40	1000	150	30
1N4752A	33	7.5	0.25	2	25.1	45	1000	135	27
1N4753A	36	7	0.25	2	27.4	90	1000	125	25
1N4754A	39	6.5	0.25	2	29.7	09	1000	115	23
1N4755A	43	9	0.25	2	32.7	70	1500	110	22
1N4756A	47	5.5	0.25	2	35.8	80	1500	98	19
1N4757A	51	2	0.25	2	38.8	92	1500	06	18
1N4758A	56	4.5	0.25	2	42.6	110	2000	80	16
1N4759A	62	4	0.25	2	47.1	125	2000	70	14
1N4760A	89	3.7	0.25	2	51.7	150	2000	65	13
1N4761A	75	3.3	0.25	2	56	175	2000	09	12

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⁽¹⁾ Based on DC measurement at thermal equilibrium while maintaining the lead temperature (T_L) at 30 °C + 1 °C, 9.5 mm (3/8") from the

diode body (2) Valid provided that electrodes at a distance of 4 mm from case are kept at ambient temperature (3) $t_{\rm p}=10$ ms.