











TL081, TL081A, TL081B, TL082, TL082A TL082B, TL084, TL084A, TL084B

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TL08xx JFET-Input Operational Amplifiers

Features

- Low Power Consumption: 1.4 mA/ch Typical
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias Current: 30 pA Typical
- Low Input Offset Current: 5 pA Typical
- **Output Short-Circuit Protection**
- Low Total Harmonic Distortion: 0.003% Typical
- High Input Impedance: JFET Input Stage
- Latch-Up-Free Operation
- High Slew Rate: 13 V/µs Typical
- Common-Mode Input Voltage Range Includes V_{CC+}

Applications

- **Tablets**
- White goods
- Personal electronics
- Computers

3 Description

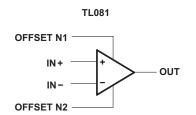
The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias offset currents, and low offset-voltage temperature coefficient.

Device Information⁽¹⁾

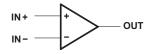
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL084xD	SOIC (14)	8.65 mm × 3.91 mm
TL08xxFK	LCCC (20)	8.89 mm × 8.89 mm
TL084xJ	CDIP (14)	19.56 mm × 6.92 mm
TL084xN	PDIP (14)	19.3 mm × 6.35 mm
TL084xNS	SO (14)	10.3 mm × 5.3 mm
TL084xPW	TSSOP (14)	5.0 mm × 4.4 mm

⁽¹⁾ For all available packages, see the orderable addendum at the end of the data sheet.

Schematic Symbol



TL082 (EACH AMPLIFIER) TL084 (EACH AMPLIFIER)





6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

				MIN	MAX	UNIT	
V _{CC+}	Supply valtage (2)				18	V	
V _{CC} -	Supply voltage -	upply voltage ⁽²⁾					
V_{ID}	Differential input voltage (3)		±30	V			
VI	Input voltage (2)(4)		±15	V			
	Duration of output short circuit (5)			Unlim	ited		
	Continuous total power dissipation	See Dissipation	Rating Table				
			TL08_C TL08_AC TL08_BC	0	70		
T _A	Operating free-air temperature		TL08_I	-40	85	°C	
			TL084Q	-40	125		
			TL08_M	- 55	125		
	Operating virtual junction temperat	ure			150	°C	
T _C	Case temperature for 60 seconds	FK package	TL08_M		260	°C	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	J or JG package	TL08_M		300	°C	
T _{stg}	Storage temperature			-65	150	°C	

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
- (3) Differential voltages are at IN+, with respect to IN-.
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	1000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC+}	Supply voltage		5	15	V
V _{CC} -	Supply voltage		-5	-15	V
V_{CM}	Common-mode voltage		V _{CC} - + 4	V _{CC+} – 4	V
	Ambient temperature	TL08xM	-55	125	
_		TL08xQ	-40	125	°C
T _A		TL08xI	-40	85	
		TL08xC	0	70	

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⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



Electrical Characteristics for TL08xC, TL08xxC, and TL08xI (continued)

 $V_{CC\pm} = \pm 15 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A ⁽¹⁾	TL081C, TL082C, TL084C		TL081AC, TL082AC, TL084AC		TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT		
		CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I _{CC}	Supply current (each amplifier)	V _O = 0, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V _{O1} /V _{O2}	Crosstalk attenuation	A _{VD} = 100	25°C		120			120			120			120		dB

6.6 Electrical Characteristics for TL08xM and TL084x

 $V_{CC+} = \pm 15 \text{ V}$ (unless otherwise noted)

	DADAMETED	TEST CONDITIONS(1)	-	TLO	081M, TL082	2M	TL0	84Q, TL08	4M	UNIT
	PARAMETER	TEST CONDITIONS ⁽¹⁾	T _A	MIN	TYP	MAX	MIN	TYP	MAX	UNII
	Innut offeet valtege	V 0. B 50.0	25°C		3	6		3	9	\/
V_{IO}	Input offset voltage	$V_{O} = 0, R_{S} = 50 \Omega$	Full range			9			15	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_{O} = 0, R_{S} = 50 \Omega$	Full range		18			18		μV/°C
	Input offset current ⁽²⁾	V 0	25°C		5	100		5	100	pА
I _{IO}	input offset current(=)	V _O = 0	125°C			20			20	nA
	Input bias current(2)	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	25°C		30	200		30	200	pА
I _{IB}	input bias current	V _O = 0	125°C			50			50	nA
V _{ICR}	Common-mode input voltage range		25°C	±11	-12 to 15		±11	-12 to 15		V
		$R_L = 10 \text{ k}\Omega$	25°C	±12	±13.5		±12	±13.5		
V_{OM}	Maximum peak output voltage swing	R _L ≥ 10 kΩ	F. II	±12			±12			V
	output voltage swilig	R _L ≥ 2 kΩ	Full range	±10	±12		±10	±12		
^	Large-signal differential	$V_{\Omega} = \pm 10 \text{ V}, R_{\parallel} \ge 2 \text{ k}\Omega$	25°C	25	200		25	200		V/mV
A_{VD}	voltage amplification	$V_0 = \pm 10 \text{ V}, R_L \ge 2 \text{ K}\Omega$	Full range	15			15			V/IIIV
B ₁	Unity-gain bandwidth		25°C		3			3		MHz
r _i	Input resistance		25°C		10 ¹²			10 ¹²		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min,$ $V_O = 0, R_S = 50 \Omega$	25°C	80	86		80	86		dB
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	$V_{CC} = \pm 15 \text{ V to } \pm 9 \text{ V},$ $V_{O} = 0, R_{S} = 50 \Omega$	25°C	80	86		80	86		dB
I _{CC}	Supply current (each amplifier)	V _O = 0, No load	25°C		1.4	2.8		1.4	2.8	mA
V _{O1} /V _{O2}	Crosstalk attenuation	A _{VD} = 100	25°C		120			120		dB

⁽¹⁾ All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

6.7 Operating Characteristics

 $V_{CC\pm} = \pm 15 \text{ V}, T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR		V_I = 10 V, R_L = 2 k Ω , C_L = 100 pF, See Figure 19	8 ⁽¹⁾	13		
		V_I = 10 V, R_L = 2 k Ω , C_L = 100 pF, T_A = - 55°C to 125°C, See Figure 19	5 ⁽¹⁾			V/µs

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

⁽²⁾ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 13. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

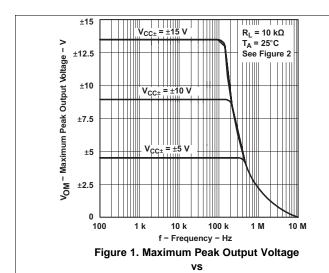


6.9 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in *Parameter Measurement Information*.

Table 1. Table of Graphs

			Figure
V _{OM}	Maximum peak output voltage	versus Frequency versus Free-air temperature versus Load resistance versus Supply voltage	Figure 1, Figure 2, Figure 3 Figure 4 Figure 5 Figure 6
٨	Large-signal differential voltage amplification	versus Free-air temperature versus Load resistance	Figure 7 Figure 8
A _{VD}	Differential voltage amplification	versus Frequency with feed-forward compensation	Figure 9
P _D	Total power dissipation	versus Free-air temperature	Figure 10
Icc	Supply current	versus Free-air temperature versus Supply voltage	Figure 11 Figure 12
I _{IB}	Input bias current	versus Free-air temperature	Figure 13
	Large-signal pulse response	versus Time	Figure 14
Vo	Output voltage	versus Elapsed time	Figure 15
CMRR	Common-mode rejection ratio	versus Free-air temperature	Figure 16
V _n	Equivalent input noise voltage	versus Frequency	Figure 17
THD	Total harmonic distortion	versus Frequency	Figure 18



Frequency

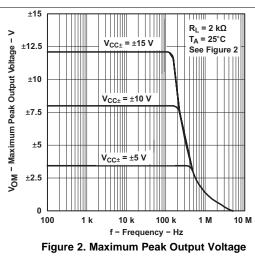


Figure 2. Maximum Peak Output Voltage vs
Frequency