IOB-SoC

A RISC-V-based System on Chip

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Introduction

- Building processor-based systems from scratch is challenging
- The IOB-SoC template eases this task
- Provides a base Verilog SoC equipped with
  - a RISC-V CPU
  - a memory system including boot ROM, RAM and AXI4 interface to DDR
  - a UART communications module
- Users can add IP cores and software to build more complex SoCs
- Here, the addition of a timer IP and its software driver is exemplified

Project setup

- Use a Linux machine or VM
- Install the latest stable version of the open source Icarus Verilog simulator (iverilog.icarus.com)
- Make sure you can access github.com using an ssh key
- Clone the repository github.com/IObundle/iob-soc
- Follow the instructions in its the README file

Create an IP core to instantiate in your SoC

- Create a timer IP core repository or, alternatively, use the one at www.github.com/IObundle/iob-timer.git
- An IP core can be integrated in an IOb-SoC if it provides the following X files:
  1. hardware/hardware.mk
  2. software/software.mk
     - Please refer to the files `hardware/hardware.mk` and `software/software.mk` in the iob-timer submodule to learn how to organize a peripheral core.
- Add the IP core repository as a git submodule of your IOb-SoC repository:

```
git submodule add https://github.com/IObundle/iob-timer.git submodules/TIMER
```

- To configure the system to host the IP core, edit the `./system.mk` file as in the next slide

Edit the ./system.mk configuration file to configure the system with a new peripheral

```
#FIRMWARE
FIRM_ADDR_W:=13

#SRAM
SRAM_ADDR_W=13

#DDR
ifeq ($(USE_DDR),)
USE_DDR:=0
endif
ifeq ($(RUN_DDR),)
RUN_DDR:=0
endif

DDR_ADDR_W:=30
CACHE_ADDR_W:=24

#ROM
BOOTROM_ADDR_W:=12

#Init memory (only works in simulation or FPGA not running DDR)
ifeq ($(INIT_MEM),)
INIT_MEM:=1
endif

#Peripheral list (must match respective submodule name)
PERIPHERALS:=UART TIMER

...
```

Edit the firmware.c file to drive the new peripheral

./software/firmware/firmware.c

```
#include "system.h"
#include "periphs.h"
#include "iob-uart.h"
#include "iob_timer.h"

int main()
{
  unsigned long long elapsed;
  unsigned int elapsedu;

  //read current timer count, compute elapsed time
  elapsed = timer_get_count(TIMER_BASE);
  elapsedu = timer_time_us(TIMER_BASE);

  //init uart
  uart_init(UART_BASE, FREQ/BAUD);

  uart_printf("\nHello world!\n");

  uart_txwait();

  uart_printf("\nExecution time: %d clocks in %dus @%dMHz",
              (unsigned int)elapsed, elapsedu, FREQ/1000000);

  uart_txwait();
  return 0;
}
```

Run the firmware in internal SRAM

1. Initialize the internal RAM with the firmware
   - Define `USE_DDR=0` and `INIT_MEM=1`
   - Works in simulation and FPGA
   - Loading programs after the FPGA is programmed is enabled: if the firmware is modified it is automatically recompiled
2. Do not initialize the internal RAM with the firmware
   - Assign `USE_DDR=0 INIT_MEM=0`
   - Works in simulation, FPGA and ASIC
   - The firmware is (re)compiled and (re)loaded via UART

Run the firmware in external DDR

1. Initialize the DDR with the firmware
   - Define `USE_DDR=1` and `INIT_MEM=1`
   - Works in simulation only
   - In FPGA or ASIC the external DDR cannot be initialized
2. Do not initialize the DDR with the firmware
   - Define `USE_DDR=1 INIT_MEM=0`
   - This option is valid for simulation, FPGA and ASIC
   - The firmware is (re)compiled and (re)loaded via UART
   - In FPGA or ASIC a third party DDR controller IP core is required

Simulate IOb-SoC

- Add your simulation folder in `./hardware/simulation` using the other folders in there as examples
- In file `./system.mk`:
  1. Define `SIMULATOR` with the name of your simulation folder
  2. Define `SIM_SERVER` with the URL or IP address of the computer where the RTL simulator runs.
  3. Define `SIM_ROOT_DIR` with the name of the remote root directory for the repository files
- To run locally, do not define `SIM_SERVER` and `SIM_ROOT_DIR`
- To run the simulator, type `make` or `make USER=your_user_name` if you have a different username on the remote simulation server

Simulate IOb-SoC

- The firmware, bootloader and system verilog description are compiled as you can see from the printed messages
- During simulation the following is printed:

```
IOb-SoC Bootloader:

Reboot CPU and run program...

Hello world!

Execution time: 6583 clocks in 66us @100MHz
```

Implement in FPGA

- Add your FPGA folder in `./hardware/fpga` using the other folders in there as examples
- In file `./system.mk`:
  1. Define `FPGA_BOARD` with the name of your FPGA folder
  2. Define `FPGA_BOARD_SERVER` with the URL or IP address of the computer connected to the board
  3. Define ...
- To compile and load the hardware design in the FPGA, type `make fpga-load`
- To load and run your firmware in the FPGA, type `make run-firmware`

Implement in ASIC (WIP)

- Add your ASIC folder in `./hardware/asic` using the other folders in there as examples
- In the file `./system.mk`:
  1. Define `ASIC_NODE` with the name of your ASIC folder
  2. Define `ASIC_COMPILE_SERVER` with the URL or IP address of the computer connected to the node
  3. Add further server info such as username and work directories
- To compile the ASIC, type `make asic`

Conclusions and future work

- Conclusions
  - A tutorial on SoC creation using IOb-SoC is presented
  - The addition of a peripheral IP core (timer) is illustrated
  - A simple software driver for the IP core is exemplified
  - How to compile and run the system is explained
  - Options for implementing the main memory are presented
  - Implementation of FPGA and ASIC is explained
- Future work
  - Non-volatile (flash) external memory support
  - Real Time Operating System (RTOS)