Rhino - LORA ANT

Board with LORA antena

DIAGRAM
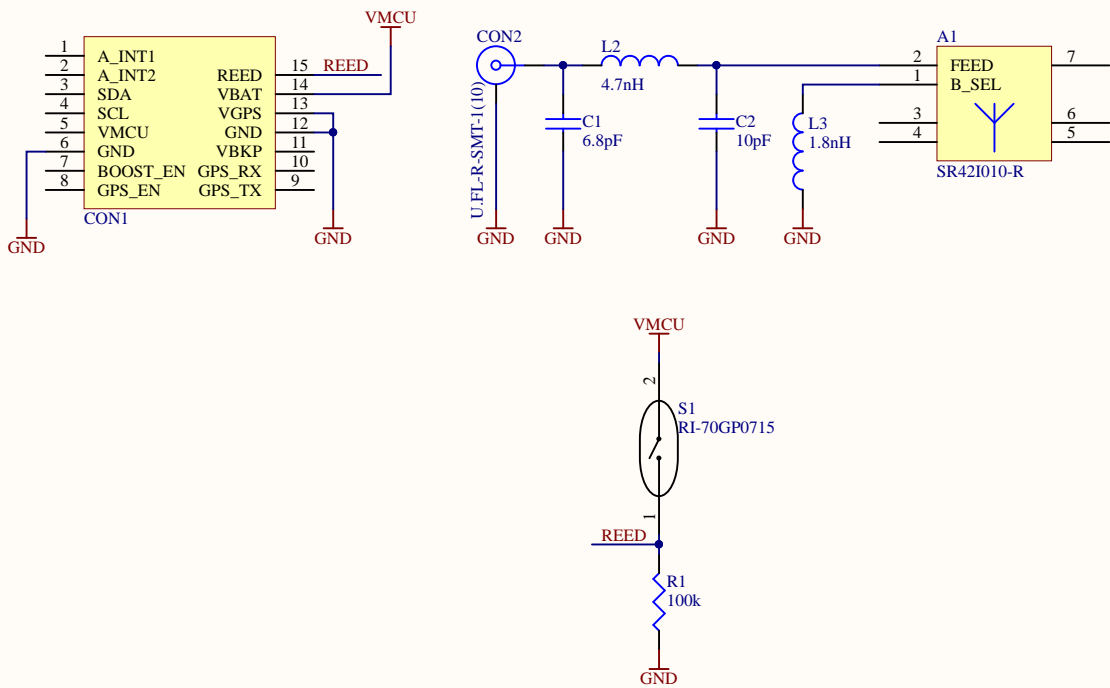
Version Revision:

V1   - dd.mm.yyyy

CON1

Pin	Signal	Signal	Pin
1	A_INT1		
2	A_INT2	REED	15
3	SDA	VBAT	14
4	SCL	VGPS	13
5	VMCU	GND	12
6	GND	VBKP	11
7	BOOST_EN	GPS_RX	10
8	GPS_EN	GPS_TX	9

VMCU

REED

GND

GND

CON2 — U.FL-R-SMT-1(10)

L2 4.7nH

C1 6.8pF

C2 10pF

L3 1.8nH

GND   GND   GND   GND

A1 — SR42I010-R

FEED
B_SEL

2   7
1
3   6
4   5

VMCU

S1
RI-70GP0715

REED

R1 100k

GND

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational
design notes.

DESIGN NOTE:
Example text for critical
design notes.

LAYOUT NOTE:
Example text for critical
layout guidelines.

IRNAS	URL

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Size: A3		Revision: V1
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