1) Consider the following Boolean expression:

$$F = \overline{\overline{d} + a} \cdot \overline{c + \overline{b}} \cdot \overline{\overline{d} + c}$$

a. Simplify the expression.

b. Design the circuit in CMOS logic

c. Construct a gate level of the same function only using NAND gates.

d. Why do we use NAND gates to implement digital logics?

2) Divide your student ID by 4 and the remainder is the new ID in the following table. Dismiss NOT gate propagation delay and if there are any gates with more than 4 input in your design, assume the delay as a delay of 4 input gate.

Delay	ID			
	0	1	2	3
TNAND2	1ns	2ns	1ns	1ns
TNAND3	2ns	3ns	3ns	2ns
TNAND4	3ns	5ns	5ns	4ns

Calculate total gate delay of a 32-bit Ripple Carry Adder.

Calculate total gate delay of a 32-bit Carry Look Ahead.

3) Answer the following questions:

a. What is FPGA? What is the difference of FPGA and microprocessor?

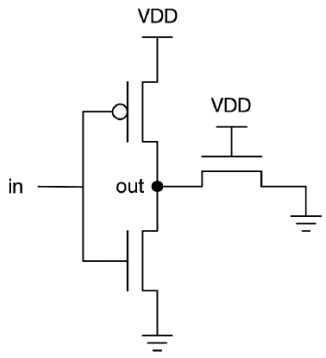
b. What is ASIC design?

c. What is VLSI (Very Large Scale Integration)?

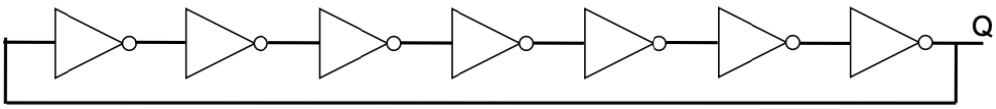
d. What are the common concepts between part a, b and c?

4) Using the transistor as a switch model, draw the voltage transfer characteristic for the circuit below.

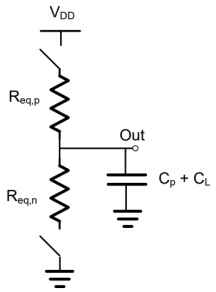
You will eventually recognize this as half of a 6T CMOS SRAM bit-cell. Assume that $|Vth\text{-}p| = Vth\text{-}n < VDD/2$ and that $Ron\text{-}p = Ron\text{-}n$.



5) By taking advantage of the fact that logic gates take some time to propagate changes in their input, we can build a simple ring oscillator (a circuit that switches back and forth between 0 and 1) from an odd number of inverters, as shown below. Suppose we use 7 inverters to do so.



For this question, we will use the model of a transistor as a resistor and a capacitor. Here is the diagram of an inverter under this model:



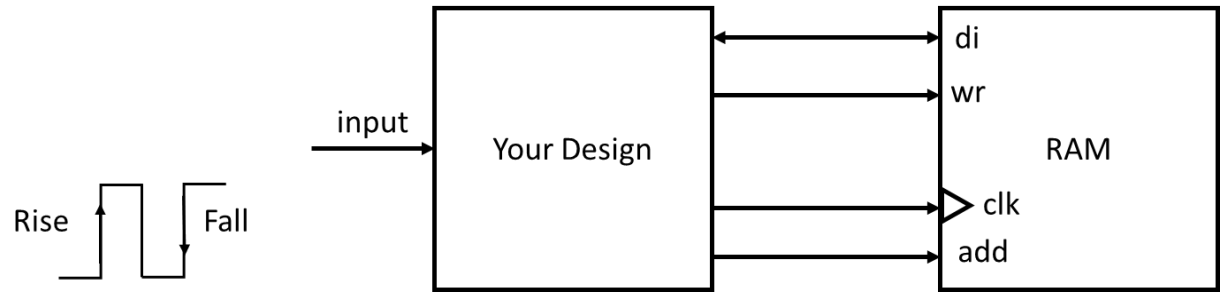
a. Say $Req\text{-}n = Req\text{-}p = 5m\Omega$ and $C_P = Cin = 2nF$. What is the propagation delay of an inverter in this design?

b. At what frequency will the output signal oscillate? Assume Q is not connected to anything outside the ring.

Bonus point) In the following setup, we would like to design a circuit which will fill 16 cells of a 16-cell RAM in every clock cycle.

$$for\ (i = 0; i < 16; i++)$$
$$d[i] = i;$$

On the rising edge of the clock, the data is going to be fetched and prepared and on the falling edge of the clock, data will be written on the memory and this process will last at 16 clocks. Also we'd like to stop writing on the other cells of RAM after the end of the 16 clocks (even with receiving new clock signal).



Why do we prepare data on rising edge and write on falling edge?

Draw a schematic for your design and write a brief explanation for it.

Please submit your homework, simulations and projects in the following format:

Name_StudentNumber_HW1 (BillGates_12345678_HW1)

Good Luck!