Pseudo Random Sequence (PRS) example project

3.0

Features

- Generation PRS input signals same as clock, reset.
- Hardware Reset generation for PRS_Clocked component.
- Software initialization for PRS_SingleStep component.
- Generation PRS sequence by both components with API Single Step and Clocked run modes
- Software PRS sequence calculation.
- Software and hardware PRS sequence on LCD are displayed.
- Possibility of the PRS Components input/output signals handling.

General Description

This example project demonstrates the PRS component with various Run Mode configuration (API Single Step and Clocked) operations. Software PRS calculation is executed for visual compare values. Hardware PRS calculations are displayed on the LCD step by step over defined (SEED_VALUE_COUNT – default is 20) steps. Software PRS calculation is displayed on the LCD at once.

Development kit configuration

1. This project is written for 2X16 display as the one available on Cypress kit CY8CKIT-001.
2. The PSoC3/5/5LP DVK CY8CKIT-001 boards besides default configuration should have LCD power jumper (J12).
3. Build the project and program the hex file on to the target device using MiniProg3.
4. Power cycle the device and observe the results on the LCD.

Project configuration

This project consists of two 16 bit PRS (in the Clocked and API Single Step Run Modes), two Control Registers, Character LCD components and four digital output pins. The top design schematic is shown in Figure 1. The Clock signal is generated by the control register

"Clock_Gen". The Reset signal is generated by the control register "Reset_Gen". All signals changes can observed on an oscillator or a signal analyzer at PORT0 [3:0] by default.

Software Defines on main.c file:

SEED_VALUE_COUNT - set number of PRS calculate iteration (20 by default);

DISP_DELAY - set delay of information on the LCD (1000 by default).

LCD views:

SV = Software calculated PRS value.

Calc = Hardware calculated PRS iteration at this time.

SS = Hardware calculated Single Step PRS value for current iteration.

CL = Hardware calculated Clocked PRS value for current iteration.

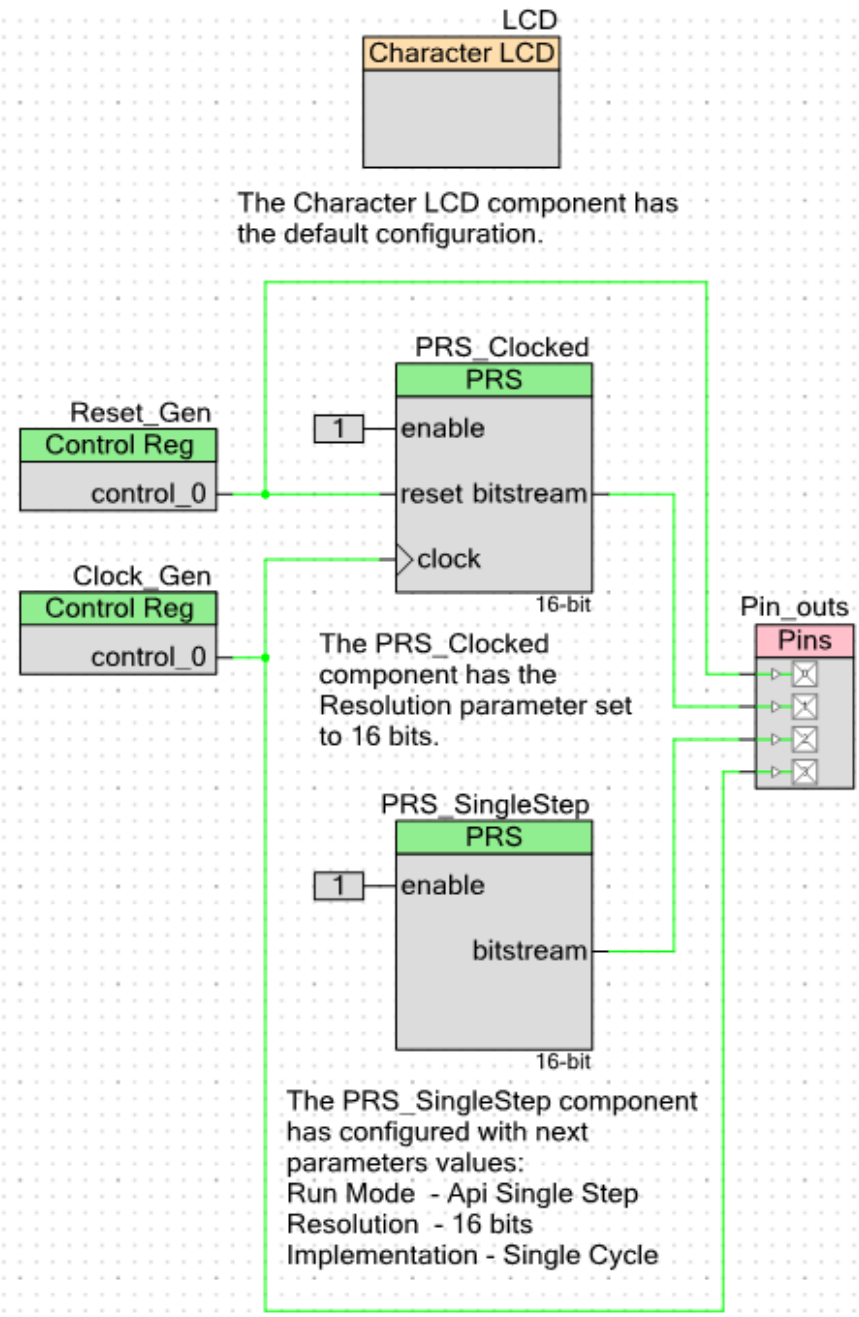

Figure 1. Top design schematic.

The Character LCD Component has the default configuration.
The PRS_Clocked component configuration (Figure 2):

- Run Mode - Clocked
- Resolution - 16 bits

- Implementation - Single Cycle
- Polynomial Value - 0xB400
- Seed Value - 0xFFFF

The PRS_SingleStep component configuration (Figure 3):

- Run Mode - API Single Step
- Resolution - 16 bits
- Implementation - Single Cycle
- Polynomial Value - 0xB400
- Seed Value - 0xFFFF

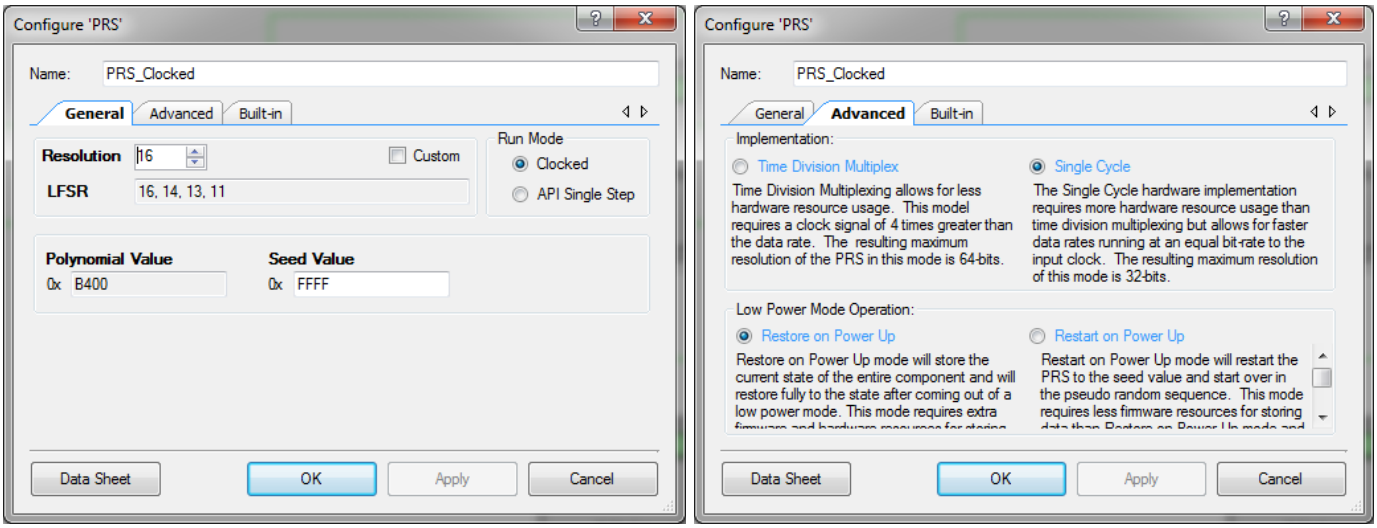

Figure 2. PRS_Clocked Component Configuration Window

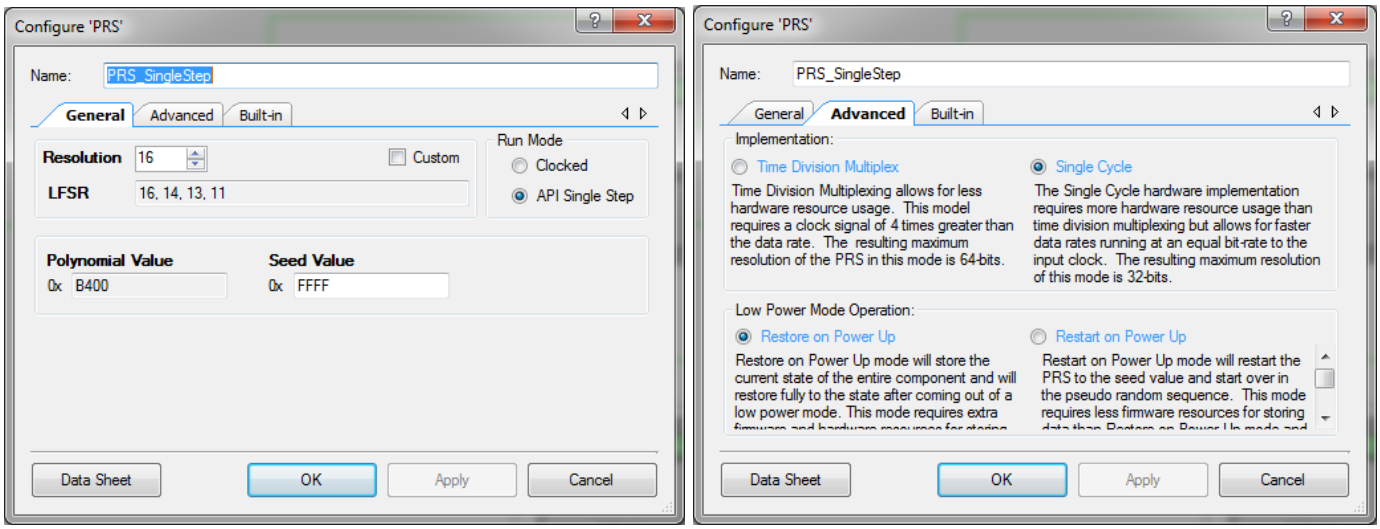

Figure 3. PRS_SingleStep Component Configuration Window

Project description

Both the PRS Components consistently execute some calculations (SEED_VALUE_COUNT define) at the same time. Its value displayed on LCD and named: SS (Single Step), CL (Clocked). The software calculated value is output on the LCD for verification (SV). After the calculation is finished, the resets on the both PRS components are executed. The values after reset are displayed on LCD and named: SS (Single Step), CL (Clocked).

Expected results

Display legend is described below:

First string: “SV=XXXX Calc=YY”
SV – Software calculated, XXXX – Software calculated PRS value, Calc – The current hardware PRS calculation iteration, YY – value of the current hardware PRS calculation iteration.

Second string: “SS=ZZZZ CL=SSSS”
SS – PRS_SingleStep component, ZZZZ – current iteration hardware calculated value of the PRS_SingleStep component, CL – PRS_Clocked component, SSSS – current iteration hardware calculated value of the PRS_Clocked component.

1)

2)

3)

4)

5)

6)

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