

The Power of Telemetry: Uncovering Software-Based Side-Channel Attacks on Apple M1/M2 Systems

Nikhil Chawla

Intel Corporation

nikhil.chawla@intel.com

Chen Liu

Intel Corporation

chen1.liu@intel.com

Abhishek Chakraborty

Intel Corporation

abhishek1.chakraborty@intel.com

Igor Chervatyuk

Intel Corporation

igor.chervatyuk@intel.com

Ke Sun

Intel Corporation

ke.sun@intel.com

Thaís Moreira Hamasaki

Intel Corporation

thais.moreira.hamasaki@intel.com

Henrique Kawakami

Intel Corporation

henrique.kawakami@intel.com

Abstract—Power analysis is a class of side-channel attacks, where power consumption data is used to infer sensitive information and extract secrets from a system. Traditionally, such attacks required physical access to the target, as well as specialized devices to measure the power consumption with enough precision.

The PLATYPUS attack [1] has shown that on-chip power meter capabilities exposed to a software interface might form a new class of power side-channel attacks. This paper presents a software-based power side-channel attack on Apple Silicon M1/M2 platforms, exploiting the System Management Controller (SMC) and its power-related keys, which provides access to the on-chip power meters through a software interface to user space software.

We observed data-dependent power consumption reporting from such keys and analyzed the correlations between the power consumption and the processed data. Our work also demonstrated how an unprivileged user mode application successfully recovers bytes from an AES encryption key from a cryptographic service supported by a kernel mode driver in MacOS. Furthermore, we discuss the impact of software-based power side-channels in the industry, possible countermeasures, and the overall implications of software interfaces for modern on-chip power management systems.

I. INTRODUCTION

It is well-known that CMOS circuits, when processing data, generate data-dependent power consumption. This behavior has been misused by attackers to perform power analysis attacks, extracting sensitive data, such as secret keys or passwords, from the target system. In traditional power side-channel attacks, the attacker typically requires physical access to the system to measure power consumption information.

Software-based power side-channel attacks represent a new class of power side-channel attacks that can be performed by a software attacker leveraging on-chip power meter capabilities provided by the hardware, without requiring physical access to the system. One example of such attacks is the PLATYPUS attack [1], which leverages the Running Average Power Limit (RAPL) energy counters available on x86 CPUs to extract sensitive information.

In this paper, we demonstrate a software-based power side-channel attack targeting ARM-based Apple M1/M2 systems. We observed that the System Management Controller (SMC) on Apple silicon exposes power meter capabilities to software. A set of such metrics are also accessible to user mode application in macOS. With experiments, we confirmed that a subset of those metrics is correlated with the data processed

by the CPU. Furthermore, we show that cryptographic operations, such as AES [2], performed by privileged software (e.g., kernel software) become vulnerable to software-based power side-channel attacks, by exploiting the unprivileged access to sensor data exposed by SMC.

This attack shows that software-based power side-channel attacks are an industry-wide problem spanning across various architectures, and show that it is not trivial to develop a suitable mitigation plan.

Our key contributions are:

- To the best of our knowledge, this is the first work that presents comprehensive software-based power side-channel analysis on ARM-based Apple silicon.
- We show that specific power meter reports provided by the Apple SMCs are data dependent. Moreover, the IOKit library exposes SMC sensor data to a user mode application, allowing an unprivileged attacker to infer secret keys from kernel mode.
- We discuss the impact of software-based power side-channels on the industry as a whole, the implication of software interfaces to modern on-chip power management systems, and possible countermeasure techniques to mitigate the risks of keeping such software interfaces available to unprivileged user mode application.

The remainder of this paper starts by presenting background and related work (Section II). In Section III, we present the details of our research on the SMC power meters reporting and data dependency finding, as well as the exploitation of the power side-channel. We then discuss possible countermeasure techniques in Section IV and Section V concludes our paper.

Responsible Disclosure: We responsibly disclosed our findings to Apple Inc. on November 29th, 2022. Following up on Apple’s request, we provided two different Proof-of-Concept (PoC) versions on January 2023 and March 2023, respectively. Apple acknowledged the findings, validated the PoC on June 27, 2023 and do not propose to take further actions to mitigate the issue.

II. BACKGROUND & RELATED WORK

In this section, we provide background on Apple System Management Controller, software-based power side-channels, and different methods of power analysis.

A. Power meter reporting on Apple platforms

The System Management Controller (SMC) is a co-processor responsible for power and thermal management available in multiple Apple platforms since the legacy x86-based Apple systems [3].

The SMC exposes various sensor data including temperature, voltage and power meters, battery status, fan status, and other power-related functions on the system. The sensor data is accessible to user mode software as a key-value pair, where the key is a 4-bit alphanumeric string [4] and the value can be retrieved by calling the `IOConnectCallStructMethod` function in the `IOKit` [5] library built in macOS.

B. Software-based power side-channel attacks

The PLATYPUS attack [1] has shown that the Running Average Power Limit (RAPL) energy reporting interfaces, which are available on Intel and AMD processors, expose data-dependent power consumption information that can be used to perform power side-channel attack by a software attacker.

Furthermore, recent works [6], [7] have discovered that CPUs, when hit certain reactive limits (e.g., power or current limits), will throttle to run at lower frequencies, which are correlated with energy consumption of the chip and hence correlated with data processed by the CPU.

Concurrent to this paper, Taneja *et al.* [8] discusses thermal limit induced frequency throttling side-channel on various integrated and discrete GPUs, and also mentions software-based power side-channels on ARM-based CPUs, including Apple M1/M2 systems. Compared to [8], our work conducts a more comprehensive study on the power telemetry side channel on Apple M1/M2 platforms.

C. Simple, Differential, and Correlation Power Analysis

Power analysis can be classified according to the statistical analysis applied on the data collected [9].

Simple power analysis (SPA) is a technique that supports the identification of patterns in power consumption traces during the execution of multiple operations. With aid of those patterns, one can identify the power consumption of specific instructions or operations in a single execution.

On the other hand, differential power analysis (DPA) is a more advanced technique that involves statistically analyzing multiple power traces with various input data to infer data-dependencies in the power consumption patterns.

Correlation power analysis (CPA) is also a statistical type of attack that uses the Pearson correlation coefficient. The goal is to correlate the power consumption reading and the input values being processed. This technique is powerful because it enhances even the small variations in the power consumption and helps by increasing the Signal-to-Noise Ratio (SNR). For this reason, CPA is considered a more sophisticated attack.

III. SMC POWER TELEMETRY ATTACKS

In previous works, energy consumption reported by RAPL interfaces on x86 processors are shown to correlate with both the instruction type and the data operand [1], [10]. In this section, we provide detailed descriptions of the procedures used to identify data-dependent SMC key values and evaluate

TABLE I: Specification of tested devices

Mac	#Pcore	#Ecore	OS	Max. Freq (GHz)
M1 Mini	4	4	macOS 12.5	3.2
M2 Air	4	4	macOS 13.0	3.5

the feasibility of performing software-based side-channel attacking using the keys.

A. Experimental Setup

We used an Apple Mac Mini M1 and an Apple MacBook Air M2 for all the experiments described in this section. Table I summarizes the specification of the systems.

B. Threat model

In this work, we assume the attacker is a user mode software and the victim is a kernel mode driver holding a secret. The victim may provide a service to user mode software. The attacker might use these services to call/invoke kernel routines that operate on the secret data. The attacker, as a user mode application, has no direct access to the secret which belongs to the kernel mode driver, but to the SMC key-value pairs.

C. Identifying workload-dependent SMC keys

Since official SMC key definitions for Apple M1/M2 systems are not publicly available, the initial phase of the research involved identifying the specific SMC keys that exhibit a correlation with power consumption among the extensive collection of available keys. Based on the established naming convention adopted in x86-based Mac systems, it has been observed that SMC keys associated to power-related functionalities commonly initiate with an initial capital letter “P” [11] [12]. By leveraging this information, we are able to significantly narrow down the pool of candidate keys to approximately 30.

To identify SMC keys that exhibit correlation with workload, we conducted an experiment using the open source tool `smc-fuzzer` [13]. This experiment involved comparing key values under both idle and busy system conditions. Through this comparative analysis, our objective was to derive the subset of SMC keys that demonstrate correlation with workload.

Figure 1 (a) lists a set of the SMC keys on the Apple M2 system that start with the letter “P”, along with their corresponding values when the system is in an idle state. Subsequently, in Figure 1 (b), we show the measurements of the same SMC keys during the execution of the `stress-ng` [14] workload, which involves performing matrix operations on all available cores. By conducting a side-by-side comparison of the results, we were able to identify certain SMC keys that exhibit variations in their values correlated with the workload. These specific SMC keys, highlighted in red, signify the impact of the workload on their respective values. This observation highlights the potential relationship between these specific SMC keys and the energy consumption during different workload scenarios.

For Apple M1, we replicated the experiment and the results of the comparison is shown in Figure 2. Table II summarizes the list of SMC keys related to the workload on M1/M2 systems, respectively.

PBAT [flt] 0.000000 (bytes 00 00 00 00)
PBLR [flt] 0.000000 (bytes 00 00 00 00)
PBLR [flt] 0.000000 (bytes 00 00 00 00)
PDTR [flt] 9.416653 (bytes 9a aa 16 41)
PHPC [flt] 65.000000 (bytes 00 00 02 42)
PHPC [flt] 0.360121 (bytes 00 00 00 40)
PHRM [flt] 0.738000 (bytes 91 9d 3c 3f)
PHPS [flt] 6.846638 (bytes a8 17 db 40)
PKBC [flt] 0.000000 (bytes 00 00 00 00)
PMVC [flt] 8.719171 (bytes b9 81 0b 41)
PO3 [flt] 0.000000 (bytes 00 00 00 00)
PO3 [flt] 0.000000 (bytes 00 00 00 00)
PP01 [flt] 4.497846 (bytes ad a6 8e 40)
PP1b [flt] 0.000140 (bytes 17 87 12 39)
PP2b [flt] 0.252031 (bytes 27 0a 81 3e)
PP2l [flt] 0.000578 (bytes 6c 68 17 3a)
PP3b [flt] 1.000000 (bytes 00 00 00 00)
PP4b [flt] 0.035282 (bytes 5a 94 10 3d)
PP7b [flt] 0.000000 (bytes 00 00 00 00)
PP7l [flt] 0.023215 (bytes d7 2e 3c 3d)
PP8l [flt] 0.107338 (bytes d7 d3 db 3d)
PP9b [flt] 0.262403 (bytes a9 59 86 3e)
PP9l [flt] 0.000110 (bytes 80 7e 7f 38)
PPBR [flt] 0.4463390 (bytes 71 41 ed 3e)
PPBb [flt] 0.016990 (bytes 27 41 8b 3c)
PPD [flt] 0.000000 (bytes 00 00 00 00)
PPF1 [flt] 0.144769 (bytes 16 46 14 3e)
PR41 [flt] 0.006890 (bytes 30 c7 1e 3b)
PR5b [flt] 0.013392 (bytes 80 69 5b 3c)
PR6b [flt] 0.000000 (bytes 00 00 00 00)
PR8b [flt] 0.020220 (bytes 18 a4 5c 3c)
PRAb [flt] 0.000000 (bytes 00 00 00 00)
PRC1 [flt] 0.022941 (bytes 75 f5 eb 3c)
PReb [flt] 0.000000 (bytes 00 00 00 00)
PSTR [flt] 9.332568 (bytes 33 52 15 41)

(a) (b)

Fig. 1: Apple M2 power related SMC key values comparison when the system is (a) idle and (b) running stressor code

PDTR [flt] 2.430592 (bytes d1 8e 1b 40)
PGDP [flt] 0.000000 (bytes 00 00 00 00)
PHPC [flt] 65.000000 (bytes 00 00 02 42)
PHPC [flt] 1.1559149 (bytes 9a aa 16 41)
PHRM [flt] 1.000000 (bytes 00 00 00 3f)
PHRS [flt] 0.031655 (bytes 11 65 b1 3c)
PMVR [flt] 0.934172 (bytes e5 25 6f 3f)
PO3R [flt] 0.945445 (bytes a8 08 72 3f)
PO5R [flt] 0.072289 (bytes 11 0c 94 3d)
PP0b [flt] 0.000000 (bytes 00 00 00 00)
PP0l [flt] 0.0009704 (bytes b0 fc 1e 3c)
PP1b [flt] 0.000000 (bytes 00 00 00 00)
PP2b [flt] 0.000000 (bytes 00 00 00 00)
PP3b [flt] 0.000000 (bytes 00 00 00 00)
PP3l [flt] 0.000000 (bytes 00 00 00 00)
PP7b [flt] 0.000000 (bytes 00 00 00 00)
PP7l [flt] 0.014640 (bytes 00 00 00 00)
PP9b [flt] 0.000000 (bytes 00 00 00 00)
PP9l [flt] 0.00055 (bytes 80 66 3e 38)
PPMR [flt] 0.598044 (bytes f6 19 19 3f)
PPSR [flt] 0.124430 (bytes 15 d5 fe 3d)
PPb [flt] 0.000000 (bytes 00 00 00 00)
PPeb [flt] 0.000000 (bytes 00 00 00 00)
PP4b [flt] 0.000000 (bytes 00 00 00 00)
PR41 [flt] 0.002006 (bytes da 6f 03 3b)

(a) (b)

Fig. 2: Apple M1 power related SMC key values (partial) comparison when the system is (a) idle and (b) running stressor code

D. Identifying data-dependent SMC keys

Subsequently, we identify the data-dependent SMC keys from the previous list of workload-dependent keys. To accomplish this, we design and implement a Proof-of-Concept (PoC) that involves repetitively executing the same workload while accepting and processing distinct input data for a fixed number of iterations. During each iteration, different input data is provided to the workload. We measure and log multiple data points of each selected SMC key for each input, generating a so-called *trace*.

In order to enhance the energy consumption correlation with the input provided, we opt to replicate the workload and execute it simultaneously on three P-cores. This amplification allows us to capture a more pronounced correlation between the power consumption and the specific data inputs processed by the SMC keys.

We then apply the Test Vector Leakage Assessment (TVLA) [15] to validate if any of the pre-selected SMC key value

TABLE II: Workload-dependent SMC Keys whose values are correlated with *stress-ng* workload

SMC keys	Mac Mini M1	Macbook Air M2
PDTR, PHPC, PHPS, PMVR, PPMR, PSTR	PDTR, PHPC, PHPS, PMVC, PSTR	

traces show data-dependency. TVLA utilizes Welch's t-test to assess side-channel leakage of cryptographic schemes. A Welch's t-test compares two datasets, A and B, by computing a statistic score, the *t-score*. A $|t\text{-score}| > 4.5$ indicates that two datasets, A and B, are statistically distinguishable with 99.99% confidence.

For this experiment, we selected the implementation of AES-128 encryption from *AES-Intrinsics* [16] as the testing workload, which utilizes the ARMv8 equivalent to the cryptographic extension AES instructions (e.g., AESE and AESMC). We observed that the SMC key values are updated approximately every one second. Therefore, the victim AES encryption for the same plaintext is repeatedly executed for more than one second. We collected 10k SMC key value traces corresponding to the encryption of each of the three chosen plaintexts - (*All_0s*, *All_1s*, and *Random*) - with a fixed key. We then applied TVLA analysis between all possible pairs of those chosen plaintexts. Table III shows the TVLA results on the Apple M2 system for the selected SMC keys between the different and same plaintexts for the AES workload. Different colors mean:

- **True positive:** two traces with different plaintexts are distinguishable.
- True negative: two traces with the same plaintext are non-distinguishable.
- **False positive:** two traces with the same plaintext are distinguishable.
- **False negative:** two traces with different plaintexts are non-distinguishable.

Out of the selected SMC keys, one key, namely *PHPC*, stands out by demonstrating true positive and true negative results consistently. Remarkably, *PHPC* exhibits no instances of false positive or false negative correlations. This finding strongly suggests that *PHPC* has the most robust and reliable correlation with the data.

In the case of *PDTR*, *PMVC*, and *PSTR*, these SMC keys exhibit a combination of true positive and true negative results for a majority of the pairs. However, they also display several instances of false positive or false negative correlations. This indicates a somewhat weaker data-correlation compared to *PHPC*. Conversely, the SMC key *PHPS* primarily generates false negative correlations for most of the pairs and does not yield any true positive correlations, suggesting a limited data-correlation.

As a result of our analysis, we have confirmed the data-dependency for all the selected SMC keys except for *PHPS* on the Apple M2 system. Additionally, we conducted TVLA analysis on the collected traces of the *PHPC* key values collected on the Apple M1 platform, affirming a similar data-dependency pattern for the *PHPC* key on this system as well.

E. AES encryption key extraction

Following the confirmation of data-dependency in the SMC key values, our research assesses the feasibility of extracting secrets from a victim program. In a manner similar to the previous experiment, our focus is on an AES-128 encryption implementation obtained from *AES-Intrinsics* [16]. The victim

TABLE III: TVLA result on Apple M2 system for selected SMC keys between different plaintexts for the AES workload.

Key	PHPC			PDTR			PHPS			PMVC			PSTR		
Plaintext	All 0s	All 1s	Random	All 0s	All 1s	Random	All 0s	All 1s	Random	All 0s	All 1s	Random	All 0s	All 1s	Random
All 0s'	-0.18	20.94	11.49	8.73	29.58	25.05	0.87	2.14	2.02	9.49	32.16	27.33	21.30	12.96	27.41
All 1s'	-21.09	0.09	-8.87	-20.42	0.02	-4.49	-1.97	-0.69	-0.84	-22.45	0.09	-5.15	9.13	0.37	15.16
Random'	-11.60	9.28	0.43	-15.28	5.01	0.55	-0.53	0.74	0.61	-17.54	4.92	-0.23	5.99	-15.03	-0.24

program repeatedly carries out encryption operations using a secret key that remains inaccessible to the attacker. However, in contrast to providing a fixed plaintext like the previous experiment, the attacker process now injects random plaintext inputs into the victim program. During this process, the attacker records the plaintext, the generated ciphertext, and the corresponding SMC key values once the encryption operation is completed. It is important to note that, to minimize noise the AES-128 encryption takes place in user mode for the purpose of this PoC.

In this experiment, we collect one million traces on the M2 system and 350k traces on the M1 system, respectively. We then perform Correlation Power Analysis (CPA) to analyze the collected SMC key value traces. CPA involves computing correlations between the power side-channel traces and a hypothetical power model derived from the Hamming Weight (HW) or Hamming Distance (HD) of intermediate states. In our CPA approach, the power traces used for analysis correspond to the SMC key value traces we collected. The hypothetical power models employed are similar to those used in traditional CPA. These models incorporate the HW or HD of intermediate states, which are:

- **Rd0-HW:** HW after the first *AddRoundKey* operation to recover initial round key
- **Rd10-HW:** HW before the last round *SubBytes* operation to recover round #10 key
- **Rd10-HD:** HD between last round input and ciphertext to recover round #10 key.

For each targeted key byte, the hypothetical power model is constructed using HW/HD of intermediate round state for all possible key guesses. We calculate the correlation coefficient between the SMC key value trace and the hypothetical power model, then rank all key guesses in decreasing order of correlation coefficient's magnitude. The outcome of the CPA test is the rank of the correct key byte with a value of 1 indicating recovery of the secret key byte. The average rank across all key bytes is measured by *Guessing Entropy* (GE). Lower GE indicates lower ranks across all key bytes and $GE = 0$ indicates recovery of all key bytes.

Table IV summarizes the final ranks of secret key bytes and the Guessing Entropy after applying CPA on the collected SMC key value traces with *First round Hamming Weight* (Rd0-HW) power model on the M2/M1 system. Key bytes that are correctly recovered (rank = 1) are marked as red, while key bytes that are almost recovered (rank < 10) are marked as yellow.

On the Macbook Air M2 system, comparing key ranks across SMC key value traces, we observe CPA on PHPC key value traces recover most secret key bytes (6 out of 16) with the other 6 bytes almost recovered. CPA on PDTR and PMVC key value traces shows the low rank for multiple key bytes (10

TABLE IV: Rank of the recovered secret key byte of AES applying CPA on collected SMC key value traces with Round 0 HW power model on Macbook Air M2 and M1 (PHPC only)

	PHPC	PDTR	PMVC	PSTR	PHPC (M1)
0	7	1	3	211	9
1	7	7	3	22	19
2	1	5	3	188	4
3	11	11	12	189	12
4	5	1	1	151	1
5	4	15	12	223	31
6	4	6	14	113	16
7	13	8	12	39	5
8	1	15	17	201	9
9	37	16	22	101	18
10	1	5	11	214	7
11	1	2	2	117	2
12	1	2	1	146	1
13	4	12	13	184	36
14	1	9	8	18	25
15	26	24	14	137	50
GE	31.0	41.6	42.8	109.3	40.9

out of 16 key bytes – *PDTR*, 7 out of 16 key bytes – *PMVC*). *PSTR* key traces, on the other hand, recovers none of the key bytes. On the Apple M1 mini system, we repeated the test for the *PHPC* key and observed that 2 out of the 16 bytes can be recovered, while 6 other bytes have ranks lower than 10. .

Fig. 3 shows the trend in GE with different number of *PHPC* key value traces with different power models, for both M1 and M2 systems. The GE trend is shorter corresponding to M1 system due to shorter number of *PHPC* key value traces (350K traces). A consistent and converging trend when analyzing an increasing number of collected SMC key value traces indicates that as more traces are gathered, the recoverability of all key bytes becomes feasible. There is a distinct convergence patterns among the different power models utilized. Notably, the *Rd0-HW* power model exhibited the fastest convergence rate, indicating its effectiveness in recovering the key bytes. The *Rd10-HW* power model also demonstrated convergence, albeit at a considerably slower rate. However, the *Rd10-HD* power model exhibited minimal convergence, suggesting limited effectiveness in recovering the key bytes. This further supports the suitability and reliability of the *Rd0-HW* model for extracting valuable information from the SMC key value traces on Apple M1/M2 platforms.

F. Targeting a kernel module

To provide insight of the feasibility of the attack with a more realistic threat model, we implement a kernel module that serves as an encryption engine to encrypt the user provided plaintexts using AES-128. The secret key is hosted in the kernel-only memory. The attacker is a user mode application, with read access to the SMC key values through the interface provided by the IOKit framework. To implement this kernel module, we leveraged the kernel extensions support in the

TABLE V: TVLA analysis on selected SMC key traces corresponding to encryption of different plaintext inputs from AES device driver on the Macbook Air M2 system

Key Plaintext	PHPC			PDTR			PHPS			PMVC			PSTR		
	All 0s	All 1s	Random	All 0s	All 1s	Random	All 0s	All 1s	Random	All 0s	All 1s	Random	All 0s	All 1s	Random
All 0s'	2.78	19.28	9.41	13.84	41.52	43.01	2.72	3.60	6.51	15.13	45.38	47.10	40.66	18.45	37.50
All 1s'	-17.91	-0.76	-11.12	-30.27	-2.16	-0.26	-3.99	-3.12	-0.11	-32.93	-2.44	-0.48	-18.45	1.66	20.01
Random'	-6.77	10.14	-0.04	-30.84	-0.73	-0.99	-3.85	0.11	0.03	-33.30	-0.56	-1.03	0.73	-20.70	-2.16

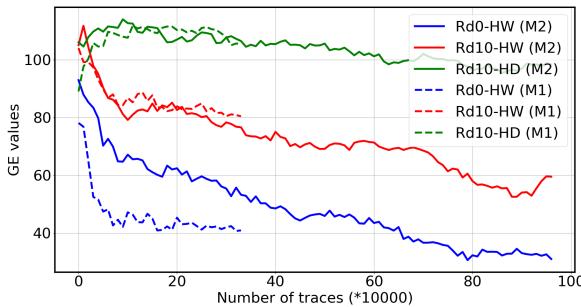


Fig. 3: GE trend against collected *PHPC* SMC key value traces for CPA targeting user space AES encryption on Apple M1 Mini and M2 Air system

Xcode IDE for iOS developers [17]. This kernel extension implements the AES-128 encryption from *AES-Intrinsics* using a device driver. The device driver accepts the plaintext from a user mode application, repeatedly encrypts the plaintext for fixed amount of iterations and writes the ciphertext to a buffer, which can be read by the user mode application. In this implementation, a single thread executing on P-core invokes the device driver for encrypting the plaintext.

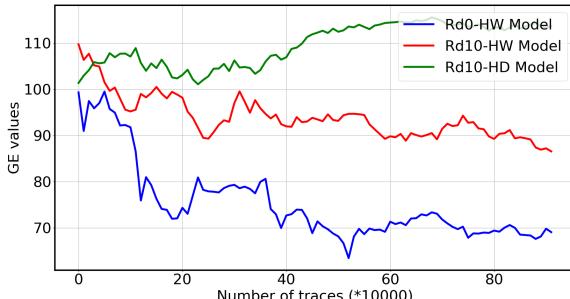


Fig. 4: GE trend against number of collected *PHPC* SMC key value traces for CPA targeting AES kernel module on the Macbook Air M2 system

Next, we applied TVLA on collected SMC key traces to check if the SMC keys identified in previous test still exhibit data-dependency. We followed similar steps outlined in section III-D to collect SMC key traces corresponding to encryption of different plaintext inputs obtained from the device driver. Table V summarizes the *t-scores* evaluated for SMC key traces corresponding to encryption of *All_zero*, *All_one*, and *Random* plaintext input with a fixed key from device driver on Macbook Air M2 system. We followed the same color-coding convention as outlined in section III-C to interpret the TVLA test results. We observe similar trend, meaning that *PHPC* key traces ex-

hibit the strongest correlation, followed by *PDTR*, *PMVC* and *PSTR* key traces, and that *PHPS* shows the lowest correlation. These results once more confirm our findings regarding data-dependency for most SMC keys, except *PHPS*.

We conducted a CPA test on the collected SMC key value traces that exhibited data correlation on the TVLA test. The objective was to recover the AES encryption key from the device driver. We collected a dataset of one million traces each for each of the SMC keys, *PHPC*, *PDTR*, *PMVC* and *PSTR*. We then applied CPA with the hypothetical power models considered in section III-D and obtained the GE metric.

Fig. 4 illustrates the GE trend against the one million traces, when CPA was applied on *PHPC* SMC key value traces using different explored power models. We observe the converging trend, indicating a reduction in the rank of correct key bytes with an increasing number of collected traces. Among the power models tested, the *Rd0-HW* power model demonstrated the strongest correlation with the collected *PHPC* key traces, as indicated by the fastest convergence of the GE metric. On the other hand, the *Rd10-HD* power model did not exhibit any convergence.

Additionally, we observed that the GE metric converged at a slower rate, approximately two times slower, when CPA was applied to the collected SMC key traces from the kernel module implementation of the AES victim, compared to the user mode AES application (Fig. 3). This can be attributed to the decreased SNR of the collected traces due to system call invocations and the lower number of victim threads.

The experimental findings from the CPA test indicate that an unprivileged attacker can compromise the confidentiality of assets protected by the kernel.

IV. DISCUSSION & POSSIBLE COUNTERMEASURES

To address the vulnerabilities highlighted by the PLATYPUS attack [1], both Intel and AMD have taken measures to mitigate the risk. Specifically, they have removed the user space software access to the RAPL (Running Average Power Limit) energy counters from the Linux kernel drivers [18], [19]. Additionally, Intel has introduced a RAPL filtering mechanism, which introduces random energy noise into the energy reporting interface and adjusts the update interval [20]. These measures aim to decrease the SNR of observable power consumption differences, making it more challenging to extract sensitive information through similar power side-channel attacks.

Considering the issues discussed in our paper, we believe similar countermeasures can be applied to address the vulnerabilities discussed in this paper. By implementing mechanisms to reduce the SNR of power consumption differences and introducing random energy noise, the effectiveness of this type of power side-channel attacks can be significantly reduced.

However, as of the publication of this paper, we are not aware of any specific plans from Apple to provide mitigations against the vulnerabilities discussed in our research. It is important that system vendors and developers consider the potential security implications of this class of power side channel attacks and implement appropriate safeguards to protect sensitive information.

This work, along with numerous other studies conducted in recent years, highlights the widespread nature of power meters side-channel attacks across various CPU architectures. The findings underscore the importance of acknowledging this issue and prompt all vendors in the industry to recognize the significance of software-based power side-channel attacks. It is crucial for vendors to proactively explore architectural solutions and implement preventive measures to mitigate the risks associated with newer power side-channel attacks.

By raising awareness about the prevalence and potential impact of exposing power meters reports to unprivileged software, we aim to encourage industry-wide collaboration and collective efforts towards enhancing the security and privacy of CPU architectures. It is imperative that vendors prioritize the development and implementation of robust security mechanisms that effectively address the vulnerabilities exposed by these attacks. This proactive approach will contribute to the creation of more secure and resilient systems, safeguarding sensitive information from potential exploitation through software-based power side-channel attacks.

V. CONCLUSION

This paper has explored the vulnerabilities arising from software-based power side-channel attacks and their implications across CPU architectures. Our experiments and analysis have revealed the data dependency of the power consumption reported by the selected System Management Controller (SMC) key values on ARM-based Apple Silicon M1/M2 systems. Furthermore, we demonstrated that a user space attacker can exploit the unprivileged access to the SMC key values to extract secrets from the kernel device driver. Our research underscores the need for industry-wide awareness and proactive exploration of architectural solutions to prevent software-based power side-channel attacks. It is crucial for vendors to prioritize security measures and collaborate in order to enhance the resilience of CPU architectures against such vulnerabilities.

REFERENCES

- [1] M. Lipp, A. Kogler, D. Oswald, M. Schwarz, C. Easdon, C. Canella, and D. Gruss, “PLATYPUS: Software-based Power Side-Channel Attacks on x86,” in *2021 IEEE Symposium on Security and Privacy (SP)*, 2021, pp. 355–371.
- [2] National Institute of Standards and Technology, “Advanced encryption standard (aes),” U.S. Department of Commerce, Washington, D.C., Tech. Rep., 2001.
- [3] A. Barisani, “Practical exploitation of embedded systems,” (Accessed June 8, 2023). [Online]. Available: https://github.com/abarisani/abarisani.github.io/blob/master/research/smc/practical_exploitation_of_embedded_systems.pdf
- [4] A. Ionescu, “Ninjas and Harry Potter - ‘Spell’unking in Apple SMC Land,” (Accessed June 8, 2023). [Online]. Available: <http://publications.alex-ionescu.com/NoSuchCon/NoSuchCon%202013%20-%20Ninjas%20and%20Harry%20Potter%20-%20Spellunking%20in%20the%20Apple%20SMC%20Land.pdf>

- [5] Apple Inc., “Apple Developer Documentation - IOKit,” (Accessed June 8, 2023). [Online]. Available: <https://developer.apple.com/documentation/iokit/1514274-icontectcallstructmethod>
- [6] Y. Wang, R. Paccagnella, E. T. He, H. Shacham, C. W. Fletcher, and D. Kohlbrenner, “Hertzbleed: Turning power Side-Channel attacks into remote timing attacks on x86,” in *31st USENIX Security Symposium (USENIX Security 22)*. Boston, MA: USENIX Association, Aug. 2022, pp. 679–697.
- [7] C. Liu, A. Chakraborty, N. Chawla, and N. Roggel, “Frequency throttling side-channel attack,” ser. CCS ’22. New York, NY, USA: Association for Computing Machinery, 2022, p. 1977–1991.
- [8] H. Taneja, J. Kim, J. J. Xu, S. van Schaik, D. Genkin, and Y. Yarom, “Hot pixels: Frequency, power, and temperature attacks on gpus and arm socs,” 2023.
- [9] S. Mangard, E. Oswald, and T. Popp, *Power analysis attacks: Revealing the secrets of smart cards*. Springer Science & Business Media, 2008, vol. 31.
- [10] C. Liu, M. Kar, X. Wang, N. Chawla, N. Roggel, B. Yuce, and J. M. Fung, “Methodology of assessing information leakage through software-accessible telemetries,” in *2021 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*. IEEE, 2021, pp. 259–269.
- [11] “VirtualSMC,” (Accessed June 2, 2023). [Online]. Available: <https://github.com/acidanthera/VirtualSMC/tree/master>
- [12] “iSMC,” (Accessed June 8, 2023). [Online]. Available: <https://github.com/dkorunic/iSMC/blob/master/smc/sensors.go>
- [13] b. Teddy Reed, “SMC Fuzzer,” <https://github.com/theopolis/smcfuzz>, 2023-05-26.
- [14] C. I. King, “Stress-ng,” URL: <http://kernel.ubuntu.com/git/cking/stressng.git/> (visited on 28/03/2018), 2017.
- [15] B. J. Gilbert Goodwill, J. Jaffe, P. Rohatgi *et al.*, “A testing methodology for side-channel resistance validation,” in *NIST non-invasive attack testing workshop*, vol. 7, 2011.
- [16] R. Z. Jeffrey Walton, “AES-Intrinsics,” <https://github.com/noloader/AES-Intrinsics/tree/master>, 2023-05-26.
- [17] Apple Inc., “Xcode,” <https://developer.apple.com/xcode/>, 2023-06-09.
- [18] Intel Inc., “2020.2 IPU - Intel RAPL Interface Advisory,” <https://www.intel.com/content/www/us/en/security-center/advisory/intel-sa-00389.html>, 2023-06-09.
- [19] MITRE, “CVE-2020-12912,” <https://cve.mitre.org/cgi-bin/cvename.cgi?name=CVE-2020-12912>, 2023-06-09.
- [20] Intel Inc., “Running Average Power Limit Energy Reporting / CVE-2020-8694, CVE-2020-8695 / INTEL-SA-00389,” <https://www.intel.com/content/www/us/en/developer/articles/technical/software-security-guidance/advisory-guidance/running-average-power-limit-energy-reporting.html>, 2023-06-09.