A HARDWARE IMPLEMENTATION OF A VQ INDEX BASED STEGANOGRAPHY TECHNIQUE

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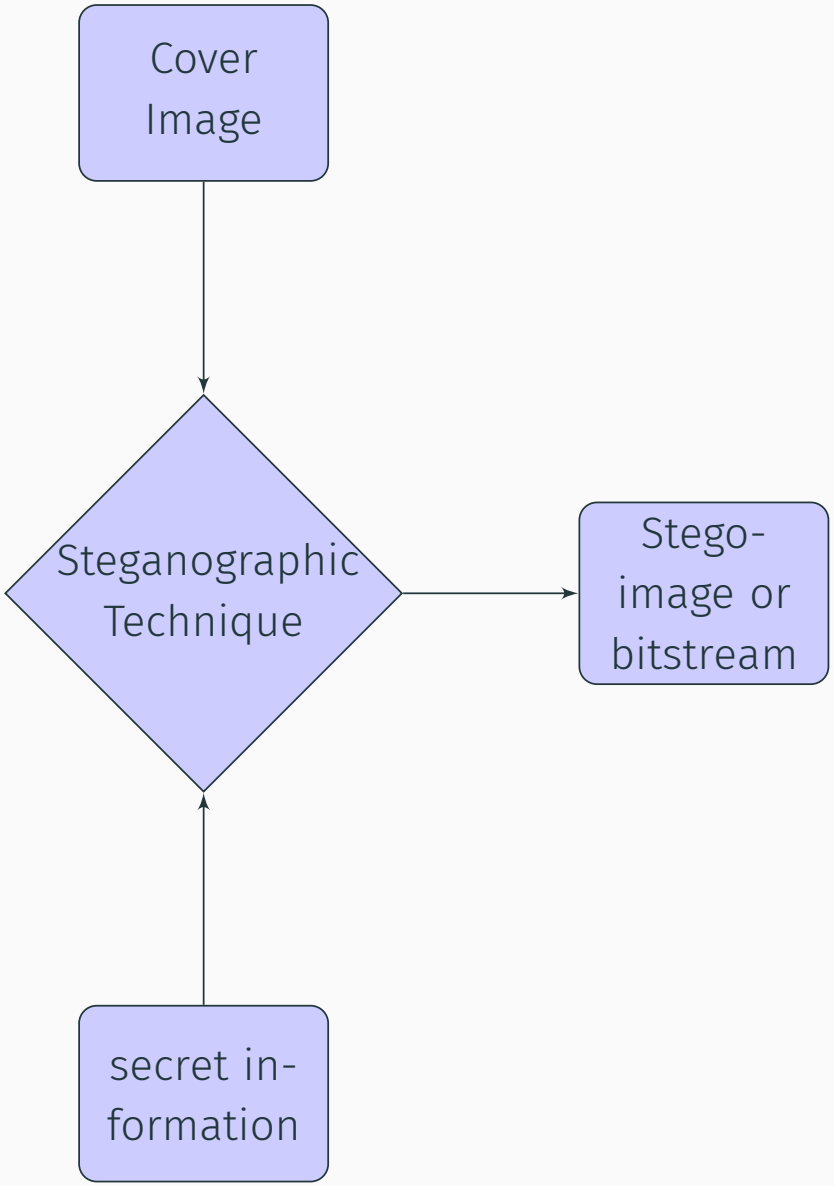
BACKGROUND

WHAT IS STEGANOGRAPHY ?



WHAT IS AN FPGA ?

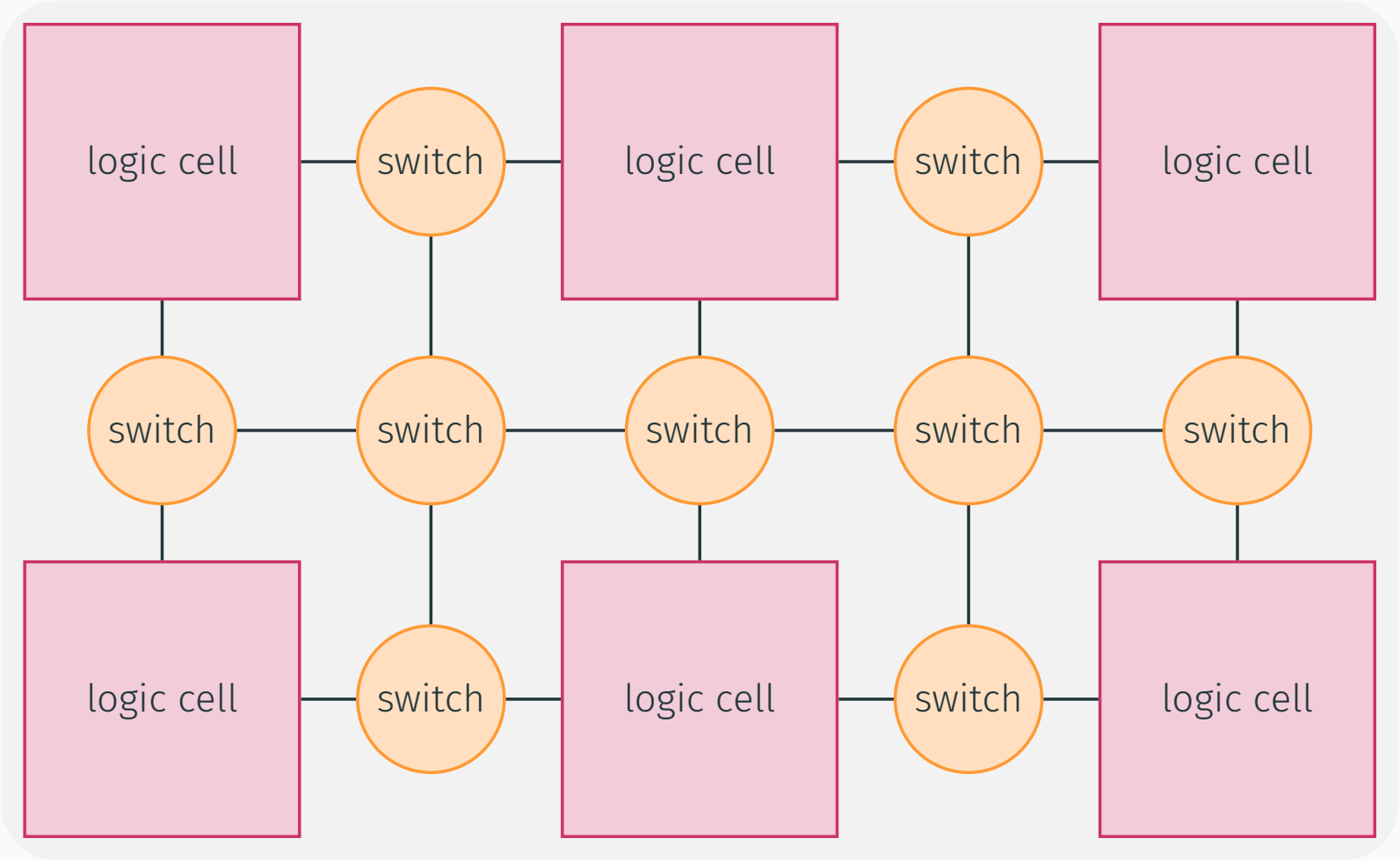


Figure: FPGA structure

WHAT IS AN FPGA ?

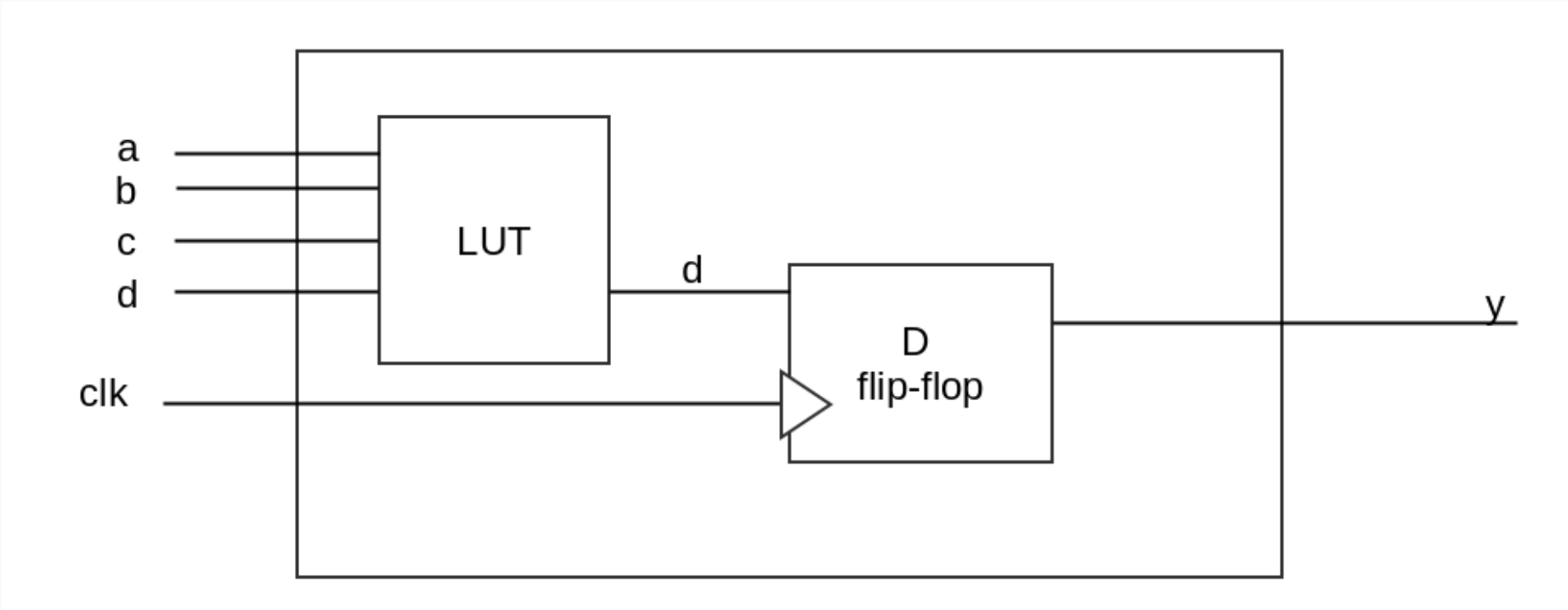


Figure: Internal structure of logic cell

WHY IMPLEMENT ON AN FPGA ?

WHY IMPLEMENT ON AN FPGA ?

- No Von Neumann Bottleneck
- No Context Switching
- Is more energy efficient than a software implementation
- Is a standalone component

RESULTS

ENCODER STATE MACHINE

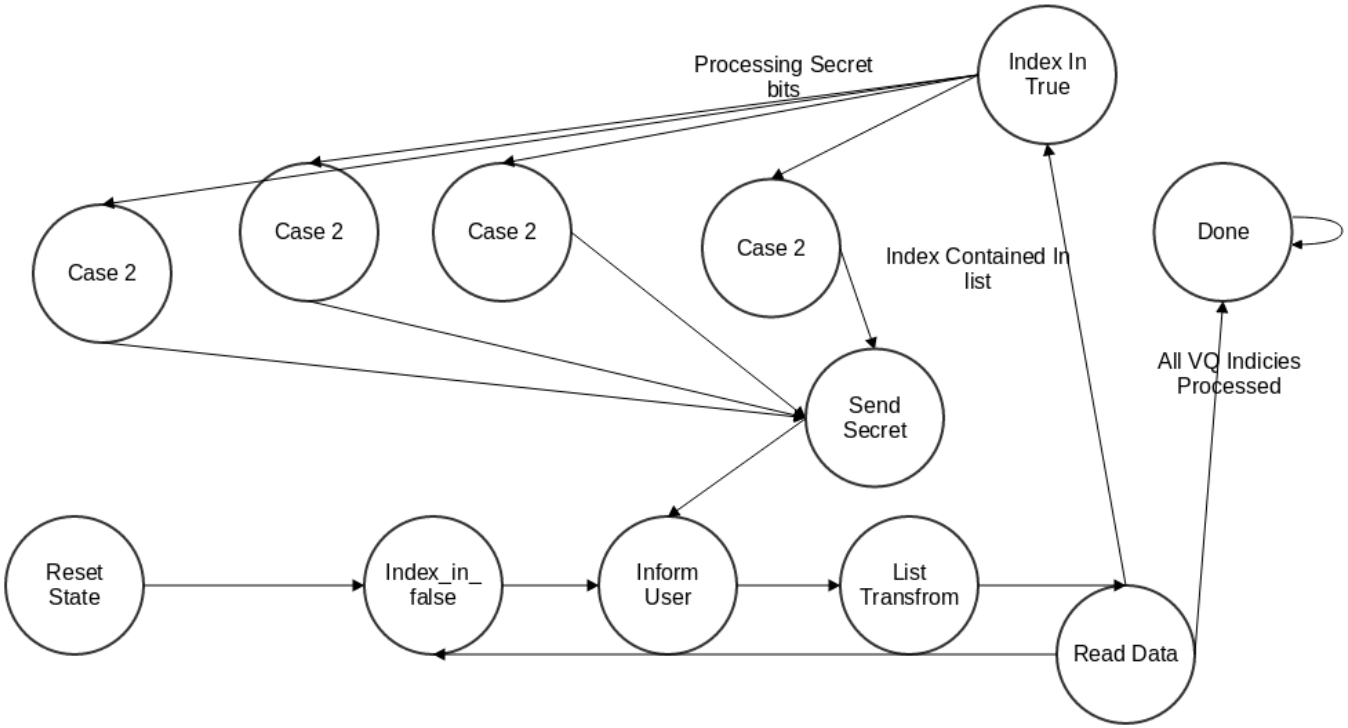
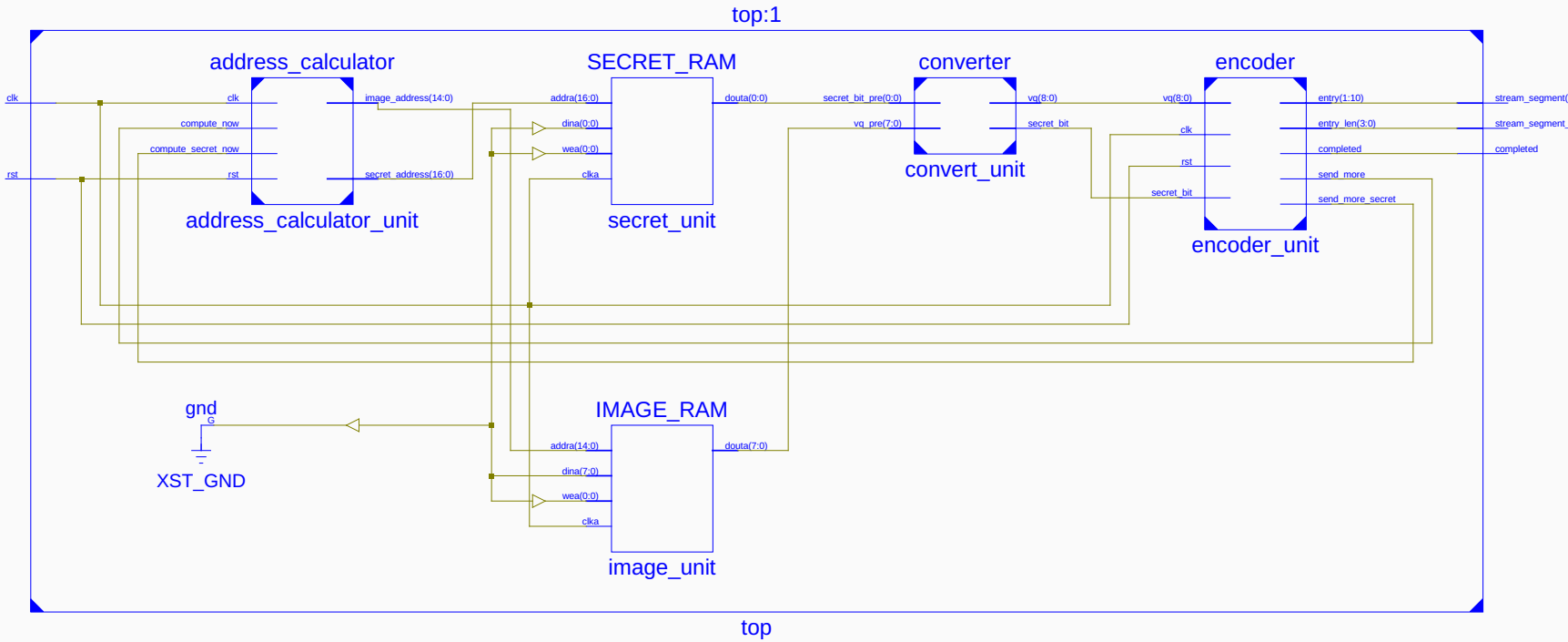


Figure: State machine for encoder circuit

ENCODER CIRCUIT OVERVIEW



ENCODER CIRCUIT UTILIZATION

Logic Utilization	Used	Available	Utilization
Number of Slices	97	4656	2 %
Number of Slice Flip Flops	125	9312	1 %
Number of 4 input LUTs	143	9312	1 %
Number of bonded IOBs	17	232	7 %
Number of BRAMs	15	20	75 %
Number of GCLKs	1	24	4 %

Table: Summary of resource utilization for encoder on XC3S500E

ENCODER TIMING STATISTICS

Minimum period	9.058 ns
Maximum Frequency	110.405 MHz
Minimum input arrival time before clock	3.900 ns
Maximum output required time after clock	4.040 ns
Maximum combinational path delay	No Path found

Table: Timing estimates for the encoder produced by the systhesis tool

DECODER STATE MACHINE

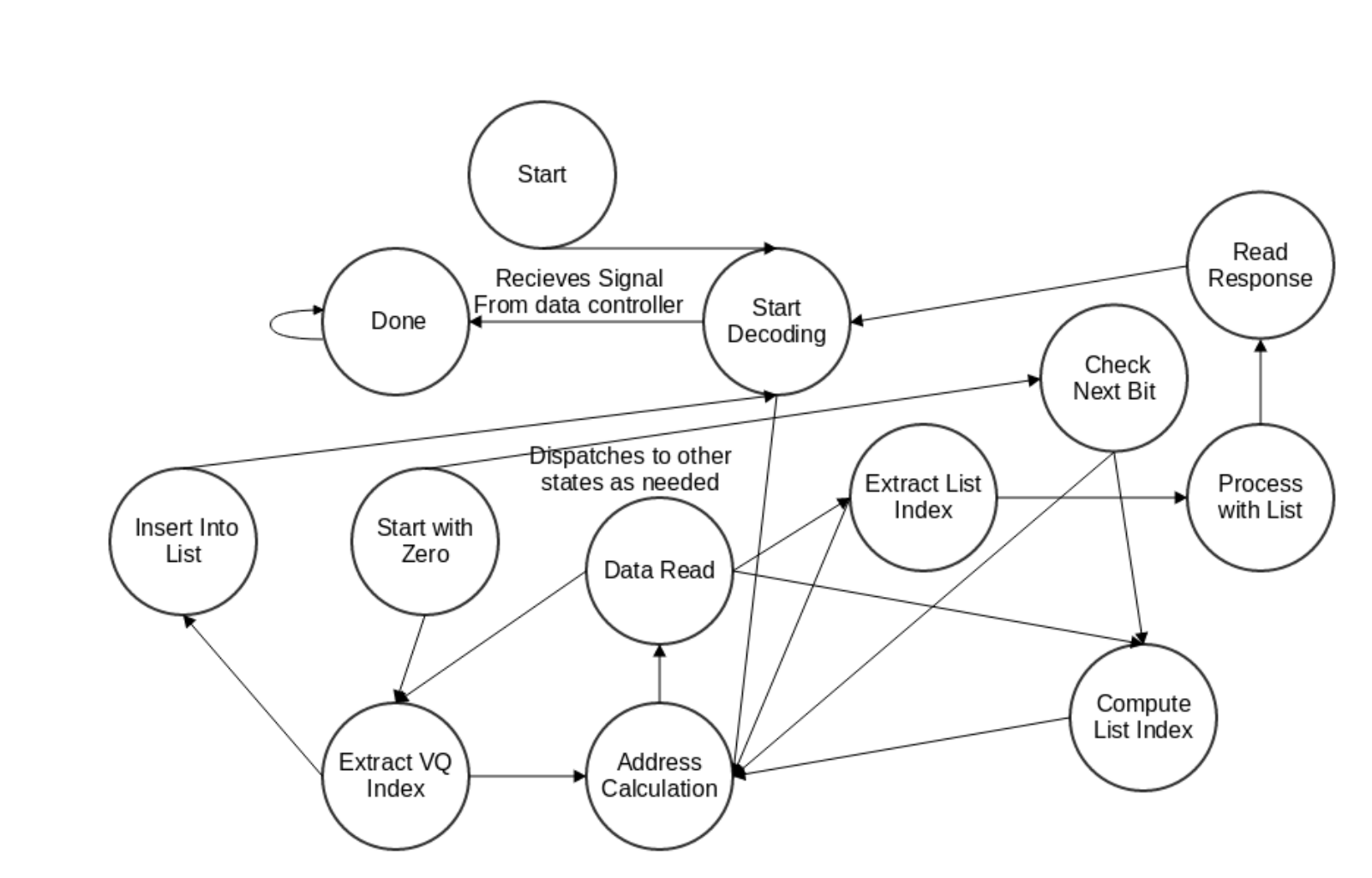
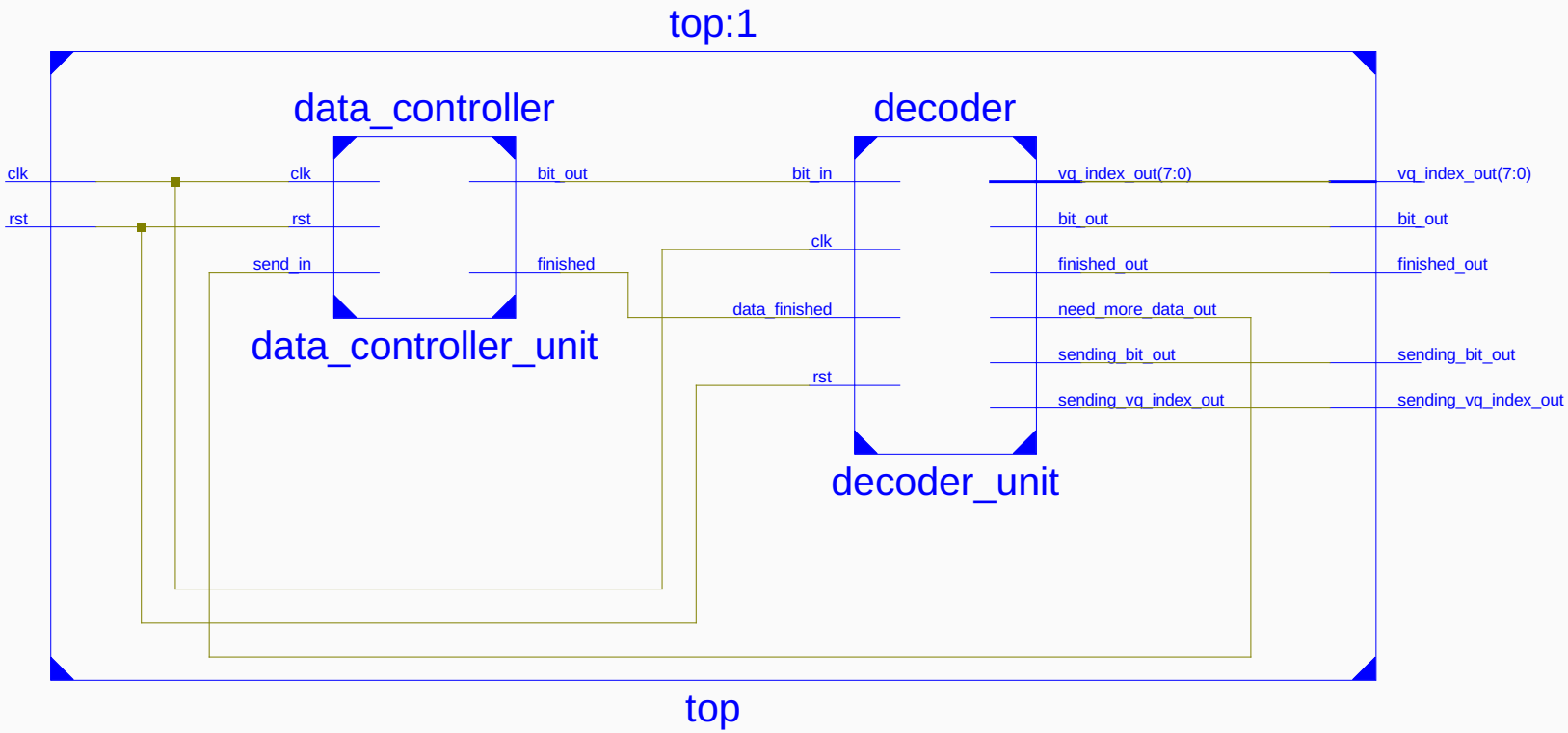


Figure: State machine for decoder circuit

DECODER CIRCUIT OVERVIEW



DECODER CIRCUIT UTILIZATION

Logic Utilization	Used	Available	Utilization
Number of Slices	152	4656	3 %
Number of Slice Flip Flops	157	9312	1 %
Number of 4 input LUTs	285	9312	3 %
Number of bonded IOBs	14	232	6 %
Number of BRAMs	9	20	45 %
Number of GCLKs	1	24	4 %

Table: Summary of resource utilization for decoder on XC3S500E

DECODER TIMING STATISTICS

Minimum period	8.067 ns
Maximum Frequency	123.967 MHz
Minimum input arrival time before clock	4.371 ns
Maximum output required time after clock	4.040 ns
Maximum combinational path delay	No Path found

Table: Timing estimates for the decoder produced by the systhesis tool

Questions?