Visualizing SAT Instances
and Runs of the DPLL Algorithm

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Abstract. SAT-solvers have turned into essential tools in many areas of applied logic like, for example, hardware verification or satisfiability checking modulo theories (SMT). And although recent implementations are able to solve problems with hundreds of thousands of variables and millions of clauses, much smaller instances still remain unsolved. What makes a particular instance hard or easy is at most partially understood—and is often attributed to the instance's *internal structure.* By converting SAT instances into graphs and applying established graph layout techniques this internal structure can be visualized and thus serve as the basis of subsequent analysis. Moreover, by providing tools that animate the structure during the run of a SAT algorithm, dynamic changes of the problem instance become observable. Thus, we both expect to gain new insights into the hardness of the SAT problem and to help in teaching SAT algorithms.

1. Motivation

Progress in SAT-solving has been tremendous over the past years. Problems that were completely out of reach ten years ago can now be handled with success [8]. Especially in hardware verification SAT solvers (and the associated method of bounded model checking [15]) wrote a glittering success story [44, 66], and in many areas replaced the until then predominant BDD-based model checkers [13]. But also in other combinatorial problem domains like planning [40], configuration [41], satisfiability modulo theory [5], or software verification [65, 71] SAT-solvers were able to play out their strengths.

Although the advent of new methods and optimized implementations made SAT-solvers very successful on these "real-world" instances, large classes of SAT instances have remained (e.g., unsatisfiable random 3-SAT problems with a clause-variable-ratio near the phase transition point [14, 32, 42, 45]) on which these solvers fail—even on instances that are considerably smaller (by four to five orders of magnitude). This is not very surprising, as SAT is an NP-complete problem [55]. The reasons for this phenomenon, however, are at least partially understood, and besides results that are often not directly applicable to large industrial instances (e.g. treewidth), there are no a priori criteria available to decide whether an instance is tractable or not. In fact,

determining the hardness of a particular instance may be even more complex than solving the SAT instance itself.

The standard argument found in the literature to explain this dichotomy is that real-world instances are equipped with some kind of internal (and sometimes hidden) "structure" that makes these problems tractable [67]. The term "structure", due to its vagueness, leaves much room for interpretation, though, and it remains unclear how this structure manifests itself and how it could be exploited. Among the methods that were proposed are randomization [35], clause learning [43], symmetry and component detection [1, 10, 16, 56], and tree decomposition [52, 63]. The first two techniques (clause learning and randomization) can be found in most implementations of modern SAT-solvers for real-world instances today [26, 34, 47]. Concepts explaining the boundary between tractability and intractability (besides graph-based properties like treewidth) include backbone variables [46] and backdoor sets [70]. Although highly valuable from both an epistemological and a practical point of view, these concepts do not deliver an a priori criterion to directly "read off" the computational hardness of a given instance.

We therefore propose a novel, mainly empirical approach in order to shed some light on an instance's internal structure [60]. A major ingredient of our method is the visualization of internal variable- and clause-dependencies as they emerge from a graph transformation of the SAT problem. From the graph we hope to be able to derive new criteria for problem hardness.

Different graph representations of SAT instances have been proposed in the literature, including variable interaction graphs [52], resolution graphs [64], implication graphs [3], factor graphs [12], or hypergraph variants of these [31, 50][1]. We have decided to use variable interaction graphs and resolution graphs for the visualization approach presented in this paper, as these graphs are both amenable to layout algorithms (as opposed to hypergraphs) and general enough (as opposed to implication graphs). To graphically render graphs we use existing graph layout algorithms or, more specifically, force-directed placement procedures [24, 29]. These procedures are known to reflect clustering and symmetry—properties that we are interested in—especially well [29].

Besides computing static layouts, we have developed a tool called DPvis which is able to generate animations showing the dynamic change of a problem's structure during a run of the DPLL (Davis-Putnam-Logemann-Loveland) procedure. The DPLL procedure is used

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[1] Unfortunately, there is no established nomenclature for these graphs. Szeider [63], e.g., uses the name "primal graph" for our variable interaction graphs and the notion "incidence graph" for what we call factor graph; Galesi and Kullmann [30] call resolution graphs "conflict graphs".

(with variations and extensions) by almost all SAT-solver implementations for real-world problems today.

The rest of this paper is organized as follows: In the next section we introduce basic notions of SAT-solving and graph layout. Then we present our implementations DPvis and 3Dvis which compute two- and three-dimensional graph layouts of SAT instances. We then show results obtained by our visualization and summarize observations we have made. Finally, we report on related work and conclude.

2. Theoretical Background

In this section we define basic notions of SAT-solving, present different transformations from SAT instances to graphs, and give a short introduction into graph layout algorithms, as far as it is needed here. We also state known results on treewidth and tree decompositions.

2.1. SAT AND THE DPLL ALGORITHM

The propositional logic satisfiability problem (SAT) asks whether a formula in conjunctive normal form (CNF)—a SAT instance—is satisfiable, i.e. whether there exists an assignment to the variables such that the whole formula evaluates to true. More formally, a SAT instance is defined as follows:

DEFINITION 2.1. *Given a finite set X of propositional variables, a* **SAT instance** $S = \{C_1, \ldots, C_m\}$ *(over X) is a finite set of clauses, where a* **clause** $C = \{l_1, \ldots, l_k\}$ *is a finite set of literals, and a* **literal** l *is either a variable $x \in X$ or its negation $\neg x$ (with $x \in X$). We denote the set of literals (over X) by $L := X \cup \neg X = X \cup \{\neg x \mid x \in X\}$.*

Logically, a clause $C = \{l_1, \ldots, l_k\}$ is interpreted as the disjunction of its literals, i.e. as $(l_1 \vee \ldots \vee l_k)$, and a SAT instance $S = \{C_1, \ldots, C_m\}$ as the conjunction of its clauses, i.e. as $C_1 \wedge \ldots \wedge C_m$.

The problem of determining whether a formula in CNF is satisfiable is the classical NP complete problem [55]. Different algorithms have been proposed to solve it [18, 17, 54], with the Davis-Putnam-Logemann-Loveland (DPLL) algorithm being the one mainly used in practical applications today. We have depicted the basic DPLL algorithm in Figure 1. It has been extended in various ways in modern implementations, the most important ones being clause learning and non-chronological backtracking [43], fast Boolean constraint propagation [47], and random restarts [35].

```
boolean DPLL(ClauseSet S)
{
  while (S contains a unit clause {l}) {
    delete clauses containing l from S      // unit-subsumption
    delete l̄ from all clauses in S          // unit-resolution
  }
  if (∅ ∈ S) return false                   // empty clause?
  if (S = ∅) return true                    // no clauses left?
  choose a literal l occurring in S         // case-splitting on l
  if (DPLL(S ∪ {{l}}) return true           // first branch
  else if (DPLL(S ∪ {{l̄}}) return true      // second branch
  else return false
}
```

Figure 1. Pseudo-code of the basic DPLL algorithm (without clause learning).

2.2. GRAPH REPRESENTATIONS OF SAT INSTANCES

In order to obtain graph representations from SAT instances, a mapping from the latter to the former is needed. As an intermediate step in generating such a mapping it is useful to consider hypergraphs [31] first, as they allow for a natural, lossless transformation from the propositional logic domain to a graph-like setting (see also [50]).

DEFINITION 2.2. *A **hypergraph** $H = (V, E)$ is a pair of a vertex set V and a set of hyperedges E, where E is a subset of the powerset of V, i.e. $e \subseteq V$ for all $e \in E$.*

This suggests a natural translation of a SAT instance S to a hypergraph H, by setting the vertex set V of H to the set of literals of S and letting the clauses of S generate the hyperedges of H. We thus obtain $H = (L, S)$ as a natural representation of S as a hypergraph.

Unfortunately, it is hard to render hypergraphs graphically, except for the case where all hyperedges are of size two, in which the hypergraphs coincide with ordinary graphs. Thus, different ways have been proposed in the literature [46, 52, 62] to obtain ordinary graphs by modifying the hypergraph representation in some way. In what follows, we assume a SAT instance consisting of a clause set S over a set of variables X. Figure 2 illustrates these graph representations on an exemplary formula.

Factor graph. Factor graphs have been used in the context of SAT solving by Braunstein and Zecchina *et al.* [12] and Szeider [63] (among others). A factor graph $G_F = (V, E)$ is a bi-partite graph, in which the vertex set consists of the union of the instance's clauses and variables, thus $V = X \cup S$. An (undirected) edge

is drawn between variable x and clause c if and only if $x \in c$ or $\neg x \in c$. It is obtained from the hypergraph representation $H = (S, L)$ by adding a new vertex for each hyperedge (i.e. for each clause), connecting the new vertex with all elements of the hyperedge, ignoring signs of literals. In a slight variant of the factor graph (called *directed factor graph*), a directed graph is used instead of an undirected one, where the direction of the arc indicates whether the variable occurs positively or negatively in the clause.

Variable interaction graph. The variable interaction graph $G_I = (X, E)$ is obtained from the hypergraph $H = (L, S)$ by replacing each hyperedge e^* with a set of ordinary edges, one edge for each pair of elements of e^*, and merging nodes of positive and negative literals for each variable [52]. Thus, an edge $\{x, y\}$ is drawn between two variables x and y, if they occur together in at least one clause.

Resolution graph. In the resolution graph $G_R = (S, E)$ an (undirected) edge is drawn between two clauses C_1 and C_2 if and only if there is a variable $x \in X$ such that $x \in C_1$ and $\neg x \in C_2$. Clauses C_1 and C_2 which are adjacent in G_R can thus be resolved. (Note that we also allow tautological resolvents here.)
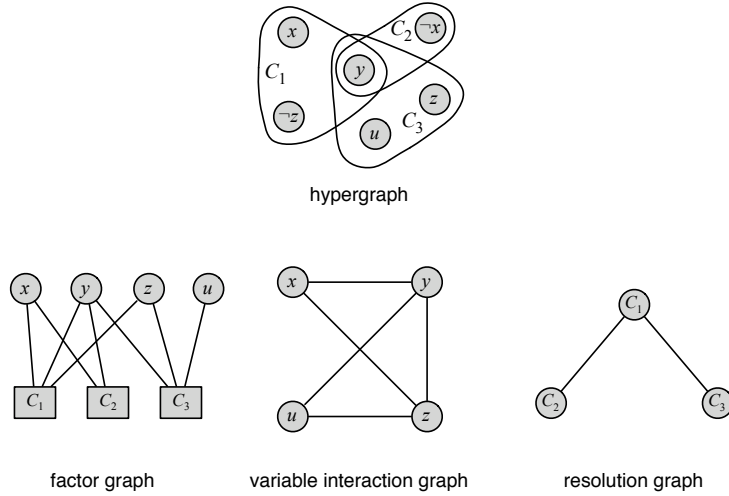

Figure 2. Different hypergraph and graph representations of the SAT instance $S = (C_1, C_2, C_3) = (\{x, y, \neg z\}, \{\neg x, y\}, \{u, y, z\})$.

Whereas directed factor graphs are lossless representations of SAT instances, both (undirected) factor graphs, variable interaction graphs

and resolution graphs are lossy representations of SAT instances—in the sense that the mapping from SAT instances to graphs is not injective. In the case of factor graphs and variable interaction graphs, signs of literals are ignored (and thus cannot be "reconstructed"), and clauses are not represented uniquely as the following example shows: the 3-clause $\{x, y, \neg z\}$ and the set of three two-clauses $\{\{\neg x, y\}, \{x, \neg z\}, \{y, z\}\}$ share the same interaction graph and thus cannot be differentiated. For resolution graphs, as parallel edges are merged, the transformation is also not invertible. Lossy representations, however, allow to abstract away certain properties that are not currently in focus.

In the variable interaction graph, a path from a variable x to a variable y means that assigning a value to x may influence possible assignments to y (e.g. exclude that y is set to true). Conversely, if there is no path from x to y, these variables are independent, which also means that the SAT problem for the components containing x and y, respectively, can be solved independently. In the resolution graph, a path from a clause C to a clause D indicates that literals of C and D may be merged by a series of resolution steps (cf. del Val's no-merge resolution for knowledge compilation [20], or Plaisted and Zhu's ordered semantic hyper-linking [51]).

2.3. TREEWIDTH AND TREE DECOMPOSITIONS

Treewidth is a notion that was introduced by Robertson and Seymour in their work on graph minors [53]. The treewidth $\mathrm{tw}(G)$ is a structural parameter of a graph G. It plays an important role in algorithmic graph theory, as many graph algorithms become tractable when restricted to graphs of bounded treewidth.

Treewidth is defined via *tree decompositions*, where a tree decomposition of a graph $G = (V, E)$ is defined as a pair (T, χ), where T is a tree, χ a labeling of the vertices of T by sets of vertices of G. (T, χ) is a tree decompostion of G provided the following conditions hold:

- For every vertex $v \in V$ there is a vetex t in T with $v \in \chi(t)$.

- For every edge $(v, w) \in E$ there is a vertex t in T such that $\{v, w\} \subseteq \chi(t)$.

- For any vertices t_1, t_2, t_3 in T, if t_2 lies on a path from t_1 to t_3, then $\chi(t_1) \cap \chi(t_3) \subseteq \chi(t_2)$.

The *width* of a tree decomposition (T, χ) is defined as the maximum of $|\chi(t)| - 1$ over all vertices t in T. The *treewidth* $\mathrm{tw}(G)$ of G is the minimum width over all its tree decompositions.

For a fixed k, deciding whether a graph has treewidth at most k can be decided in linear time [11]. However, computing the treewidth of a given graph is an NP-hard problem [2].

Tree decompositions can be used to obtain fast algorithms for subclasses of otherwise intractable problems. For SAT, Gottlob *et al.* have shown, e.g., that clause sets with bounded treewidth of the variable interaction graph are fixed-parameter tractable [36]. Szeider proved that clause sets with bounded treewidth of the factor graph are fixed-parameter tractable [63].

A problem is called *fixed-parameter tractable (FPT)* [23, 49], if its run-time depends exponentially only on the parameter k, but is otherwise polynomial, i.e. it is $\mathcal{O}(f(k) \cdot l^{\alpha})$, where f is any function, l is the size of the problem instance (for SAT the number of occurring literals), and α is a constant independent of k.

Treewidth is also closely related to bucket elimination algorithms for SAT. Dechter [19, 52], e.g., has presented such an algorithm. Zabiyaka and Darwiche have defined the notion of *functional treewidth* [72], and give results of an algorithm based on this notion for circuit benchmarks from the LGSynth93 suite. Narodytska and Walsh [48] have applied an algorithm that exploits structural properties related to treewidth to automotive configuration problems. Array Logic [27], working with decompositions and partial solution tables, is also closely related to tree decompositions and has also been applied to configuration problems. It seems that especially in the application area of product configuration, treewidth is a promising concept.

2.4. Graph Layout Algorithms

The *graph layout* or *graph drawing* problem consists of generating a geometric representation of a graph in two or three dimensions. Nodes have to be positioned in the Euclidean space while optimizing certain layout properties like minimal number of edge crossings, uniform edge length, reflection of inherent symmetry, etc [29, 22].

Different algorithms are available for graph layout, a prominent one being the *spring-embedder model* of Eades [24] or its close relative, the *force-directed placement* algorithm of Fruchterman and Reingold [29]. Both are known to produce layouts that reflect symmetry very well.[2] The physical model used by the spring-embedder assumes metal springs of a certain length attached between each pair of connected nodes. The springs impose attractive and repellent forces on the nodes depending on their current distance in the layout. The layouter attempts to mini-

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[2] We have considered other existing layouts as well, like hierarchical or orthogonal layout, but found them not being equally suitable for our purpose.

mize the sum of all affecting forces (i.e. the energy of the whole system) by iteratively repositioning the nodes.

Unfortunately, using only local spring forces is not sufficient to obtain a globally untangled graph [68]. As an example, Walshaw [68] considers a chain of three vertices a, b and c which are connected by two edges $\{a, b\}$ and $\{b, c\}$. Now, having only local spring forces, a placement where a and c are put at the same location and b one spring length away would be a state of minimal energy and thus considered optimal. However, having a and c put at the same place is typically not regarded an acceptable layout. On a larger scale, repulsion is necessary to push whole regions that are not immediately connected away from each other. The standard technique [24, 29, 68] to avoid such situations is to add global repellent forces between all vertices. These are typically simulated by a physical model that considers nodes as equally charged particles that push away from each other. A drawback of this approach is that a simplistic algorithm to compute global forces requires quadratic time in the number of vertices. However, there are more advanced algorithms like the Fast Multipole Method (FMM) [37] or the Barnes-Hut-algorithm [4] that can avoid the quadratic behavior—at the cost of a more complicated implementation, though.

3. Implementations

We have developed two tools for visualizing SAT instances: DPvis, which generates two-dimensional layouts of SAT instances and which can also animate runs of the DPLL algorithm, and 3Dvis, which produces three-dimensional layouts.

3.1. DPvis: Visualizing the DPLL Algorithm

DPvis is a Java tool to visualize the structure of SAT instances and runs of the DPLL procedure. It builds upon the commercially available graph layout package yFiles of yWorks (`http://www.yworks.com`), from which it uses the *Organic Layouter* and *Smart Organic Layouter*, both of which implement force-directed placement algorithms. DPvis is also able to generate animations showing the dynamic change of a problem's structure during a DPLL run. Besides implementing a simple variant of the DPLL algorithm on its own, DPvis also features an interface to MiniSAT [26], a state-of-the-art DPLL implementation, by which runs of MiniSAT can be visualized—including the generated search tree and the effects of clause learning. A screenshot of DPvis is shown in Figure 3.
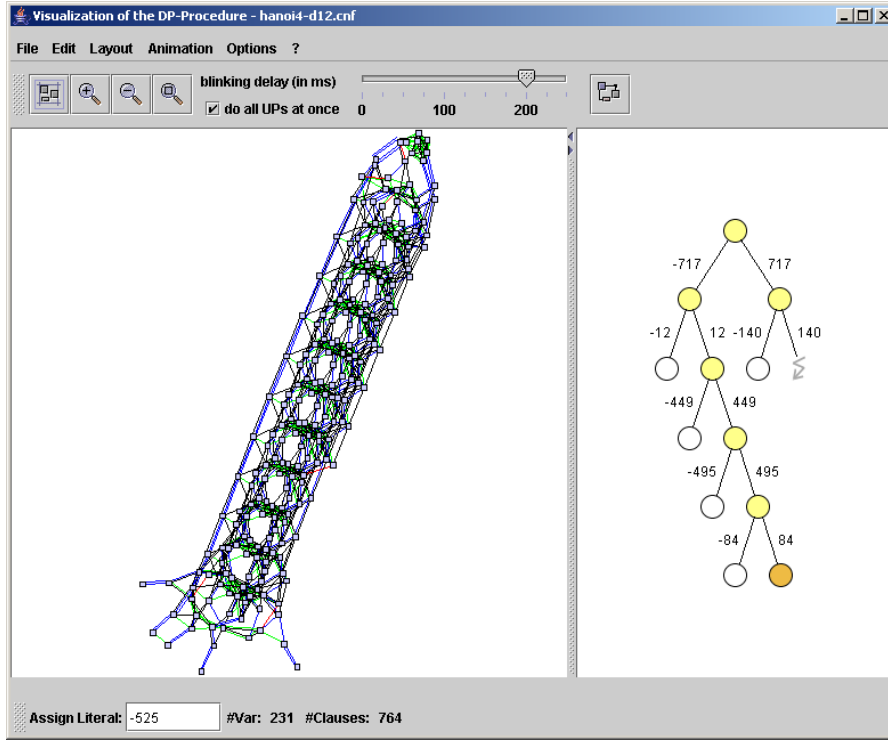
Figure 3. DPVIS tool showing a visualized SAT instance (`hanoi4` of the DIMACS benchmark collection[3]): The variable interaction graph is shown on the left and a manually generated, partial search tree on the right.

DPVIS uses a refined variant of the variable interaction graph, in which 2-clauses (aka binary clauses, i.e. clauses containing exactly two literals) are represented as visually emphasized directed or undirected arcs in the graph. Different colors are used depending on the signs of the literals occurring in the 2-clause. Special treatment of 2-clauses is motivated by their importance for tractability: A problem consisting only of 2-clauses is solvable in linear time [3]. Moreover, experiments with random instances from the $(2+p)$-model (problems with a fraction of p 3-clauses and $(1-p)$ 2-clauses) indicate that random instances with up to forty percent of 3-clauses (i.e. $p \leq 0.4$) might be computationally tractable [46]. Binary clauses occur to a considerable extent in real-world SAT instances (for example in hardware verification) as well.

Besides providing two different layout algorithms, DPVIS allows zooming into the interaction graph, performing unit propagation, and

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[3] The `hanoi4` instance represents the well-known Towers of Hanoi game with four disks, encoded as a planning problem. Individual actions of the plan as well as their dependencies are clearly visible as linearly arranged clusters in the graph layout.

manually setting variables to true or false. During all these operations, the variable interaction graph is updated to reflect the current partial assignment. Moreover, DPVIS allows to navigate freely in the search tree generated by the DPLL algorithm and thus to compare reduced instances (due to partial variable assignments) at different points of the search tree.

The interface to MiniSAT allows play-back of DPLL traces generated by this SAT-solver. Such traces contain information about case-splitting, unit-propagation, learned clauses and back-jumps, all of which can be animated and analyzed with the help of DPVIS.

DPVIS was developed in collaboration with E.-M. Dieringer and was mainly implemented by her. DPVIS is available as a Java applet and can be downloaded from `http://www-sr.informatik.uni-tuebingen.de/ ~sinz/DPvis`. Details on DPVIS are described in a different paper [60].

3.2. 3DVIS: THREE-DIMENSIONAL GRAPH LAYOUT

Our second implementation, 3DVIS, generates three-dimensional layouts. It implements the multilevel force-directed graph-drawing algorithm by Walshaw [68], is written in C++ and makes use of OpenGL. There is a Linux version of 3DVIS with a simple user interface based on the OpenGL Utility Toolkit (GLUT), and a Mac OS X version with a Cocoa/Objective-C user interface (see Figure 4).[4]

In a first step, Walshaw's multilevel algorithm computes a sequence $G_0, \ldots, G_l$ of increasingly coarsened graphs, starting with the initial variable interaction graph G_0, and repeating until the size of the coarsest graph consists of only two nodes. Each coarsening step works by computing a matching (not necessarily perfect), where each vertex is matched with one of its neighbors (such that no vertex has more than one neighbor in the matching, but solitary vertices may remain). Computing such matchings reduces the size of the graph (i.e. the number of vertices) at most by half in each coarsening step. So after approximately $\mathcal{O}(\log_2 |V|)$ steps the coarsest graph is reached.

Then, in reverse order, layouts are computed, for the coarsest graph first, continuing until a layout for the original graph is obtained. In each layout step, nodes for G_i are initially positioned according to the positions computed for G_{i+1}. Then the force-directed layouter is started on G_i with this approximate placement as initial layout. By computing approximate layouts for coarser graphs first, the whole layout process can be accelerated. Details on Walshaw's algorithm can be found in one

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[4] The Linux version of 3DVIS can be downloaded from `http://www-sr. informatik.uni-tuebingen.de/~sinz/3Dvis`. The Mac OS X version is available from the author of this paper on request.
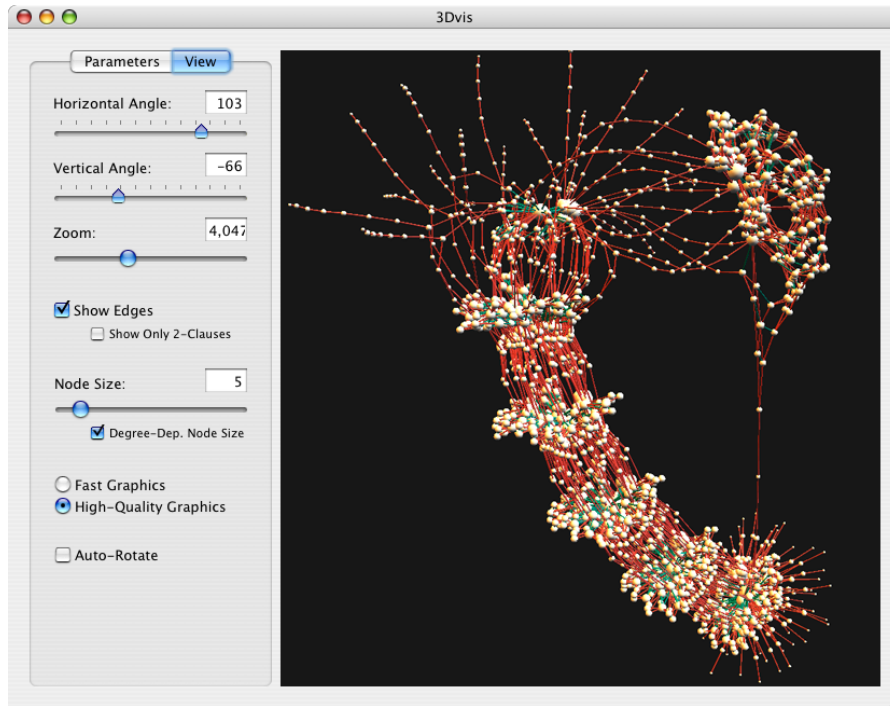
Figure 4. 3DVIS showing an instance on equivalence checking of two hardware multipliers (`longmult5`, available at `http://www.cs.cmu.edu/ modelcheck/bmc.html`).

of his papers [68]. Figure 5 shows an example of the iterative multilevel layout algorithm in action. On the top, layouts for the coarsened graphs G_7, G_5 and G_3 are shown, on the bottom the final result, a layout for G_0, is depicted.

4. Experiments

In this section, we report on experimental results obtained with our implementations DPVIS and 3DVIS. We start with layout examples, and then present run-times of our implementation of Walshaw's three-dimensional layout algorithm.

4.1. GRAPH LAYOUT EXAMPLES

We started our experiments on visualization with an example from hardware verification that stems from equivalence checking of a 16-bit sequential shift-and-add multiplier with a combinatorial multiplier (see
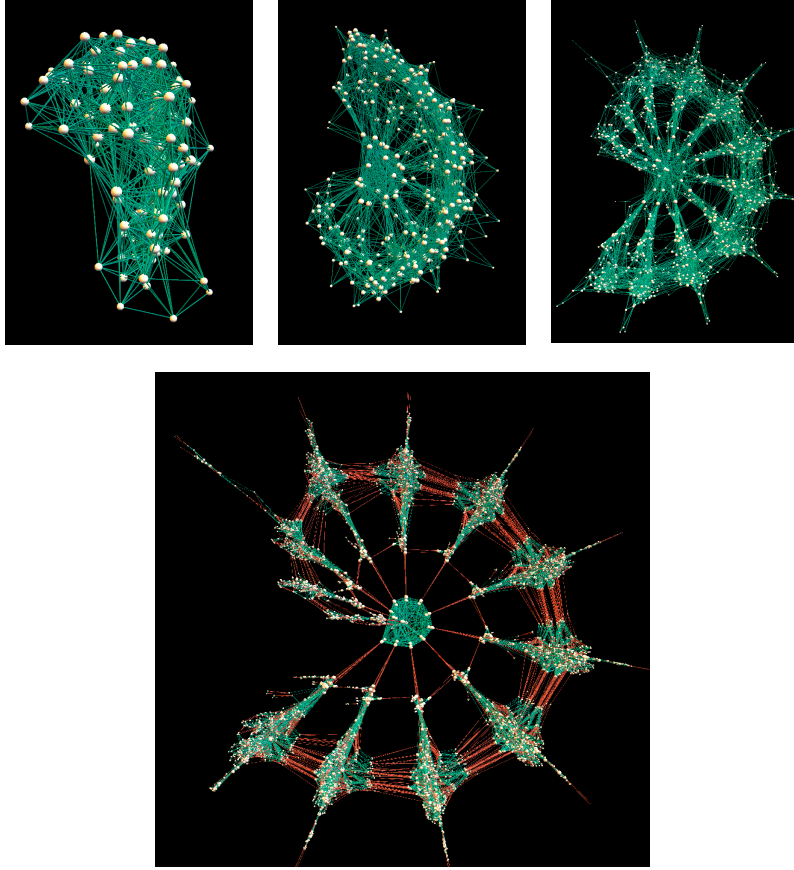
Figure 5. Layouts computed by the multilevel algorithm of 3Dvis. On the top row, layouts of coarsened graphs for SAT instance `bmc-ibm-5` on levels $l = 7, 5, 3$ are shown, the final layout ($l = 0$) is shown on the bottom. `bmc-ibm-5` is an instance from bounded model checking [9], and the 12 time steps of the unrolled transition relation are clearly visible as clusters on an outer circle. Adjacent time steps are connected by 2-clauses (shown in red) that interrelate current and next state variables. The last three time steps (top left) are smaller due to a bounded cone of influence optimization. The checker automaton, which is connected to all time steps, is clearly visible in the center.

[9] for further information). We used the file `longmult8`, representing equivalence of bit 8 of the two circuit designs.[5]

Whereas one single variable interaction graph already reveals a lot of information about the instance's structure, we observed that by visualizing depth-bounded runs of a DPLL-style algorithm and comparing different interaction graphs of the same instance at different states

[5] http://www.cs.cmu.edu/~modelcheck/bmc/bmc-benchmarks.html

during search delivers considerably more information. We therefore simulated such depth-bounded runs of a typical DPLL algorithm in our experiments. The depth-bounded search tree obtained that way for the `longmult8` instance is shown in Figure 6.
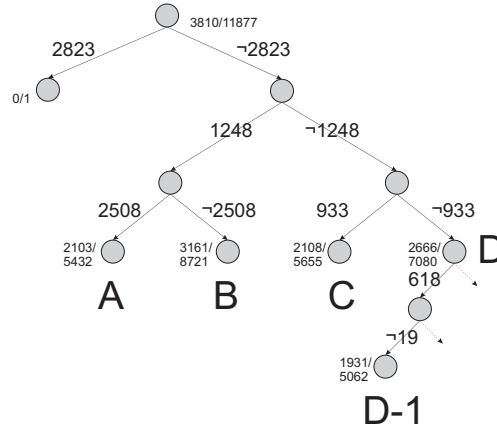

Figure 6. Search tree of a depth-bounded run of the DPLL algorithm on the `longmult8` benchmark problem.

The picture shows the search tree up to depth 3 (one branch extended down to depth 5), with the initial instance as the root node of the tree. Each node is labeled with two numbers (n/k), where n indicates the number of propositional variables of the instance and k the number of clauses. Child nodes are generated by case distinction (on the indicated variable) and are simplified by subsequent unit propagation. On search depth 3, we have four non-trivial clause sets (A, B, C, D) with between 2103 and 3161 variables. To illuminate the dynamics of the interaction graphs, we have added a further node at an increased search depth of 5, named D-1. Variable interaction graphs for these five snapshots are shown in Figures 8, 9 and 10, whereas the original (complete) instance is shown in Figure 7. Diagram A-1 on top of Figure 10 additionally shows a magnified view of the top left part of Diagram A.

We performed additional experiments with another instance of hardware verification, the bounded model checking instance `bmc-ibm-2`. This instance encodes a verification problem (IBM CPU Part #2) from IBM's research laboratory in Haifa. The instance contains 3628 variables and 14468 clauses. It can—together with a short description about how it was generated—be downloaded from the Canadian SATLIB site.[6] The interaction graph of this instance is shown in Figure 11.

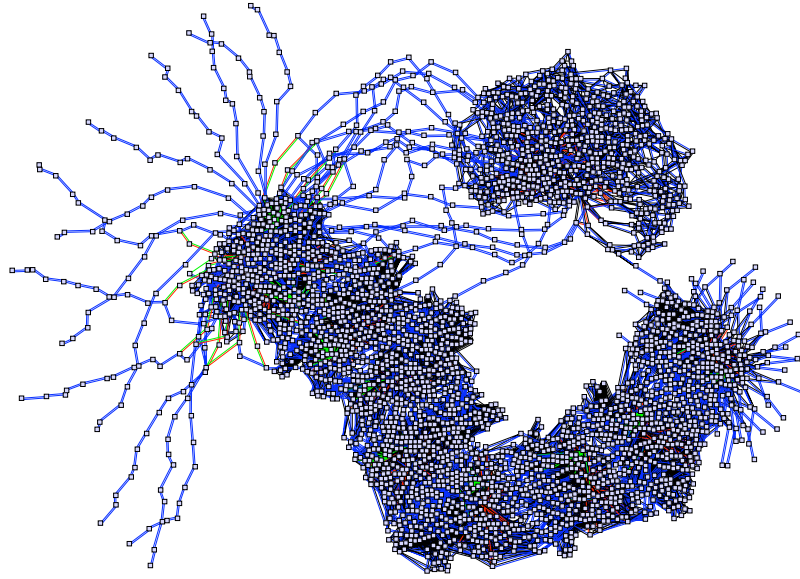[6] See respective link on `http://www.satlib.org`.

Figure 7. Variable interaction graph of the instance `longmult8` (top-level, after unit propagation).

For comparison reasons, we initiated experiments with further SAT instances outside the realm of hardware verification. We used an instance from automotive product configuration[7], one instance of the well-known pigeon hole problems (`hole10`) and a random 3-SAT formula with 100 variables and 425 clauses. The last two instances are known to be hard for resolution-based SAT-solvers, whereas the configuration instance is known to be very easy. The variable interaction graphs shown on the left of Figure 12 correspond to a state during the run of a DPLL algorithm where a few literals already have been fixed. After setting of three further variables and subsequent unit propagation the interaction graphs shown on the right resulted.

Besides generating variable interaction graphs, we also built resolution graphs. Figure 13 shows two resolution graphs for restriction A of instances `longmult8` and for instance `bmc-ibm-2`. Clustering and symmetry of the resolution graphs is similar to the respective variable interaction graphs. This suggests that properties of an instance like symmetries carry over from one representation to the other (for the component structure of a SAT instance this is obvious).

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[7] File `C202_FW`, downloadable at `http://www-sr.informatik.uni-tuebingen.de/~sinz/DC`.
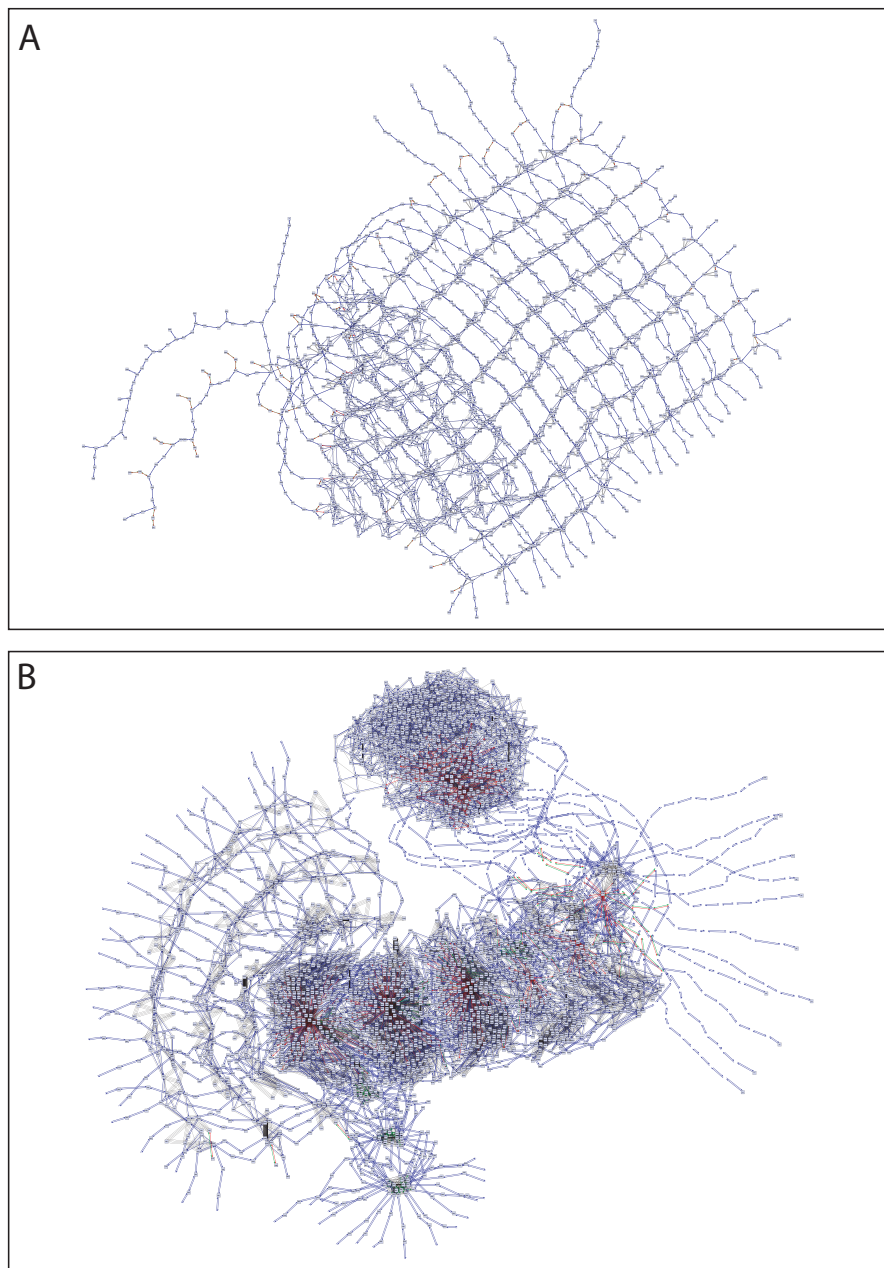
Figure 8. Variable interaction graphs for two sub-instances of `longmult8`, obtained by setting variable 2823 to false, variable 1248 to true, variable 2508 to true (A) or false (B), and subsequent unit propagation. In (A), the grid structure of the combinatorial multiplier is clearly visible, whereas the shift-and-add multiplier could be considerably simplified by fixing the value of the three variables. In (B), large parts of the shift-and-add multiplier have remained mainly unchanged, and individual time steps of the sequential circuit are clearly visible as large, connected clusters.
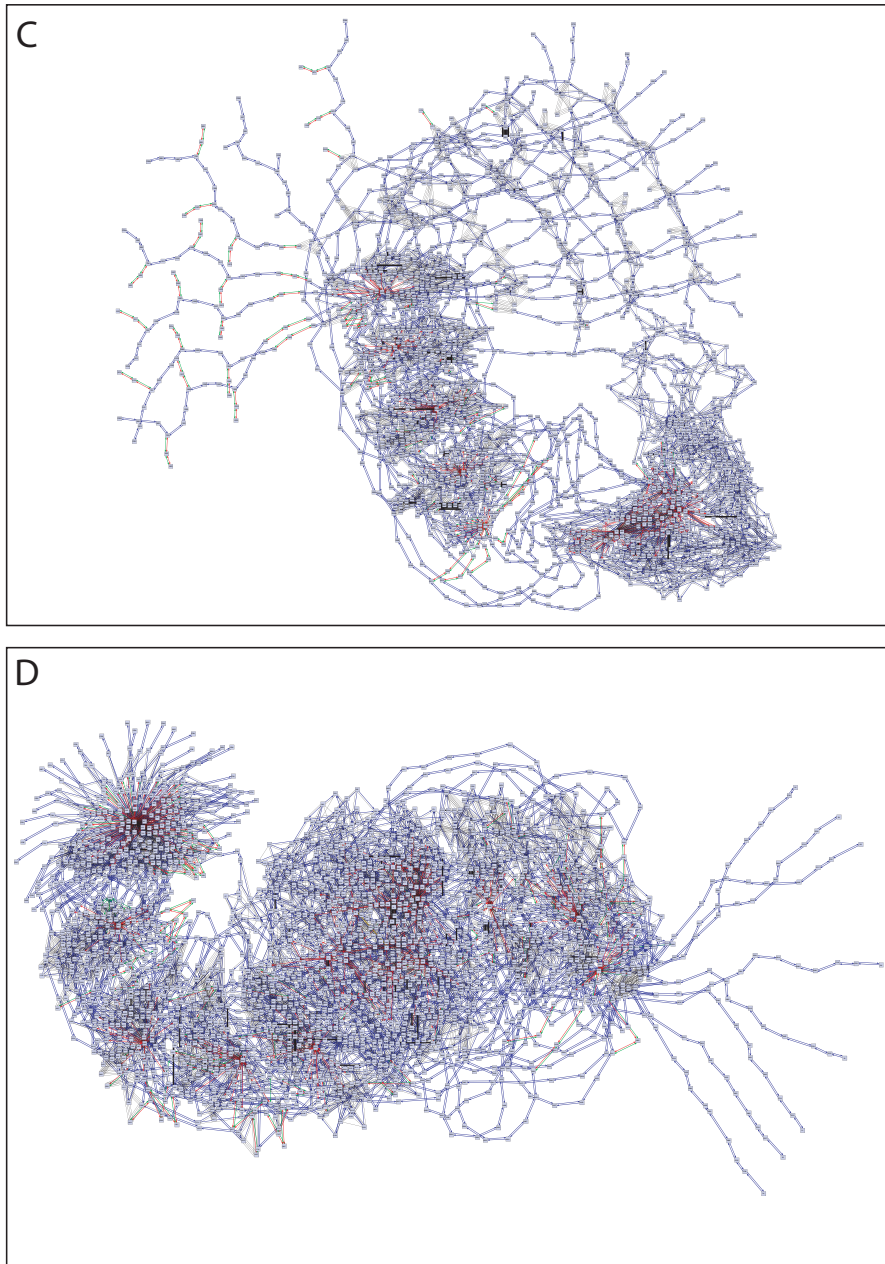
Figure 9. Variable interaction graphs for two sub-instances of `longmult8`, obtained by setting variables 2823 and 1248 to false, variable 933 to true (C) or false (D), and subsequent unit propagation. It is noteworthy that almost no simplification by unit propagation occurred in (D), which clearly contrasts (A) in Fig. 8, resulting from setting only two variables to opposite values.
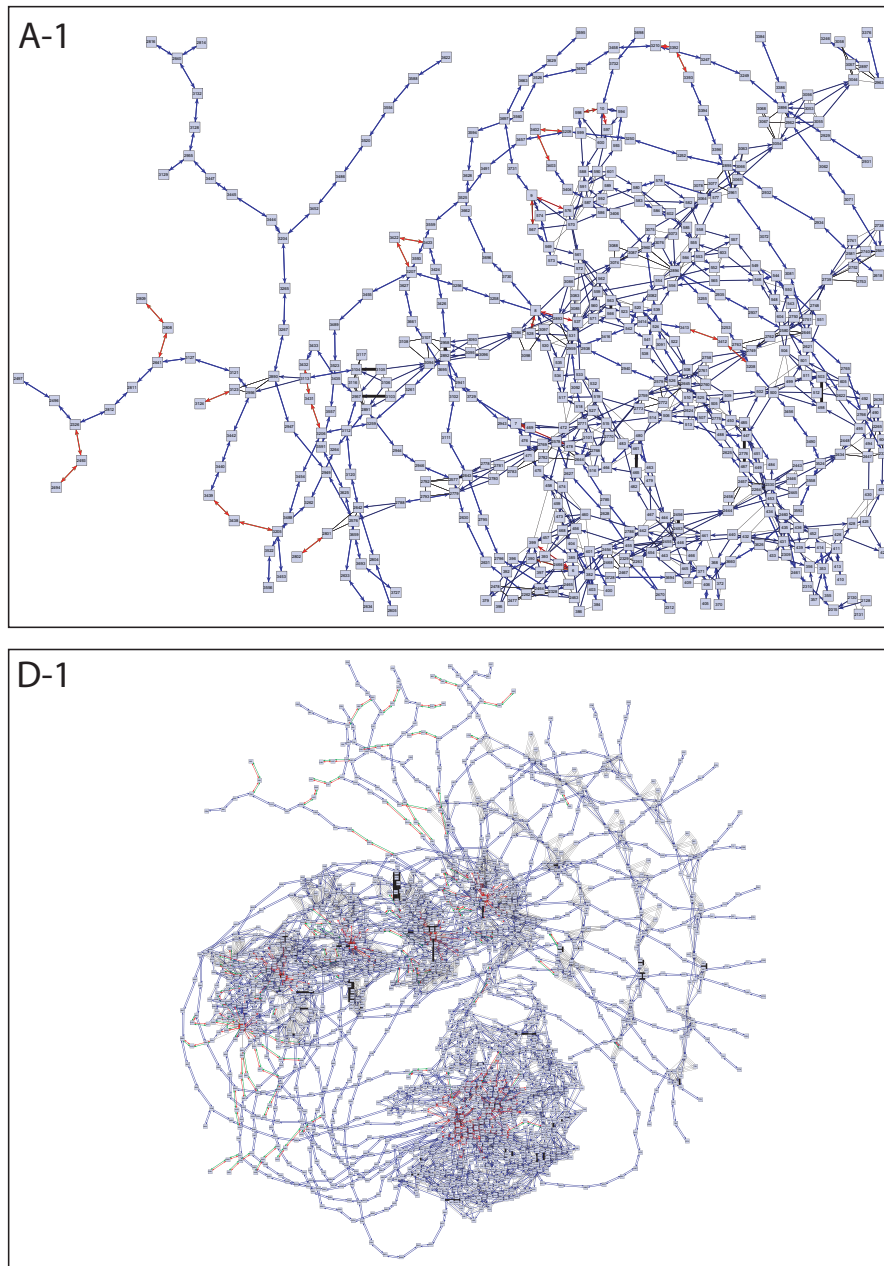
Figure 10. Two further variable interaction graphs: (A-1) displays a magnified view of the top left part of Diagram (A) of Figure 8, and (D-1) shows the instance obtained from (D (Figure 9) by additionally setting variable 618 to true, variable 19 to false, and subsequent unit propagation. Diagram (A-1) reveals long chains of variables connected by bi-implications. Each of these chains could be contracted to only one variable (by an equivalence detection algorithm) without changing the semantics of the partially processed SAT instance. These chains, however, emerge only after fixing the values of the two variables (and subsequent unit propagation), but do not occur in the original instance. Diagram (D-1) shows that sub-instance (D) is considerably simplified by fixing the values of only two further variables.
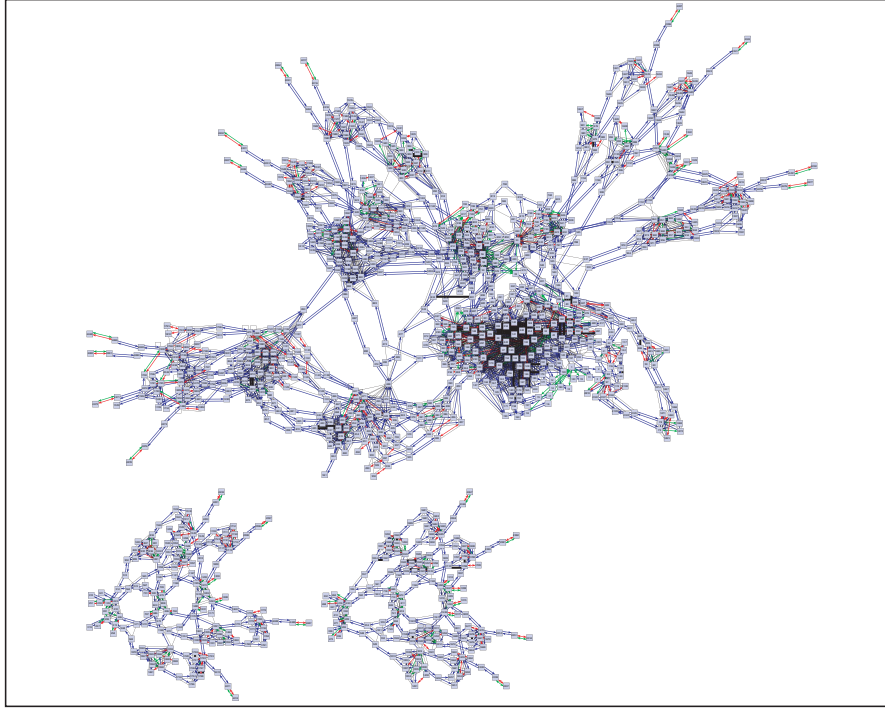
Figure 11. Variable interaction graph for the SAT instance `bmc-ibm-2`. It is noticeable that the instance—without further restrictions just by unit propagation—already decays into three independent components.

4.2. Run-Time of 3Dvis

In this section we report on the performance of our implementation 3Dvis of Walshaw's algorithm for three-dimensional graph layout. All performance measurements were done with the GLUT/C++ implementation under Linux on a machine with a Pentium 4 processor running at 3 GHz (hyperthreading switched off) and 2 GB of main memory. The results of our measurements can be seen in Table I.

Layouts for instances with up to ten thousand variables are computed in a few minutes, layouts for larger graphs are still feasible, but may require several hours to be computed. However, as can also be seen from Figure 5, layouts of coarsened graphs (e.g. on level $l = 3$) can already give a rough estimate how the final layout will look like and are computed much faster.
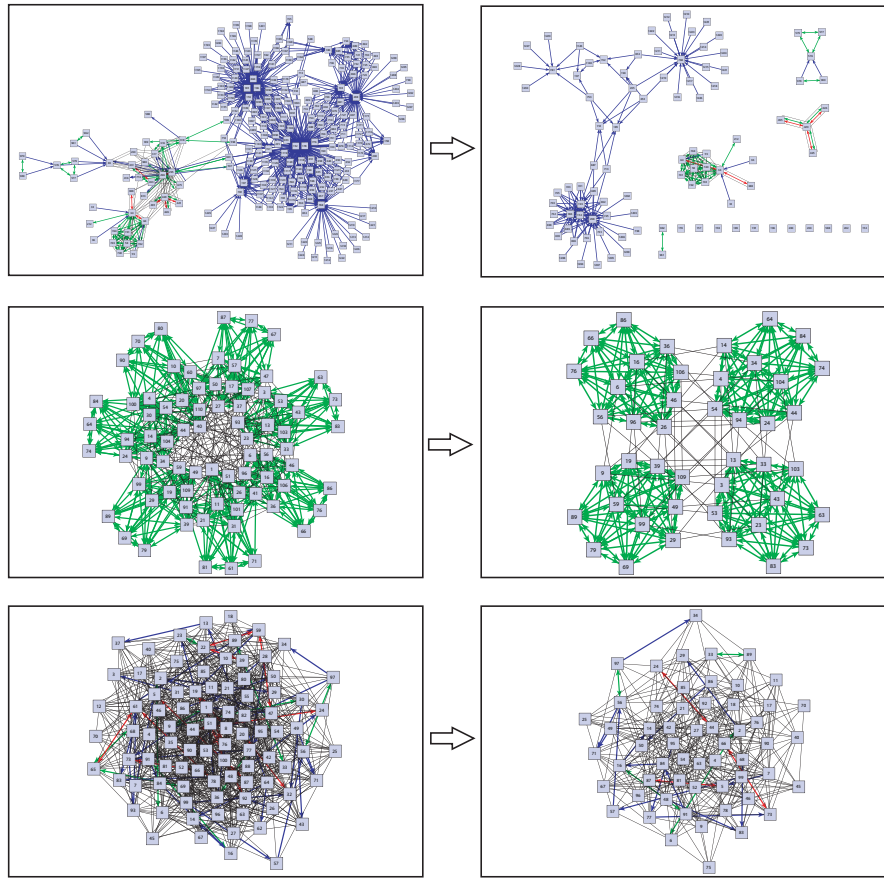
Figure 12. Variable interaction graphs for different SAT instances before (left) and after (right) three steps of a DPLL algorithm run (and subsequent simplification by unit propagation). On the top, an instance from automotive product configuration is shown, in the middle a pigeon hole formula, and on the bottom a random 3-SAT formula with a clause-variable-ratio near the phase-transition point. Whereas the product configuration instance (which is easy for current DPLL-based solvers) reduces considerably after fixing the value of three variables (and even decomposes into many independent sub-components), this effect does not show up on the other instances which are hard for DPLL. These hard instances reveal a "self-similar" behavior between the whole instance and the subproblems that occur during runs of the DPLL algorithm, which might partially explain their hardness.

5. Observations

We divide our observations in those made on the static graph presentations, and those that take the change of the graph structure into account (cf. Figures 8, 9, and especially Fig. 12).
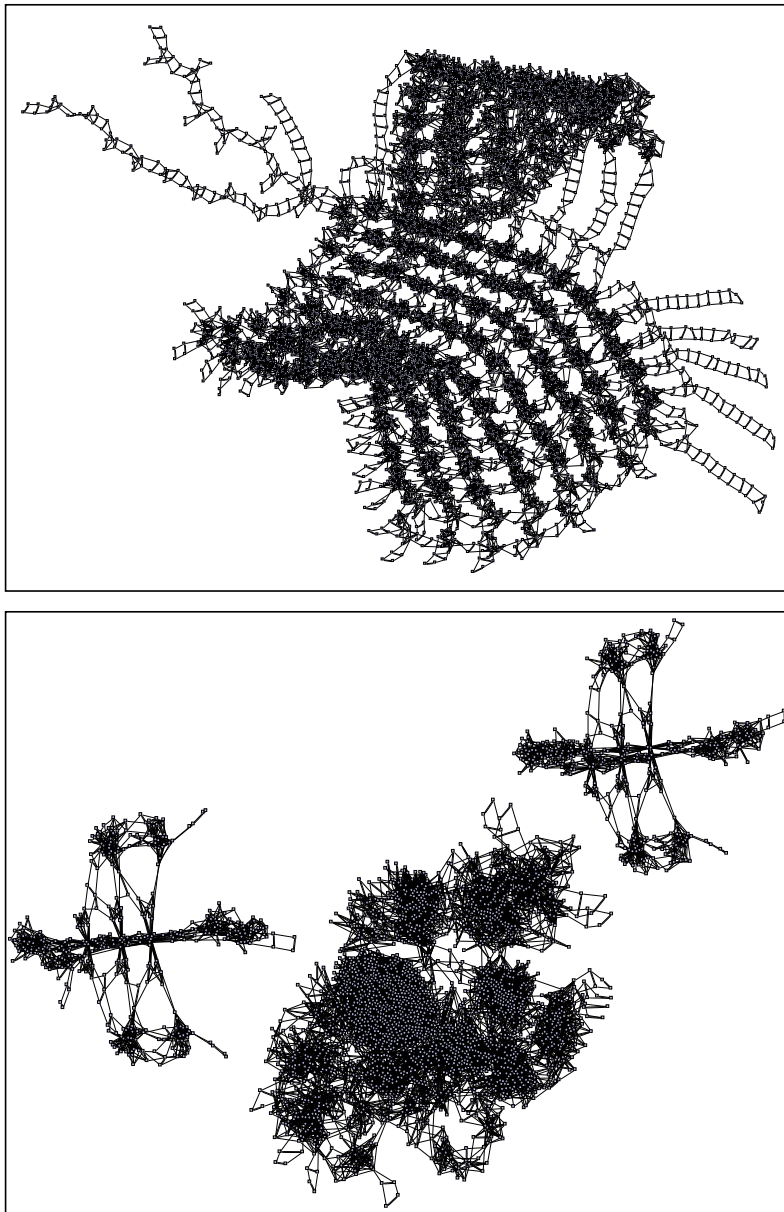
Figure 13. Resolution graphs for two SAT instances: `longmult8` with the same restriction as in Figure 8 (A) on the top, and `bmc-ibm-2` on the bottom. Note the similarity with regard to symmetry and clustering compared to the respective variable interaction graphs in Figures 8 and 11.

Table I. Run-times of 3Dvis on different SAT instances. The instances were selected from the industrial section of previous SAT Competitions [7]. The size of each instance (number of variables and clauses) is shown, as well as the size of the graph, the run-time (in seconds) to compute a layout on levels $l = 3$ and $l = 0$ (final layout), and the memory consumption (in MB). A dash indicates a time-out.

SAT instance	#vars	#clauses	#edges	run-time L3/L0	memory
vmpc-21	441	45339	32193	0.5 / 7.3	6.8
queueinvar-10	886	5622	17578	1.3 / 6.2	6.3
barrel-5	1407	5383	12201	1.3 / 15.2	6.4
longmult-4-up	1764	5081	5124	0.9 / 8.1	5.5
longmult-5-up	2181	6355	6429	1.1 / 9.8	5.7
barrel-7	3523	13765	70512	9.8 / 75.1	16.3
1dlx-c-liveness	6874	65479	134672	18.0 / 468.4	21.3
x1mul.miter	8760	55571	51610	18.0 / 218.6	13.2
bmc-ibm-5	9395	41207	55130	6.3 / 75.0	12.4
c7552mul.miter	11282	69529	70553	10.3 / 105.6	14.4
9dlx-iq1	24604	261473	687398	141.4 / 3822.6	85.6
bmc-ibm-6	51639	368352	726085	64.8 / 38972.1	83.2
bmc-galileo-8	58074	294821	379050	63.4 / 45568.2	62.2
bmc-galileo-9	63624	326999	427698	74.8 / —	68.5
clauses-2	75528	272784	392910	291.7 / 3247.1	79.6
9dlx-iq3	69789	968295	2599017	890.0 / —	319.8
9dlx-iq6-bug7	173811	5609632	9921587	4365.0 / 39404.3	1223.8
9dlx-iq6-bug9	235184	8063818	14453844	8390.4 / —	1757.1

5.1. STATIC ASPECTS

When considering graphs obtained from hardware verification instances we made the following observations:

1. There are noticeably many implication chains of considerable length (this is best seen in Diagram A-1 of Figure 10). In many cases these chains are even made up of equivalences. Many of them do not occur directly in the original instance, but only after setting of a few variables. This indicates that incorporation of equivalence handling (or, more generally, special treatment of 2-clauses) may be fruitful for such instances.

2. Decomposition into independent subproblems occurs frequently, at least on higher levels of the search tree. Some problem instances already decay into independent components after unit propagation (as, e.g., bmc-ibm-2, cf. Fig. 11). This indicates that detection and

special handling of independent components may be a useful feature to integrate into DPLL solvers.

Both aspects—implication chains and decomposition—have been considered in the SAT literature [10, 33, 50, 58], but are only partially implemented in today's solvers. Thus, it may be worthwhile trying to exploit these advantageous properties more directly in the future.

5.2. Dynamic Aspects

When considering the dynamic change of the graph structure of a SAT instance we observed the following:

1. Hard problem instances (pigeon hole, random 3-SAT) not only possess a lower rate of variable reduction by unit propagation, but also lack the decomposition feature that appeared, e.g., in the configuration and hardware verification instances (see Figure 12). The hard instances seem to possess a "fractal" or "self-similar" behavior on problem reduction by unit propagation.

2. We observed a huge amount of problem reduction caused by so-called *top-level assignments* (TLAs) [26] (cf. also Fig. 7 in [60]). TLAs are unit clauses that are learned during the search process. Each top-level assignment fixes the value of a variable for the whole instance and thus indicates that in each solution of the instance the TLA-variable must have that fixed value. (The notion of top-level assignment is closely related to that of a *backbone variable* [59]).

In other experiments [60] we perceived that although TLAs occur in many instances (also in random 3-SAT instances), the number of TLAs is much higher for (comparatively easy) real-world problems than for (comparatively hard) random 3-SAT instances. Comparing the variable interaction graphs of original instances with those where the detected TLAs were added, revealed a considerable simplification for the real-world instances, whereas the structure of random 3-SAT instances remained mainly unchanged [60].

5.3. Hypotheses

From these observations we derive the following (preliminary) hypotheses:

1. Both long implication chains (cf. Fig. 10, Diagram (A-1)) and decomposition into independent subproblems may explain the benign behavior of real-world instances. These are properties that we have

not yet observed in hard instances. It is important to consider decomposition not only at the top level (i.e. on the original instance), but also at deeper levels of the DPLL algorithm (cf. Fig. 12, top) when several variables are set and thus a partial assignment has been applied to the instance. The decomposition property at the top level is closely related to tree decompositions.

2. Hard instances seem to exhibit a "fractal", "self-similar" or "scale-free" [69] behavior on reductions by case-splitting and unit-propagation (cf. Fig. 12, middle and bottom) . For such instances the conformation of the interaction graph does not change considerably during the search process.

Making use of these hypotheses in future algorithms seems to be more conceivable for the first one (see Paragraph 5.1 above), whereas it is not so evident how to make use of the second one. However, we dare to hope that observations based on graph structure similar to ours may stimulate generation of new ideas in both theory and practice.

6. Related Work

Connecting graph-based concepts with SAT-solving is a relatively frequent topic in the SAT literature: Rish and Dechter [52] consider a directional resolution algorithm on instances with a special variable interaction graph structure, and gain tractability results for instances with bounded induced width (which is equivalent to bounded treewidth) and limited induced diversity ($\text{div}^* \leq 1$). Del Val [21] takes this approach a step further by examining acyclic component networks and by using literal interaction graphs instead of variable interaction graphs.

Galesi and Kullmann [30] study properties of the resolution graph resulting in the establishment of different tractable subclasses (e.g. for clause sets F with hermitian rank $h(F) \leq 1$).

Previous work on connected components for the SAT problem was mainly conducted in the context of model counting [6, 39, 56], although there are also approaches for constraint satisfaction problems in general [28, 38]. Bayardo and Pehousek extended the SAT solver Relsat 2.0 developed by Bayardo and Schrag in order to count models using connected components [39]. Their algorithm tries to detect components recursively at each node of a DPLL search tree. However, they do not take clause learning into account. Sang *et al.* carry on the recursive decomposition approach of Bayardo and Pehousek, and combine it with clause learning and component caching. Slater [61] compares different

SAT solvers on clustered problem instances, without experimenting with specialized algorithms that exploit the structure, however.

Park and van Gelder [50] apply hypergraph partitioning algorithms to decompose a SAT instance into independent subproblems. They claim that using the dual hypergraph (in which the vertices are clauses and hyperedges encompass clauses with common variables) induces a more natural decomposition, as a (minimal) cut in the dual hypergraph coincides with a set of variables that has to be assigned in order to break the instance into independent components. However, their algorithm seems to be not competitive in practice. Biere and Sinz [10] modify a zChaff-like SAT-solver to detect independent components and present techniques to handle these components.

Another graph-based approach is taken by Walsh [67], who carries over the influential work of Watts and Strogatz on "small world" networks [69] to combinatorial search problems. Walsh examines different classes of search problems, e.g. CSP translations of quasigroup problems, with respect to their "small world" properties (characteristic path length and clustering coefficient of the interaction graph).

Work on visualization of SAT instances was done by Slater [62] and, to some extent, by Selman [57]. Slater uses different graph translation techniques (variable interaction graph, literal interaction graph, and further ones) and visualizes the resulting graphs with the GraphVis software package from AT&T. However, the hierarchical layouter he uses is not as efficient in revealing symmetries as are force-directed placement algorithms. Selman [57] uses a specialized three-dimensional layouter to display variable interaction graphs. In his approach nodes with different degree are placed on different "height levels", and nodes with the same degree are equally distributed on circles growing with the number of nodes that have to be placed on them. Again, this layout cannot reveal symmetries and clustering as well as force-directed placement. Eén and Biere [25] have implemented a visual demo of their SAT pre-processor SatELite which graphically shows how clauses are processed by their algorithm.

Considering graph visualization in general, there are many graph layout packages available, e.g. Tulip or Graphviz, to name just a few.[8] Most of these packages focus on customizable layouts and do not allow for a tight integration with specialized SAT-related algorithms, however.

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[8] See, e.g., `http://directory.google.com/Top/Science/Math/Combinatorics/ Software/Graph Drawing` for a list of such packages.

7. Conclusion

We have presented an approach to visualize SAT instance in two and three dimensions by converting them to graph structures. We have generated visually attractive graph layouts using two different graph translations (variable interaction and resolution) by applying force-directed placement algorithms. Moreover, we have developed a tool, DPvis, which can generate animations of runs of the DPLL algorithm showing both the generated search tree and the temporal change of the SAT instance's structure.

We assume that our techniques can help in obtaining a better understanding of what makes a particular instance hard or easy. Moreover, we believe that our tool DPvis can be of great help in teaching and understanding the DPLL algorithm and its modern variants that incorporate clause learning.

Possible directions for future work include the design and implementation of faster graph layout algorithms (by using, e.g., fast multipole methods [37]), visualizing clause- and variable-activity in zChaff-like solvers to obtain a better understanding of clause learning, and trying to establish a theoretical link between graph properties and hardness of SAT instances.

Acknowledgements

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