Laboratory of Digital Logic Design Project 2 – Verilog HDL

Due: 23:55, Oct. 18, 2019

Write the Verilog gate-level descriptions of (1) 16-bit ripple carry adder (RCA) and (2) 16-bit carry lookahead adder (CLA). Perform simulations to verify the correctness of your designs and to observe the circuit delay under various input patterns. Note that the gate delay is mandatory in your simulation. A reference delay table is listed below. You may define your own delay time of each type of logic gates. Please submit your design report according to the following rules:

1- The font size of your report is 12 in PDF format.
2- The filename is your student ID (e.g., B12345678.pdf)
3- The Verilog modules of your designs.
4- The Verilog test bench to verify your designs.
   a. Use $dumpvars for visualized waveform
5- The screenshots of the simulation results.
6- Discuss the circuit delay of the two adders.
   a. Is CLA always faster than RCA?
   b. If not, explain your simulation results.
   c. If the circuit delay is not a fixed value, which one should we care about?
   d. Judge the two adders in terms of cost and performance.

Table 1: Logic gate delay.

Gate Type	Delay (ns)
NOT	5
2-input AND	10
3-input AND	15
2-input OR	15
3-input OR	20
2-input XOR	20

Reference:

[1] https://en.wikipedia.org/wiki/Carry-lookahead_adder
[2] https://en.wikipedia.org/wiki/Lookahead_carry_unit