Laboratory of Digital Logic Design Project 3 – Verilog HDL

Due: 23:55, Oct. 25, 2019

Write a Verilog behavioral description of an eight-bit arithmetic logic unit (ALU) and perform simulations to verify the correctness of your design. The circuit has a three-bit select bus (Sel), two eight-bit input datapaths (A[7:0] and B[7:0]), and one eight-bit output datapath (y[7:0]). The circuit module performs the arithmetic and logic operations listed below.

Sel	Operation	Description
000	y = 8'b0	Minimum value
001	y = A & B	Bitwise AND
010	y = A | B	Bitwise OR
011	y = A ^ B	Bitwise exclusive OR
100	y = ~A	Bitwise complement
101	y = A - B	Subtract
110	y = A + B	Add (Assume A and B are unsigned)
111	y = 8'hFF	Maximum value

Please submit your design report according to the following rules:

1- The font size of your report is 12 in PDF format.
2- The filename is your student ID (e.g., B12345678.pdf)
3- The Verilog module of your design.
4- The Verilog test bench to verify your design.
   a. Use $dumpvars system task for visualized waveform
   b. Use $display/$write system tasks
   c. Use $monitor system task
   d. Use $time system task
5- The screenshots of the simulation results.