Laboratory of Digital Logic Design Project 6 – Verilog HDL

Due: 23:55, Nov. 15, 2019

In this project, you are going to design 2 classic finite state machines. Each circuit has a one-bit input and a one-bit output. (1) Write the behavioral description of a Moore FSM described by Figure 1. (2) Write the behavioral description of a Mealy FSM described by Figure 2. There are 4 states (a, b, c, and d) in each circuit. Use keyword "parameter" to assign your own state numbers.

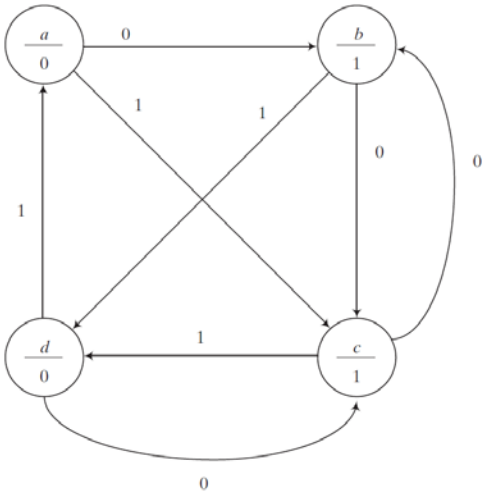

Figure 1. A Moore FSM.

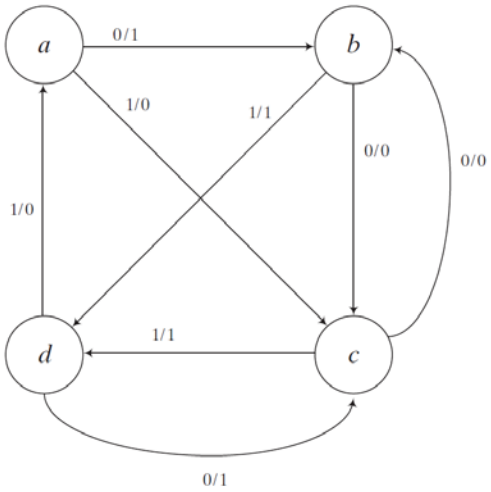

Figure 2. A Mealy FSM.

Please submit your design report according to the following rules:

1- The font size of your report is 12 in PDF format.
2- The filename is your student ID (e.g., B12345678.pdf)
3- The Verilog modules of your designs.
4- The Verilog test bench to verify your designs.
   a. Use $dumpvars system task for visualized waveform
5- The screenshots of the simulation results.