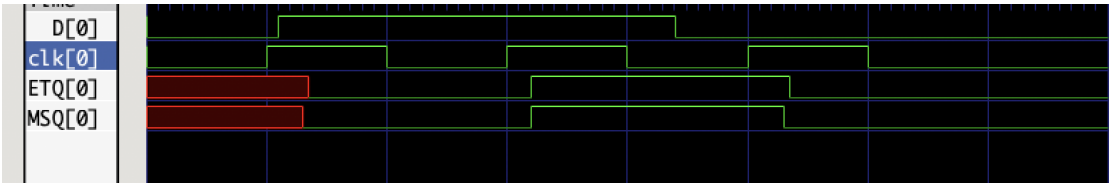
Verilog project4　　b10601002 廖品捷

Github: https://github.com/JamesLiao714/DLD-verilog

Waveform:



Test bench:

```
15
16  ////////////testbench/////////
17  module w4_TB();
18      reg D, clk;
19      wire ETQ;
20      wire MSQ;
21      //
22      MS_D ms1(D, clk, MSQ);
23      ET_D et1(D, clk, ETQ);
24      //
25  initial
26  begin
27      clk = 0;
28      repeat (6)
29      #100 clk = ~clk;
30  end
31  initial
32      begin
33          D = 0;
34          #110 D = 1;
35          #110 D = 1;
36          #110 D = 1;
37          #110 D = 0;
38          #110 D = 0;
39          #110 D = 0;
40      end
41  initial #800 $finish;
42  initial $dumpvars;
43  endmodule
44
```

(1) the gate-level description of master-slave D flip-flop（positive edge trigger）

```
58
59  //master slave
60  module MS_D(D, clk, Q);
61      input D, clk;
62      output Q;
63
64      wire w1, w2, w3, _c;
65      not #(5) n2(_c, clk);
66      Dlatch master(D, _c, w1, w2);
67      Dlatch slave(w1, clk, Q, w3);
68  endmodule
69
```

(2) the gate-level description of edge-triggered D flip-flop

```
//et D flip-flop
module ET_D(D, clk, Q);
    input D, clk;
    output Q, _Q;

    nand #(10) n1(w1, D, w2);
    nand #(15) n2(w2, w1, clk, w3);
    nand #(10) n3(w3, clk, w4);
    nand #(10) n4(w4, w1, w3);

    SRlatch sr(w3, w2, Q, _Q);
endmodule
```

SRlatch:

```
//sr latch////
`timescale 1 ns/100ps
//SR latch
module SRlatch(S, R, Q, _Q);

    input S,R;
    output Q, _Q;


    nand #(10) g1(Q,_Q, S);
    nand #(10) g2(_Q,R, Q);
endmodule
```

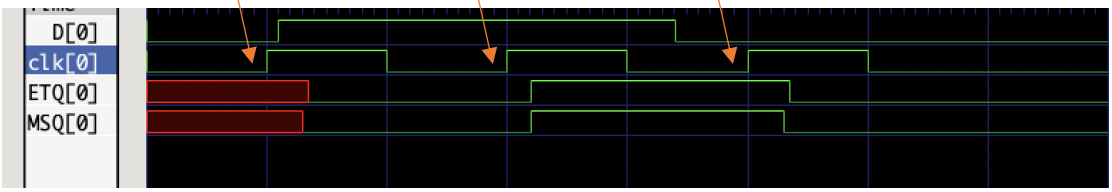
Dlatch:

```
45
46  //D-latch
47  module Dlatch(D, en, Q, _Q);
48      input D, en;
49      output Q, _Q;
50
51      wire _D;
52      not #(5) n1(_D, D);
53      wire w1, w2;
54      nand #(10) g1(w1, en, D);
55      nand #(10) g2(w2, en, _D);
56      SRlatch sr1(w1, w2, Q, _Q);
57  endmodule
58
```

(3) the behavior description (i.e., use always block) of D flip-flop

TRUTH TABLE

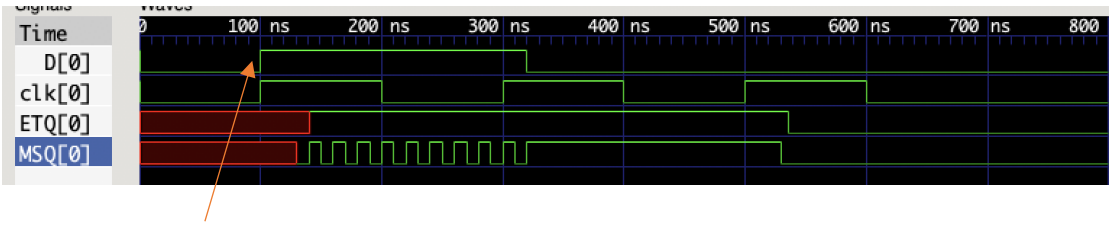
INPUTS				OUTPUTS	
$\overline{PR}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	X	X
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_0	$\overline{Q}_0$



這是 d-flip flop 的真值表，我將 masterslave 範例的 negative-edge trigger 轉成 positive,所以當 clk 從 0 變 1 時，Q 的值會變成D 。

一開始在實作 testbench 時沒把 clock 跟 D 的時間錯開，沒注意到 setup time and hold time ， 根據分析顯示 holdup time 如果小於 11ns 的時候 master-slave 會出現類似 glitch 的電路異常，最後我將 clock 的時間調早一點後解決了這個問題。

而相較起來 edge-trigger 的實作則相當理想



this is the testbench that cause the violation