The Data Format for the HPS Engineering Run 2015

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1 Overview

Description of the FADC?

The SVT DAQ consists of multiple data processing daughter boards (DPMs) with two processing nodes (RCEs) per DPM. Each RCE is accessing data from between two and four hybrids that each carry five APV25 readout ASICs. Each RCE runs a CODA Readout Controller (ROC) to transfer data to the CODA event builder.

2 ECal Data Format

Description of the content of the ECal data.

3 SVT Data Format

The SVT data from each of Readout Controllers (ROCs) is stored in a SVT evio bank of type "bank-of-banks" as described in Tab. 1. During normal data taking there are 14 SVT data banks. The SVT evio bank contains information distributed by the master trigger interface (TI) board and the SVT DAQ itself. These are described in detail in Sec. 3.1 and 3.2, respectively.

3.1 SVT TI Data

Each of the SVT RCEs (one per ROC) obtain TI information from the DTM over the COB. This information is attached to each of the events. The TI data contains the event number and trigger time stamp broadcasted by the master TI. Table 2 and Tab. 3 describes the TI bank header and the TI data, respectively.

Table 1: SVT EVIO bank description.

Content	**Type**	**Description**
TI Data	UINT32 bank	TI information
SVT Data	UINT32 bank	SVT data

Table 2: SVT TI bank header description.

Word	**Desc.**	**32-bits**			
0	Type	Exclusive length			
0	Bits	[31:0]			
1	Type	tag	pad	type	num
1	Bits	"0xe10A" [31:16]	"00" [15:14]	"000001" [13:8]	"roc id" [7:0]

Table 3: SVT TI data.

Word	**Desc.**	**32-bits**		
0	Type	EVENT TYPE		EVENT WORD COUNT
0	Bits	[31:24]	"0x0F" [23:16]	[15:0]
1	Type	EVENT NUMBER LOW 32		
1	Bits	[31:0]		
2	Type	TIME STAMP LOW 32 BITS		
2	Bits	[31:0]		
3	Type	TIME STAMP HIGH 16 BITS		
3	Bits	[31:0]		

3.2 SVT Data

An event from the SVT consists of data from hybrids attached to a single RCE or one ROC. The SVT data is contained in an EVIO bank described in Tab. 4. The data itself consists of a header with an event counter and a type indicator, a number of so-called multisamples, and a tail with information about the number of multisamples and any errors encountered. This is described in Tab. 5. The four 32-bit word long multisample contains the ADC converted data, six 14-bit samples from each ASIC channel for each trigger packed into three 32-bit words as described in Tab. 6. The third 32-bit word contains the channel identification and any errors. In addition to the data, each front end ASIC attached to a ROC has a "header" and "tail" multisample for each trigger. These are identified in the third word "head" and "tail" bits. The header multisample contains information regarding the system synchronization and multiplexing data. The information is packed into six 16-bit words, one for each APV25 sample, and reported in place of the ADC samples in the multisample header. The 16-bit word is described in detail in Tab. 7. The "tail" multisample is not used at the moment and stripped out in firmware.

Table 4: SVT Data bank header description.

Word	**Desc.**	**32-bits**			
0	Type	Exclusive length			
0	Bits	[31:0]			
1	Type	tag	pad	type	num
1	Bits	"3" [31:16]	"00" [15:14]	"000001" [13:8]	"roc id" [7:0]

Table 5: SVT data.

Word	**Desc.**	**32-bits**					
0	Type	type			event counter		
0	Bits	”0x01” [31:24]			[23:0]		
multisamples ... multisamples							
’n’	Type	zero	OverflowError	SyncError	zero	#skipped multisamples	# multisamples
’n’	Bits	[31:28]	[27]	[26]	[25:24]	[23:12]	[11:0]

Table 6: SVT multisample.

Word	**Desc.**	**32-bits**								
0-2	Type	ADC samples				ADC samples				
0	Bits	SAMPLE1[31:16]				SAMPLE0[15:0]				
1	Bits	SAMPLE3[31:16]				SAMPLE2[15:0]				
2	Bits	SAMPLE5[31:16]				SAMPLE4[15:0]				
3	Type	zero	Head	Tail	Err.	Hybrid	APV	Ch.	FEB	RCE
3	Bits	[31]	[30]	[29]	[28]	[27:26]	[25:23]	[22:16]	[15:8]	[7:0]

Table 7: APV25 debug sample.

Desc.	**16-bits**			
Type	ApvId	ApvFrameCount	ApvBufferAddress	ApvReadError
Bits	[15:13]	[12:9]	[8:1]	[0]

Table 8: Error classification.

Error	**Description**	**Where**	**Correlated with**
SyncError	Indicates that APV25 event frames built on this RCE had at least two APV chips with inconsistent APV25 buffer addresses.	SVT tail	multisample header error, ApvFrameCount error.
OverflowError	Buffer overflow in the RCE event builder.	SVT tail	
Multisample header error	Inserted empty APV25 frames to complete an event.	multisample header error bit	SyncError, ApvFrameCount
ApvReadError	If '0', the APV25 reported latency or pipeline overflow.	multisample header	
ApvBufferAddress error	The APV25 buffer addresses are not identical.	APVFrameCount, SyncError	
ApvFrameCount error	The APV25 frame count are inconsistent (should increase by 1).	APVBufferAddressError, SyncError	

3.2.1 Error classification

The SVT data contains information about a number of different errors that may occur in the system. Table. 8 contains a summary of the different errors.

3.3 SVT Configuration and Status Bank

3.4 SVT Calibration

4 Slow Control Data Format

4.1 EPICS and scaler Bank

References

[1] O. Adriani *et al.* [PAMELA Collaboration], Nature **458**, 607 (2009)