# The Data Format for the HPS Engineering Run 2015

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## 1 Overview

Description of the FADC [**?**]?

The SVT DAQ consists of multiple data processing daughter boards (DPMs) with two processing nodes (RCEs) per DPM. Each RCE is accessing data from between two and four hybrids that each carry five APV25 readout ASICs. Each RCE runs a CODA Readout Controller (ROC) to transfer data to the CODA event builder.

## 2 ECal Data Format

The ECal data is recorded in a "bank of banks" format, with one top level bank per real hardware crate. The top level banks are distinguished by the crate id# in table 2.

Table 1: ECal crates descriptions.

| **Name** | **Id** | **ECal** | **Other** |
|---|---|---|---|
| hps1 | 37 | Top FADC | |
| hps2 | 39 | Bottom FADC | LED Pulser & Cosmic PMT FADCs |
| hps11 | 46 | Bottom DISC | RF FADC, SSP |
| hps12 | 58 | TDC, Top DISC | |

Table 2: ECal mother bank description.

| **Content** | **Data Type** | **Tag** | **Number** |
|---|---|---|---|
| "bank" | 0xe | `crate_id` | 0 |

### 2.1 FADC

The calorimeter was readout in the FADC250's Mode-1 for the entire 2015 Engineering Run. This records the full 250 kHz waveform for all channels passing threshold in triggered events. The bank has a tag of 0xe101 to denote FADC250 Mode-1.

The bank format is composite, as recorded in the xml description tag: $(c, i, l, N(C, Ns))$, where $c$ is `char` (1 byte), $i$ is `unsigned int` (2 bytes), $l$ is `long` (4 bytes), $s$ is `short` (1 byte), and $N$ is a CODA `NValue` (4 bytes).

Table 3: ECal Mode-1 bank (tag 0xe101) description in terms of words and bytes.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|
| SLOT | TRIG | | TIME | | | | NCHANNELS | | | |
| 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | ... |
| CHAN | NSAMPLES | | | | ADC1 | ADC2 | ... | | | |
| $i$ | $i+1$ | $i+2$ | $i+3$ | $i+4$ | $i+5$ | $i+6$ | $i+7$ | $i+8$ | $i+9$ | ... |
| CHAN | NSAMPLES | | | | ADC1 | ADC2 | ... | | | |

### 2.2 TDC

## 3 SVT Data Format

The SVT data from each of Readout Controllers (ROCs) is stored in a SVT evio bank of type "bank-of-banks" as described in Tab. **??**. During normal data taking there are 14 SVT data banks. The SVT evio bank contains information distributed by the master trigger interface (TI) board and the SVT DAQ itself. These are described in detail in Sec. **??** and **??**, respectively.

### 3.1 SVT TI Data

Each of the SVT RCEs (one per ROC) obtain TI information from the DTM over the COB. This information is attached to each of the events. The TI data contains the event number and trigger time stamp broadcasted by the master TI. Table **??** and Tab. **??** describes the TI bank header and the TI data, respectively.

### 3.2 SVT Data

An event from the SVT consists of data from hybrids attached to a single RCE or one ROC. The SVT data is contained in an EVIO bank described in Tab. **??**. The data itself consists of a header with an event counter and a type indicator, a number of so-called multisamples, and a tail with information about the number of multisamples and any errors encountered. This is described in Tab. **??**. The four 32-bit word long multisample contains the ADC converted data, six 14-bit samples from each ASIC channel for each trigger packed into three 32-bit

Table 4: SVT EVIO bank description.

| **Content** | **Type** | **Description** |
|---|---|---|
| TI Data | UINT32 bank | TI information |
| SVT Data | UINT32 bank | SVT data |

Table 5: SVT TI bank header description.

| **Word** | **Desc.** | **32-bits** | | | |
|---|---|---|---|---|---|
| 0 | Type | Exclusive length | | | |
| 0 | Bits | [31:0] | | | |
| 1 | Type | tag | pad | type | num |
| 1 | Bits | "0xe10A" [31:16] | "00" [15:14] | "000001" [13:8] | "roc id" [7:0] |

Table 6: SVT TI data.

| **Word** | **Desc.** | **32-bits** | | |
|---|---|---|---|---|
| 0 | Type | EVENT TYPE | | EVENT WORD COUNT |
| 0 | Bits | [31:24] | "0x0F" [23:16] | [15:0] |
| 1 | Type | EVENT NUMBER LOW 32 | | |
| 1 | Bits | [31:0] | | |
| 2 | Type | TIME STAMP LOW 32 BITS | | |
| 2 | Bits | [31:0] | | |
| 3 | Type | TIME STAMP HIGH 16 BITS | | |
| 3 | Bits | [31:0] | | |

Table 7: SVT Data bank header description.

| **Word** | **Desc.** | **32-bits** | | | |
|---|---|---|---|---|---|
| 0 | Type | Exclusive length | | | |
| 0 | Bits | [31:0] | | | |
| 1 | Type | tag | pad | type | num |
| 1 | Bits | "3" [31:16] | "00" [15:14] | "000001" [13:8] | "roc id" [7:0] |

Table 8: SVT data.

| **Word** | **Desc.** | **32-bits** | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | Type | type | | | event counter | | |
| 0 | Bits | "0x01" [31:24] | | | [23:0] | | |
| multisamples<br>...<br>multisamples | | | | | | | |
| 'n' | Type | zero | OverflowError | SyncError | zero | #skipped multisamples | # multisamples |
| 'n' | Bits | [31:28] | [27] | [26] | [25:24] | [23:12] | [11:0] |

Table 9: SVT multisample.

| **Word** | **Desc.** | **32-bits** | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0-2 | Type | ADC samples | | | | ADC samples | | | | |
| 0 | Bits | SAMPLE1[31:16] | | | | SAMPLE0[15:0] | | | | |
| 1 | Bits | SAMPLE3[31:16] | | | | SAMPLE2[15:0] | | | | |
| 2 | Bits | SAMPLE5[31:16] | | | | SAMPLE4[15:0] | | | | |
| 3 | Type | zero | Head | Tail | Err. | Hybrid | APV | Ch. | FEB | RCE |
| 3 | Bits | [31] | [30] | [29] | [28] | [27:26] | [25:23] | [22:16] | [15:8] | [7:0] |

Table 10: APV25 debug sample.

| **Desc.** | **16-bits** | | | |
|---|---|---|---|---|
| **Type** | ApvId | ApvFrameCount | ApvBufferAddress | ApvReadError |
| **Bits** | [15:13] | [12:9] | [8:1] | [0] |

words as described in Tab. **??**. The third 32-bit word contains the channel identification and any errors. In addition to the data, each front end ASIC attached to a ROC has a "header" and "tail" multisample for each trigger. These are identified in the third word "head" and "tail" bits. The header multisample contains information regarding the system synchronization and multiplexing data. The information is packed into six 16-bit words, one for each APV25 sample, and reported in place of the ADC samples in the multisample header. The 16-bit word is described in detail in Tab. **??**. The "tail" multisample is not used at the moment and stripped out in firmware.

#### 3.2.1 Error classification

The SVT data contains information about a number of different errors that may occur in the system. Table. **??** contains a summary of the different errors.

### 3.3 SVT Configuration and Status Bank

### 3.4 SVT Calibration

## 4 RF Signal Data Format

## 5 Slow Control Data Format

### 5.1 EPICS and scaler Bank

## References


[1] O. Adriani *et al.* [PAMELA Collaboration], Nature **458**, 607 (2009)

[2] E.Jastrzembski and H. Dong, https://coda.jlab.org/drupal/content/vme-payload-modules

Table 11: Error classification.

| **Error** | **Description** | **Where** | **Correlated with** |
|---|---|---|---|
| SyncError | Indicates that APV25 event frames built on this RCE had at least two APV chips with inconsistent APV25 buffer addresses. | SVT tail | multisample header error, ApvFrameCount error. |
| OverflowError | Buffer overflow in the RCE event builder. | SVT tail | |
| Multisample header error | Inserted empty APV25 frames to complete an event. | multisample header error bit | SyncError, ApvFrameCount |
| ApvReadError | If '0', the APV25 reported latency or pipeline overflow. | multisample header | |
| ApvBufferAddress error | The APV25 buffer addresses are not identical. | APVFrameCount, SyncError | |
| ApvFrameCount error | The APV25 frame count are inconsistent (should increase by 1). | APVBufferAddressError, SyncError | |