AD181A Datasheet

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AD181A Features

CPU

- Single-core 32-bit CPU
- Maximum speed 160MHz
- Core inside tick timer
- Exception mange unit
- dtap debuger with 4 pc trace, 4 breakpoint, 1 watchpoint

Interrupt

- 64 interrupt sources with 8 levels of programmable priority
- Support external I/O interrupt
- With soft interrupt (virtual interrupt) function, priority can be configured

Memory

- On-chip SRAM
- Built-in flash memory controller

Clocks

- On-chip 16 MHz clock
- On-chip 200KHz lower-temperature-drift clock
- 32.768 KHz crystal oscillator

Audio APA

- Support for driving 4 or 8 ohm speaker
- Mono Class-D Speaker Amplifier
 - 0.5W/8 Ω @4.2V
 - 0.25W/8 Ω @3.0V
 - 0.7W/4 Ω @4.2V
 - 0.35W/4 Ω @3.0V

Peripherals

- One full speed USB(USB1.1) OTG controller
- Four multi-function 16-bit timers support capture and PWM mode

- Three UART Controllers supports DMA and Flow Control
- Two I2C controllers support master and slave modes
- Two SPI host controllers, support DMA
- One QDEC interface
- Support 8-bit parallel 8080 series MCU Interface
- Support segment code LCD screen driver interface
- Support Touch Key of pulse counter
- 15-channel 12-bit general purpose ADC
- Six pairs MCPWM, support dead zone
- A0:35/A4:39 Individually programmable and multiplexed GPIO pins
- Digital peripheral crossbar
- Up to 8 external interrupt / wake-up source (low power available,can be multiplexed to any I/O)
- Watchdog

PMU

- Less than 4uA soft off current
- RTC Alarm Wakeup
- VPWR range : 2.1V to 5.5V
- IOVDD range: 2.1V to 3.6V
- VLCD range : 3.0V to 4.4V

Packages

LQFP48(7mm*7mm)

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65° C to $+150^{\circ}$ C

Applications

- Sound Toy
- Audio player
- Universal Microcontroller



1 Block Diagram

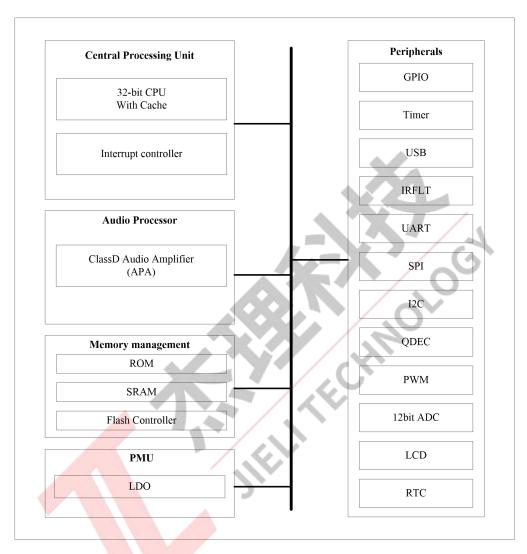


Figure 1-1 AD181A Block Diagram



2 Pin Definition

2.1 Pin Assignment

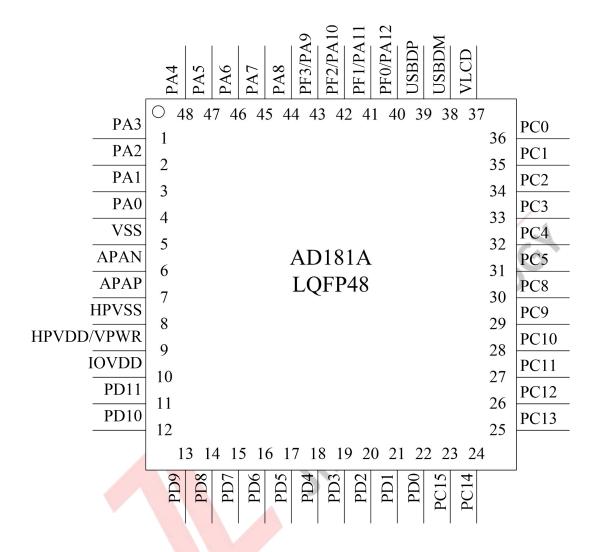


Figure 2-1 AD181A Package Diagram



2.2 Pin Description

Table 2-1 AD181A Pin Description

	Table 2-1 ADIOIA I III Description						
PIN NO.	Name	Туре	Function	Other Function			
1	PA3	I/O	GPIO	ADC3:ADC Input Channel 3;			
2	PA2	I/O	GPIO	ADC2:ADC Input Channel 2;			
3	PA1	I/O	GPIO	ADC1:ADC Input Channel 1;			
4	PA0	I/O	GPIO (pull up)	Long press reset; ADC0:ADC Input Channel 0;			
5	VSS	G		System ground;			
6	APAN	0		Class-D APA Negative Output;			
7	APAP	0		Class-D APA Positive Output;			
8	HPVSS	G		Class-D APA Ground;			
	HPVDD	PI		Class-D APA Power supply;			
9	VPWR	PI		Power supply input;			
10	IOVDD	PO	Power supply for GPIO	Built-in linear voltage regulator output;			
11	PD11	I/O	LCDIO	Timer3_PWM:Timer3 PWM Output; LCD SEG23;			
12	PD10	I/O	LCDIO	Timer2_PWM:Timer2 PWM Output; LCD SEG22;			
13	PD9	I/O	LCDIO	Timer1_PWM:Timer1 PWM Output; LCD SEG21;			
14	PD8	I/O	LCDIO	Timer0_PWM:Timer0 PWM Output; LCD SEG20;			
15	PD7	I/O	LCDIO	PWMCH5L:Motor PWM Channel5(L); LCD SEG19;			
16	PD6	I/O	LCDIO	PWMCH5H:Motor PWM Channel5(H); LCD SEG18;			
17	PD5	I/O	LCDIO	PWMCH4L:Motor PWM Channel4(L); LCD SEG17;			
18	PD4	I/O	LCDIO	PWMCH4H:Motor PWM Channel4(H); LCD SEG16;			
19	PD3	I/O	LCDIO	PWMCH3L:Motor PWM Channel3(L); LCD SEG15;			
20	PD2	I/O	LCDIO	PWMCH3H:Motor PWM Channel3(H); LCD SEG14;			
21	PD1	I/O	LCDIO	LCD_RD:MCU8080_RD; LCD SEG13;			
22	PD0	I/O	LCDIO	LCD_WR:MCU8080_WR; LCD SEG12;			



		_			LCD_D7:MCU8080_D7;			
23	PC1:	5	I/O	LCDIO	LCD SEG11;			
24	PC14 I/O		I/O	LCDIO	LCD_D6:MCU8080_D6;			
	1014		1/ 0	Lebio	LCD SEG10;			
25	PC1	3	I/O	LCDIO	LCD_D5:MCU8080_D5;			
					LCD SEG09;			
26	PC1	2	I/O	LCDIO	LCD_D4:MCU8080_D4;			
					LCD SEG08;			
27	PC1	1	I/O	LCDIO	FPIN0; LCD_D3:MCU8080_D3;			
21	101	1	1/0	LCDIO	LCD SEG07;			
					LCD D2:MCU8080 D2;			
28	PC1	0	I/O	LCDIO	LCD SEG06;			
					LCD D1:MCU8080 D1;			
29	PC9		I/O	LCDIO	LCD SEG05;			
20	D.C.O.		1/0	LCDIO	LCD_D0:MCU8080_D0;			
30	PC8		I/O	LCDIO	LCD SEG04;			
31	DC5		I/O	LCDIO	LCD SEG01;			
31	PC5 I		1/0	LCDIO	LCD COM5;			
32	PC4 I/O		I/O	LCDIO	LCD SEG00;			
	FC4 1/		1.0	Lebio	LCD COM4;			
33	PC3 I/O		I/O	LCDIO	LCD COM3;			
34	PC2		I/O	LCDIO	LCD COM2;			
35	PC1		I/O	LCDIO	LCD COM1;			
36	PC0		I/O	LCDIO	LCD COM0;			
37	VLC	D	P		LCD Voltage;			
38	UDE	BDM	I/O	USB Negative Data (pull down)	ADC14:ADC Input Channel 14;			
39	USB	DP	I/O	USB Positive Data (pull down)	ADC13:ADC Input Channel 13;			
	A0	PF0	I/O	GPIO	SFCCS:SFC Chip Select;			
40	Au	110	1/0	GI IO	SPI0CS:SPI0 Chip Select;			
	A4	PA12	I/O	GPIO	ADC12:ADC Input Channel 12;			
	A0	PF1	I/O	GPIO	SFCDI:SFC Data In;			
41	710	111	1/0	GHO	SPI0DI:SPI0 Data In;			
	A4 PA11		I/O	GPIO	ADC11:ADC Input Channel 11;			
		ATT TATE TO GITO			LVD:Low Voltage Detect;			
	A0 PF2 I/O GPIO		GPIO	SFCCLK:SFC Clk;				
42	2			SPI0CLK:SPI0 Clk;				
	A4	PA10	I/O	GPIO	ADC10:ADC Input Channel 10;			
	A0	PF3	I/O	GPIO	SFCDO:SFC Data Out;			
43	A4	PA9	I/O	GPIO	SPI0DO:SPI0 Data Out; ADC9:ADC Input Channel 9;			
	A4	гАУ	1/0	GFIO	ADC3.ADC IIIput Chaillei 3;			



	44 PA8 I/O GPIO			ADC8:ADC Input Channel 8;		
44			GPIO	OSC32KO:32.768KHz crystal oscillator output;		
				TMR0CK;		
15	DAZ I/O CDIO		CDIO	ADC7:ADC Input Channel 7;		
45	PA7	I/O	GPIO	OSC32KI:32.768KHz crystal oscillator input;		
46	GPIO GPIO		GPIO	MCLR:Low level reset;		
40	PA6	I/O	(pull up)	ADC6:ADC Input Channel 6;		
47	PA5	I/O	GPIO	ADC5:ADC Input Channel 5;		
48	PA4	I/O	GPIO	ADC4:ADC Input Channel 4;		

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PI	Power Input	Ι	Input
PO	Power Output	0	Output
AIO	Analog Input Output	G	Ground

	CROSSBAR									
SPI1	SPI2	IIC0	IIC1	UART0	UART1	UART2				
SPI1_CLK	SPI2_CLK	IIC0_CLK	IIC1_CLK	UART0_TX	UART1_TX	UART2_TX				
SPI1_DI	SPI2_DI	IIC0_DAT	IIC1_DAT	UART0_RX	UART1_RX	UART2_RX				
SPI_D0	SPI2_D0	A leaf				UART2_CTS				
SPI_DAT2						UART2_RTS				
SPI_DAT3	4									

	Input Channel x8			Output C	hannel x8	
WAKEUP0	Timer0	IRFLT	PWMCH0H	Timer0_PWM	CLK_OUT0	LCD_WR
WAKEUP1	Timer1	TOUCH_CAP	PWMCH0L	Timer1_PWM	CLK_OUT1	LCD_RD
WAKEUP2	Timer2	ICH_QDEC0	PWMCH1H	Timer2_PWM	CLK_OUT2	
WAKEUP3	Timer3	ICH_QDEC1	PWMCH1L	Timer3_PWM		
WAKEUP4	CAP0		PWMCH2H			
WAKEUP5	CAP1		PWMCH2L			
WAKEUP6	CAP2					
WAKEUP7	CAP3					



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VPWR	Supply Voltage	-0.3	6	V
HPVDD	APA Power supplyVoltage	-0.3	6	V
VLCD	LCD Voltage	-0.3	4.4	
V _{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
$ m V_{GPIO}$	Voltage applied on normal pin	-0.3	IOVDD+0.3	V
V _{LCDIO}	Voltage applied on special pin	-0.3	VLCD+0.3	V

Note: The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 ESD Protectio

Table 3-2

Parameter	Тур.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	$\pm 200 V$	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2KV	All pins	JEDEC EIA/JESD22-C101F
Lotoh vm	±200mA	All GPIO pins	IEDEC CTANDADD NO 79E
Latch up	1.5xVopmax	All power pins	JEDEC STANDARD NO.78E

Note: $1.5 \times \text{Vopmax} = 1.5 \times \text{times max}$ imum operating voltage.

3.3 PMU Characteristics

Table 3-3

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
VPWR	Voltage Input	2.1	3.7	5.5	V	_
HPVDD	APA Power supplyVoltage	2.1	3.7	5.5	V	-
VLCD	LCD Voltage	3.0	3.6	4.4	V	_
IONDD	Voltage output	2.1	3.0	3.6	V	VPWR = 4.2V, 10mA loading
IOVDD	Loading current	_	_	100	mA	IOVDD= 3.3 V@VPWR ≥ 3.6 V
$V_{ m LVD}$	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection of IOVDD



3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO and LCI	GPIO and LCDIO input characteristics								
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions			
$V_{\rm IL}$	Low-Level Input Voltage	-0.3	-	0.3* IOVDD	V	IOVDD = 3.0V			
V_{IH}	High-Level Input Voltage	0.7* IOVDD	-	IOVDD+0.3	V	IOVDD = 3.0V			
GPIO output c	GPIO output characteristics								
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions			
$ m V_{OL}$	Low-Level Input Voltage	_	-	0.1* IOVDD	V	IOVDD = 3.0V			
$ m V_{OH}$	High-Level Input Voltage	0.9* IOVDD	-		V	IOVDD = 3.0V			
LCDIO output	characteristics					/ 4			
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions			
V_{OL}	Low-Level Input Voltage	_	A-	0.1* VLCD	V	VLCD = 3.8V			
$ m V_{OH}$	High-Level Input Voltage	0.9*VLCD		_	V	VLCD = 3.8V			

3.5 IO Output Drive Strength Pull Up/Down Characteristics

Table 3-5

Port	Drive Strength	Pull Up Resistance	Pull DownResistance	Test Conditions	
PA0-PA12	00: 1.8mA 01: 6mA 10: 20mA 11: 45mA	10K/100K/1M	10K/100K/1M	IOVDD = 3.3V	
PC0-PC5 PC8-PC15 PD0-PD11	8mA	10K/100K/1M	10K/100K/1M	IOVDD = 3.3V	
DP	9mA	1.5K	15K	IOVDD = 3.3V	
DM	9mA	180K	15K	IOVDD = 3.3V	
APAP	APAP 300mA		-	HPVDD = 3.7V	
APAN	300mA	-	-	HPVDD = 3.7V	

Note1: precision of 10K/100K pull-up and pull-down resistor is $\pm 30\%$

Note2: precision of 1M pull-up and pull-down resistor is -50%, +100%

Note3: PA0 and PA6 default pull up, USBDM and USBDP default pull down



3.6 Audio APA Characteristics

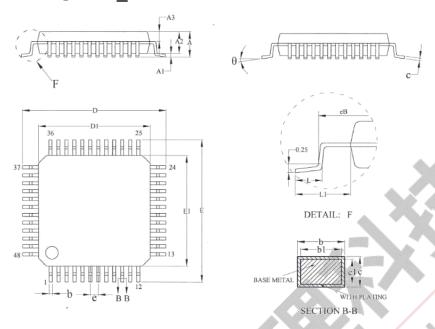
Table 3-6

Parameter	MODE	Min	Тур	Max	Unit	Test (Conditions	
Frequency Response		20	_	20K	Hz	R _L =10K	VPWR=3.7V	
		_	1.5	_	Vrms	$R_L=4\Omega$		
Output Swing	Diff (N to P)	_	1.8	_	Vrms	$R_L=8\Omega$	f=1kHz/0dB	
Output Swing		_	2.2	_	Vrms	R _L =10K	VPWR=3.7V	
	Single-ended	_	1.1	_	Vrms	R _L =10K		
Output power	Diff (N to P)		0.55	_	W	$R_L=4\Omega$	f=1kHz/0dB	
Output power	DIII (N to P)	_	0.40	_	W	$R_L=8\Omega$	VPWR=3.7V	
		_	-39	_ <	dB	$R_L=4\Omega$	f=1kHz/0dB	
THD+N	Diff (N to P)		-43		dB	$R_L=8\Omega$		
I⊓D⊤N		_	-68	1	dB	R _L =10K	A-Weighted VPWR=3.7V	
	Single-ended		-64		dB	R _L =10K	V F W K-3./ V	
		ı	95		dB	$R_L=4\Omega$	f=1kHz/0dB	
S/N	Diff (N to P)	_	95		dB	$R_L=8\Omega$	A-Weighted	
5/1\		_	97	_	dB	R _L =10K	VPWR=3.7V	
	Single-ended	ı	83		dB	R _L =10K	V F W K-3./ V	
		ı	89	-	dB	$R_L=4\Omega$	f=1kHz/-60dB	
Dynamia Panca	Diff (N to P)	p//	89		dB	$R_L=8\Omega$		
Dynamic Range		>_	89		dB	R _L =10K	A-Weighted VPWR=3.7V	
	Single-ended		81	/_	dB	R _L =10K	v r w K-3./V	



4 Package Information

4.1 LQFP48_7×7mm



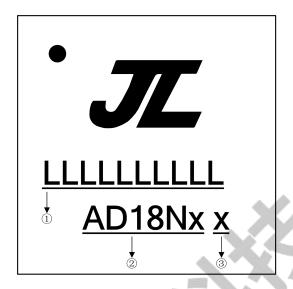
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
Α		_	1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	_	0.26
b1	0.17	0.20	0.23
С	0.13	_	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
Е	8.80	9.00	9.20
El	6.90	7.00	7.10
eB 🧆	8.10	_	8.25
e	0.50BSC		
L	0.40	_	0.65
LI	1.00REF		
θ	0	_	T

Figure 4-1 AD181A Package





5 IC Marking Information



- ① LLLLLLLLL: Production Batch
- ② AD18Nx: Chip Model
- 3 Built-in flash size
 - 0: No Flash Memory
 - 2: 2Mbit Flash
 - 4: 4Mbit Flash
 - 8: 8Mbit Flash
 - 6: 16Mbit Flash
 - 3: 32Mbit Flash



6 Solder-Reflow Condition

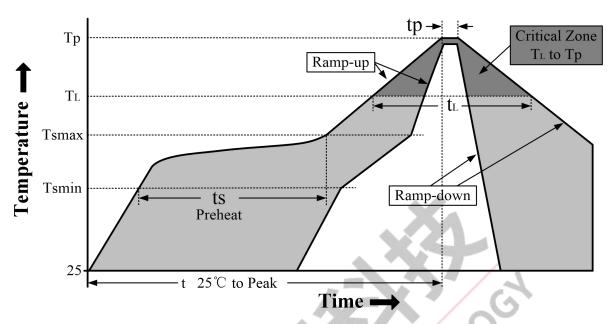


Figure 6-1 Classification Reflow Profile

Classification Profiles

Table 6-1

	Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
	Temperature Min (T _{smin})	100 °C	150 ℃
Preheat/	Temperature Max (T _{smax})	150 ℃	200 ℃
Soak	Time (ts) from (T _{smin} to T _{sma} x)	60-120 seconds	60-180 seconds
Average ra	amp-up rate $(T_{smax} \text{ to } T_p)$	3 °C/second max	3 °C/second max
Liquidous	temperature (T _L)	183 ℃	217 ℃
Time (t _L) maintained above T _L		60-150 seconds	60-150 seconds
Peak package body temperature (T _p) See Table 6-2.		See Table 6-3.	
Time within 5°C of actual Peak Temperature (tp)		10-30 seconds	20-40 seconds
Ramp-down rate (T _p to T _L)		6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5° C of actual peak temperature (tp) specified for the reflow profiles is a "supplier" minimum and "user" maximum.

SnPb - Classification Temperature

Table 6-2

Package	Volume mm ³	Volume mm ³
Thickness	< 350	≥ 350
<2.5 mm	240 +0/-5 ℃	225 +0/-5 °C
≥ 2.5 mm	225 +0/-5 °C	225 +0/-5 °C



<u>Pb-free - Classification Temperature</u> Table 6-3

Package	Volume mm ³	Volume mm ³	Volume mm ³
Thickness	< 350	350 - 2000	> 2000
< 1.6mm	260 ℃	260 ℃	260 °C
1.6 mm - 2.5mm	260 ℃	250 ℃	245 ℃
> 2.5mm	250 °C	245 ℃	245 ℃





7 Revision History

Date	Revision	Description
2023.09.06	V1.0	Initial Release.

