AD177A0 Datasheet

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AD177A0 Features

CPU

- 32bit DSP
- Maximum speed 160MHz
- Interrupts with 8 priority level

Memory

Optional built-in flash memory

Clocks

- On-chip 16 MHz clock
- On-chip 200KHz lower-temperature-drift clock

Audio APA

- Support for driving 4 or 8 ohm speaker
- Mono Class-D Speaker Amplifier
 - 0.42W/8 Ω @3.7V
 - $0.17W/8 \Omega @2.4V$
 - 0.62W/4 Ω @3.7V
 - 0.25W/4 Ω @2.4V

Peripherals

- Three multi-function 16-bit timers, support capture and PWM mode
- Two UART Controllers(UART0/1) supports DMA and Flow Control
- One IIC Master controller
- Two SPI Master / Slaver controller with DMA

SPI0 support 4bit, SPI1 support 2bit

- 16-channel 10-bit general purpose ADC
- 4-channel Advance PWM controller
- 21 Individually programmable and multiplexed GPIO pins
- Digital peripheral crossbar
- Support Touch Key of pulse counter
- Up to 8 external interrupt / wake-up source (low power available,can be multiplexed to any I/O)
- Watchdog

PMU

- Less than 2uA soft off current
- **VBAT** range: 2.0V to 5.5V
- HPVDD range: 2.0V to 5.5V
- IOVDD range: 2.0V to 3.4V

Packages

QSOP28

Temperature

- Operating temperature: -40° C to $+85^{\circ}$ C
- Storage temperature: -65° C to $+150^{\circ}$ C

Applications

- Sound Toy
- Audio player
- Universal Microcontroller



1 Block Diagram

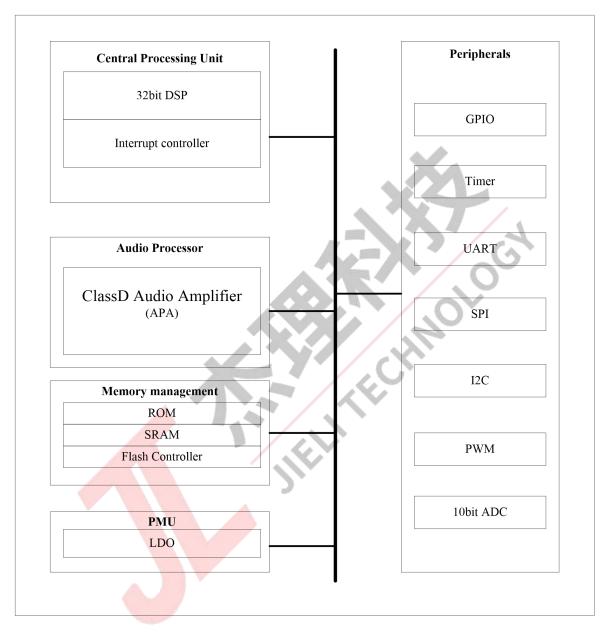


Figure 1-1 AD177A0 Block Diagram



2 Pin Definition

2.1 Pin Assignment

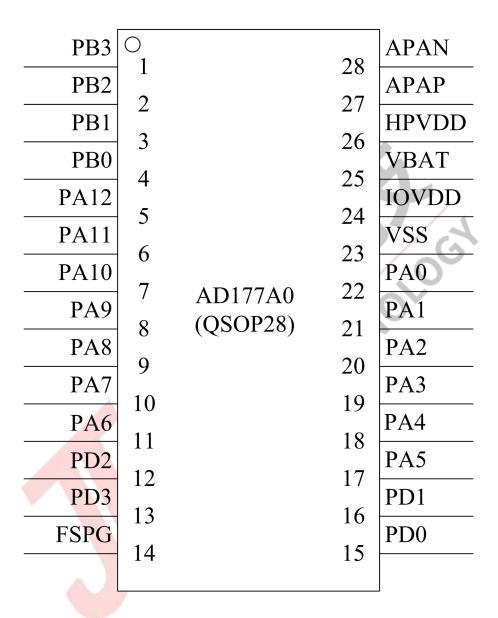


Figure 2-1 AD177A0 Package Diagram



2.2 Pin Description

Table 2-1 AD177A0 Pin Description

PIN Name					At 1 in Description
PB2		Name	Туре	Function	Other Function
PB2	1	PB3	I/O		
A	2	PB2	I/O		MCLR:Low level reset;
5 PA12 I/O GPIO ADC12:ADC Input Channel 12; 6 PA11 I/O GPIO ADC11:ADC Input Channel I1; 7 PA10 I/O GPIO ADC10:ADC Input Channel I0; 8 PA9 I/O GPIO (pull down) ADC9:ADC Input Channel 9; 9 PA8 I/O GPIO (pull down) ADC3:ADC Input Channel 8; 10 PA7 I/O GPIO (pull down) ADC3:ADC Input Channel 7; 11 PA6 I/O GPIO (pull down) ADC3:ADC Input Channel 6; 12 PD2 I/O GPIO (pull down) ADC3:ADC Input Channel 6; 13 PD3 I/O GPIO (pull down) SFCDI:SFC Data In; ADC14:ADC Input Channel 14; SFCDI:SFC Data In; ADC14:ADC Input Channel 15; 15 PD0 I/O GPIO SFCCLK:SFC Clk; 16 PD1 I/O GPIO SFCCLK:SFC Clk; 17 PA5 I/O GPIO ADC4:ADC Input Channel 13; 18 PA4 I/O GPIO ADC4:ADC Input Channel 4; <t< td=""><td>3</td><td>PB1</td><td>I/O</td><td>5V tolerant IO</td><td>Serial port code upgrade pin;</td></t<>	3	PB1	I/O	5V tolerant IO	Serial port code upgrade pin;
6 PA11 I/O GPIO ADC11:ADC Input Channel II; 7 PA10 I/O GPIO ADC10:ADC Input Channel I0; 8 PA9 I/O GPIO (pull down) ADC9:ADC Input Channel 9; 9 PA8 I/O GPIO (pull down) ADC7:ADC Input Channel 8; 10 PA7 I/O GPIO (pull down) ADC7:ADC Input Channel 7; 11 PA6 I/O GPIO (pull down) ADC6:ADC Input Channel 6; 12 PD2 I/O GPIO (pull down) ADC6:ADC Input Channel 6; 13 PD3 I/O GPIO (pull down) SFCD:SFC Chip Select; 14 FSPG O GPIO (pull down) ADC4:ADC Input Channel 14; 15 PD0 I/O GPIO (pull down) SFCD:SFC Data Out; ADC15:ADC Input Channel 15; 15 PD0 I/O GPIO (pull down) SFCD:SFC Data Out; ADC16:ADC Input Channel 13; 16 PD1 I/O GPIO (pull down) ADC3:ADC Input Channel 15; 17 PA5 I/O GPIO (pull down) ADC3:ADC Input	4	PB0	I/O	5V tolerant IO	
7 PA10 I/O GPIO ADC10:ADC Input Channel J0; 8 PA9 I/O GPIO (pull down) (pull down) ADC9:ADC Input Channel 9; (pull down) 9 PA8 I/O GPIO (pull down) ADC8:ADC Input Channel 8; (pull down) 10 PA7 I/O GPIO (pull down) ADC6:ADC Input Channel 7; 11 PA6 I/O GPIO (pull down) ADC6:ADC Input Channel 6; 12 PD2 I/O GPIO (pull down) ADC6:ADC Input Channel 6; 13 PD3 I/O GPIO (pull down) ADC14:ADC Input Channel 14; 14 FSPG O GPIO (pull down) ADC15:ADC Input Channel 14; 15 PD0 I/O GPIO (pull down) SFCD0:SFC Data Out; ADC15:ADC Input Channel 15; SFCD0:SFC Data Out; ADC15:ADC Input Channel 13; ADC3:ADC Input Channel 15; 17 PA5 I/O GPIO ADC4:ADC Input Channel 4; 18 PA4 I/O GPIO ADC4:ADC Input Channel 2; 19 PA2 I/O GPIO ADC4:ADC Input Channel 2; 17MR0:Timer0 Clock Input;	5	PA12	I/O	GPIO	ADC12:ADC Input Channel 12;
8 PA9 I/O GPIO (pull down) (pull down) ADC9:ADC Input Channel 9; 9 PA8 I/O GPIO (pull down) ADC8:ADC Input Channel 8; 10 PA7 I/O GPIO (pull down) ADC6:ADC Input Channel 7; 11 PA6 I/O GPIO (pull down) ADC6:ADC Input Channel 6; 12 PD2 I/O GPIO SFCCS:SFC Chip Select; 13 PD3 I/O GPIO SFCCISEC Data In; ADC14:ADC Input Channel 14; FIsh Power Gate; ADC15:ADC Input Channel 14; 14 FSPG O GPIO SFCCLK:SFC Clk; 15 PD0 I/O GPIO SFCCLK:SFC Clk; 16 PD1 I/O GPIO SFCCLK:SFC Clk; 17 PA5 I/O GPIO ADC5:ADC Input Channel 13; 17 PA5 I/O GPIO ADC4:ADC Input Channel 4; 19 PA3 I/O GPIO ADC3:ADC Input Channel 4; 20 PA2 I/O GPIO ADC2:ADC Input Channel 2; </td <td>6</td> <td>PA11</td> <td>I/O</td> <td>GPIO</td> <td>ADC11:ADC Input Channel 11;</td>	6	PA11	I/O	GPIO	ADC11:ADC Input Channel 11;
PA9	7	PA10	I/O	GPIO	ADC10:ADC Input Channel 10;
PAS	8	PA9	I/O	(pull down)	ADC9:ADC Input Channel 9;
10	9	PA8	I/O	(pull down)	ADC8:ADC Input Channel 8;
11	10	PA7	I/O	(pull down)	ADC7:ADC Input Channel 7;
12	11	PA6	I/O		ADC6:ADC Input Channel 6;
13	12	PD2	I/O		SFCCS:SFC Chip Select;
ADC14:ADC Input Channel 14;	12	DD2	I/O	CNIO	SFCDI:SFC Data In;
14	13	PD3	1/0	GPIO	ADC14:ADC Input Channel 14;
Comparison Com	1.4	ESDC	0		Flash Power Gate;
16	14	rard	U	(pull down)	ADC15:ADC Input Channel 15;
16 PD1 I/O GPIO ADC13:ADC Input Channel 13; 17 PA5 I/O GPIO ADC5:ADC Input Channel 5; PWMCK1; 18 PA4 I/O GPIO ADC4:ADC Input Channel 4; 19 PA3 I/O GPIO CAP0:Timer0 Capture; PWM0:Timer0 PWM Output; 20 PA2 I/O GPIO ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input; 21 PA1 I/O GPIO ADC1:ADC Input Channel 1; LVD:Low Voltage Detect; 22 PA0 I/O GPIO (pull up) Long press reset; ADC0:ADC Input Channel 0; 23 VSS G System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 25 VBAT PI Power supply input; 26 HPVDD PI Class-D APA Power supply;	15	PD0	I/O	GPIO	SFCCLK:SFC Clk;
ADC13:ADC Input Channel 13; ADC5:ADC Input Channel 5; PWMCK1; 18 PA4 I/O GPIO ADC4:ADC Input Channel 4; ADC3:ADC Input Channel 3; CAP0:Timer0 Capture; PWM0:Timer0 PWM Output; ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input; ADC1:ADC Input Channel 1; LVD:Low Voltage Detect; PA0 I/O GPIO Long press reset; ADC0:ADC Input Channel 0; System ground; VSS G System ground; Power supply for GPIO Built-in linear voltage regulator output; Power supply input; Class-D APA Power supply;	16	PD1	I/O	GPIO	SFCDO:SFC Data Out;
17 PA5 I/O GPIO PWMCK1; 18 PA4 I/O GPIO ADC4:ADC Input Channel 4; ADC3:ADC Input Channel 3; CAP0:Timer0 Capture; PWM0:Timer0 PWM Output; ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input; 21 PA1 I/O GPIO ADC1:ADC Input Channel 1; LVD:Low Voltage Detect; 22 PA0 I/O GPIO Long press reset; ADC0:ADC Input Channel 0; System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 26 HPVDD PI Class-D APA Power supply;	10	TDI	1/0	GI IO	ADC13:ADC Input Channel 13;
PWMCK1; 18 PA4 I/O GPIO ADC4:ADC Input Channel 4; ADC3:ADC Input Channel 3; CAP0:Timer0 Capture; PWM0:Timer0 PWM Output; ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input; ADC1:ADC Input Channel 1; LVD:Low Voltage Detect; PA0 I/O GPIO Long press reset; ADC0:ADC Input Channel 0; System ground; VSS G System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 26 HPVDD PI Class-D APA Power supply;	17	ΡΔ5	I/O	GPIO	ADC5:ADC Input Channel 5;
ADC3:ADC Input Channel 3; CAP0:Timer0 Capture; PWM0:Timer0 PWM Output; ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input; ADC1:ADC Input Channel 1; LVD:Low Voltage Detect; PA0 I/O GPIO Long press reset; ADC0:ADC Input Channel 0; System ground; VSS G System ground; VSS G System ground; VSS VBAT PI Power supply for GPIO Built-in linear voltage regulator output; POWER SUPPLY SEARCH STANDARD POWER SUPPLY SEARCH SUP	1 /	TAJ	1/0	GI IO	PWMCK1;
PA3 I/O GPIO CAP0:Timer0 Capture; PWM0:Timer0 PWM Output; ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input; ADC1:ADC Input Channel 1; LVD:Low Voltage Detect; PA0 I/O GPIO Long press reset; ADC0:ADC Input Channel 0; System ground; VSS G System ground; VSS G System ground; VSS VBAT PI Power supply for GPIO Built-in linear voltage regulator output; Power supply input; Class-D APA Power supply;	18	PA4	I/O	GPIO	ADC4:ADC Input Channel 4;
PWM0:Timer0 PWM Output; ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input; PA1 I/O GPIO ADC1:ADC Input Channel 1; LVD:Low Voltage Detect; PA0 I/O GPIO Long press reset; ADC0:ADC Input Channel 0; System ground; VSS G System ground; VSS G System ground; VSS PO Power supply for GPIO Built-in linear voltage regulator output; VSS VBAT PI Power supply input; Class-D APA Power supply;			p d		ADC3:ADC Input Channel 3;
20 PA2 I/O GPIO ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input; 21 PA1 I/O GPIO ADC1:ADC Input Channel 1; LVD:Low Voltage Detect; 22 PA0 I/O GPIO Long press reset; ADC0:ADC Input Channel 0; 23 VSS G System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 25 VBAT PI Power supply input; 26 HPVDD PI Class-D APA Power supply;	19	PA3	I/O	GPIO	CAP0:Timer0 Capture;
20 PA2 I/O GPIO TMR0:Timer0 Clock Input; 21 PA1 I/O GPIO GPIO GPIO Long press reset; ADC0:ADC Input Channel 1; LVD:Low Voltage Detect; Long press reset; ADC0:ADC Input Channel 0; System ground; 23 VSS G System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 25 VBAT PI Power supply input; Class-D APA Power supply;					PWM0:Timer0 PWM Output;
TMR0:Timer0 Clock Input; 21 PA1 I/O GPIO GPIO GPIO Long press reset; ADC0:ADC Input Channel 1; LVD:Low Voltage Detect; Long press reset; ADC0:ADC Input Channel 0; System ground; 23 VSS G System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 25 VBAT PI Power supply input; 26 HPVDD PI Class-D APA Power supply;	20	PA2	I/O	GPIO	ADC2:ADC Input Channel 2;
21 PA1 I/O GPIO LVD:Low Voltage Detect; 22 PA0 I/O GPIO (pull up) Long press reset; ADC0:ADC Input Channel 0; 23 VSS G System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 25 VBAT PI Power supply input; 26 HPVDD PI Class-D APA Power supply;	20	1112	10	GI IO	TMR0:Timer0 Clock Input;
LVD:Low Voltage Detect; 22 PA0 I/O GPIO (pull up) Long press reset; ADC0:ADC Input Channel 0; 23 VSS G System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 25 VBAT PI Power supply input; 26 HPVDD PI Class-D APA Power supply;	21	ΡΔ1	1/0	GPIO	ADC1:ADC Input Channel 1;
22 PA0 I/O (pull up) ADC0:ADC Input Channel 0; 23 VSS G System ground; 24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 25 VBAT PI Power supply input; 26 HPVDD PI Class-D APA Power supply;	۷1	IAI	1/0	GI 10	LVD:Low Voltage Detect;
Power supply for GPIO Built-in linear voltage regulator output; VBAT PI Power supply input; Class-D APA Power supply;	22	PA0	I/O		Long press reset;
24 IOVDD PO Power supply for GPIO Built-in linear voltage regulator output; 25 VBAT PI Power supply input; 26 HPVDD PI Class-D APA Power supply;		1110	1.0	(pull up)	ADC0:ADC Input Channel 0;
25 VBAT PI Power supply input; 26 HPVDD PI Class-D APA Power supply;	23	VSS	G		System ground;
26 HPVDD PI Class-D APA Power supply;	24	IOVDD	PO	Power supply for GPIO	Built-in linear voltage regulator output;
	25	VBAT	PI		Power supply input;
27 ADAD O Class DADA Beriting Outside	26	HPVDD	PI		Class-D APA Power supply;
21 Arar U Class-D Ara Positive Output;	27	APAP	О		Class-D APA Positive Output;
28 APAN O Class-D APA Negative Output;	28	APAN	О		Class-D APA Negative Output;



Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PI	Power Input	I	Input
PO	Power Output	0	Output
AO	Analog Output	G	Ground

	CROSSBAR								
SPI0	SPI1	IIC	UART0	UART1	PWMCH0	PWMCH1			
SPI0_CLK	SPI1_CLK	IIC_CLK	UART0_TX	UART1_TX	PWMCH0L	PWMCH1L			
SPI0_DI	SPI1_DI	IIC_DAT	UART0_RX	UART1_RX	PWMCH0H	PWMCH1H			
SP0_D0	SPI1_D0								
SP0_DAT2									
SP0_DAT3									

	Input Channel x6		Output Channel x8			
WAKEUP	Timer1	IRFLT	PWM1	CLK_OUT0	APA_DOP	
PWMFP0	Timer2	TOUCH_CAP	PWM2	CLK_OUT1	APA_DON	
PWMFP1	CAP1	UART1_CTS	UART1_RTS	CLK_OUT2		
EXT_CLK	CAP2					



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	6	V
HPVDD	APA Power supplyVoltage	-0.3	6	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
$ m V_{HVIO}$	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note: The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 ESD Protectio

Table 3-2

Parameter	Тур.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2KV	All pins	JEDEC EIA/JESD22-C101F
Tatalana A	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
Latch up	1.5xVopmax	All power pins	JEDEC STANDARD NO./8E

Note: 1.5 xVopmax = 1.5 times maximum operating voltage.

3.3 PMU Characteristics

Table 3-3

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
VBAT	Voltage Input	2.0	3.7	5.5	V	_
HPVDD	APA Power supplyVoltage	2.2	3.7	5.5	V	_
IOVDD	Voltage output	2.0	3.0	3.4	V	VBAT = 4.2V, 10mA loading
עשאטו	Loading current	_	-	100	mA	IOVDD=3.3V@VBAT ≥ 3.6V
V_{LVD}	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection of IOVDD



3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics								
GPIO input ch	aracteristics				1	1		
Symbol	Parameter Min		Тур	Max	Unit	Test Conditions		
$ m V_{IL}$	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V		
$ m V_{IH}$	High-Level Input Voltage	0.7* IOVDD	-	IOVDD+0.3	V	IOVDD = 3.0V		
High Voltage R	Resistant IO input chara	ecteristics						
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions		
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V		
$ m V_{IH}$	High-Level Input Voltage	0.7* IOVDD	_	+5V	V	IOVDD = 3.0V		
Resistant IO o	utput characteristics							
Symbol	Paramete	er	GPIO	Тур	Unit	Test Conditions		
$ m V_{OL}$	0.1*IOVDD Driv	e current	PA0~PA12 PD0~PD3	HD=1:-7 HD=2:-22 HD=3:-27	mA	IOVDD = 3.0V		
	0.1*IOVDD Driv	e current	PB0~PB3	-7		IOVDD = 3.0V		
$ m V_{OL}$	0.1*HPVDD Drive current APA IO total current limit of 400mA		APAN APAP	-400	mA	VBAT=3.7V		
$ m V_{OH}$	0.9*IOVDD Driv	PA0~PA12 PD0~PD3	HD=1:7 HD=2:24 HD=3:56	mA	IOVDD = 3.0V			
V OH	_ ~	Y	PB0~PB3	7	IIIA			
	0.9*HPVDD Driv APA IO total current l		APAN APAP	400		VBAT=3.7V		

3.5 Internal Resistor Characteristics

Table 3-5

Port	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA12,PB0~PB3,PD0~PD3	10K	200K	 PA0,PB2 default pull up PA6~PA9,FSPG default pull down Internal pull-up/pull-down resistance accuracy ±20%



3.6 Audio APA Characteristics

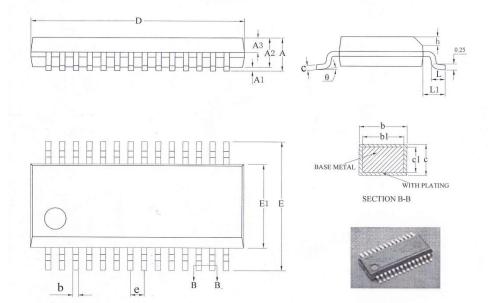
Table 3-6

Payameter MODE Min Typ May Unit Test Conditions								
Parameter	MODE			Test Conditions				
Frequency Response		20	_	20K	Hz	R _L =10K	,VBAT=3.7V	
		_	1.57	_	Vrms	$R_L=4\Omega$		
	Diff (N to P)	_	1.83	_	Vrms	$R_L=8\Omega$	f=1kHz/0dB	
		_	2.22	_	Vrms	R _L =10K	VBAT=3.7V	
Output Swing	Single-ended	_	1.11	_	Vrms	R _L =10K		
o usp us o ming		_	0.99	_	Vrms	$R_L=4\Omega$		
	Diff (N to P)	_	1.17		Vrms	$R_L=8\Omega$	f=1kHz/0dB	
		_	1.44		Vrms	R _L =10K	VBAT=2.4V	
	Single-ended	_	0.72		Vrms	R _L =10K		
		_	0.62		W	$R_L=4\Omega$	f=1kHz/0dB	
Output power	Diff (N to P)	_	0.42	<u></u> 4	W	$R_L=8\Omega$	VBAT=3.7V	
output power		_	0.25		W	$R_L=4\Omega$	f=1kHz/0dB	
		_	0.17	/ /_ \	W	$R_L=8\Omega$	VBAT=2.4V	
		_	-31	-	dB	$R_L=4\Omega$	f=1kHz/0dB	
	Diff (N to P)	_	-35		dB	$R_L=8\Omega$	A-Weighted	
		_	-75	_	dB	R _L =10K	VBAT=3.7V	
THD+N	Single-ended	10-11	-70	/-X	dB	R _L =10K	VBIII 3.7 V	
THE		7-8	-31	V	dB	$R_L=4\Omega$	f=1kHz/0dB A-Weighted	
	Diff (N to P)		-36		dB	$R_L=8\Omega$		
		4	-73	_	dB	R _L =10K	VBAT=2.4V	
	Single-ended	_	-70	_	dB	R _L =10K	VBM1 2.4V	
	Diff (N to P)	_	97	_	dB	$R_L=4\Omega$	f=1kHz/0dB	
		_	97	_	dB	$R_L=8\Omega$	A-Weighted	
			95	_	dB	R _L =10K	VBAT=3.7V	
S/N	Single-ended		75	_	dB	R _L =10K	VBM1 3.7V	
5/14		_	94	_	dB	$R_L=4\Omega$	f=1kHz/0dB	
	Diff (N to P)		94	_	dB	$R_L=8\Omega$	A-Weighted	
	A	_	88	_	dB	R _L =10K	VBAT=2.4V	
	Single-ended	_	72	_	dB	R _L =10K	V DA1-2.4 V	
Dynamic Range		_	88	_	dB	$R_L=4\Omega$	—————————————————————————————————————	
	Diff (N to P)	_	88	_	dB	$R_L=8\Omega$	f=1kHz/-60dB A-Weighted	
		_	86	_	dB	R _L =10K	VBAT=3.7V	
	Single-ended	_	75		dB	R _L =10K	V DA1-3./V	
		_	87	_	dB	$R_L=4\Omega$	£11.11. / 60 1B	
	Diff (N to P)	_	87	_	dB	$R_L=8\Omega$	f=1kHz/-60dB	
		_	85	_	dB	R _L =10K	A-Weighted	
	Single-ended	_	74	_	dB	R _L =10K	VBAT=2.4V	



4 Package Information

4.1 QSOP28



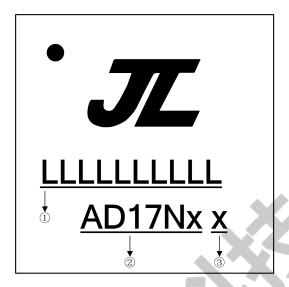
SYMBOL	MILLIMETER							
SIMBOL	MIN	NOM	MAX					
Α	_	_	1.75					
A1	0.05	_	0.225					
A2	1.30	1.40	1.50					
A3	0.60	0.65	0.70					
b	0.23	-	0.31					
b1	0.22	0.25	0.28					
С	0.20	_	0.24					
c1	0.19	0.20	0.21					
D	9.80	9.90	10.00					
Е	5.80	6.00	6.20					
E1	3.80	3.90	4.00					
e	0.635BSC							
h	0.25	-	0.50					
L	0.50	-	0.80					
L1	1.05BSC							
θ	0°		8°					

Figure 4-1 AD177A0 Package





5 IC Marking Information



- 1 LLLLLLLLL: Production Batch
- ② AD17Nx: Chip Model
- 3 Built-in flash size
 - 0: No Flash Memory
 - 2: 2Mbit Flash
 - 4: 4Mbit Flash
 - 8: 8Mbit Flash
 - 6: 16Mbit Flash
 - 3: 32Mbit Flash



6 Solder-Reflow Condition

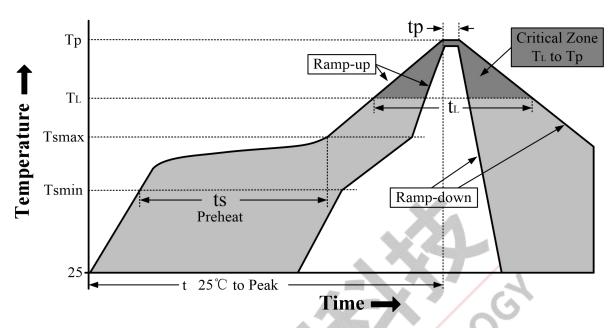


Figure 6-1 Classification Reflow Profile

Classification Profiles

Table 6-1

	Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
	Temperature Min (T _{smin})	100 °C	150 ℃
Preheat/	Temperature Max (T _{smax})	150 ℃	200 ℃
Soak	Time (ts) from (T _{smin} to T _{sma} x)	60-120 seconds	60-180 seconds
Average ra	amp-up rate (T _{smax} to T _p)	3 °C/second max	3 °C/second max
Liquidous	temperature (T _L)	183 ℃	217 ℃
Time (t _L) 1	naintained above T _L	60-150 seconds	60-150 seconds
Peak pack	age body temperature (T _p)	See Table 6-2.	See Table 6-3.
Time within 5°C of actual Peak Temperature (tp)		10-30 seconds	20-40 seconds
Ramp-down rate (T _p to T _L)		6 °C/second max.	6 °C/second max.
Time 25	C to peak temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5° C of actual peak temperature (tp) specified for the reflow profiles is a "supplier" minimum and "user" maximum.

SnPb - Classification Temperature

Table 6-2

Package	Volume mm ³	Volume mm ³
Thickness	< 350	≥ 350
<2.5 mm	240 +0/-5 ℃	225 +0/-5 °C
≥ 2.5 mm	225 +0/-5 °C	225 +0/-5 °C



Pb-free - Classification Temperature Table 6-3

Package Thickness	Volume mm ³ < 350	Volume mm ³ 350 - 2000	Volume mm ³ > 2000
< 1.6mm	260 ℃	260 ℃	260 ℃
1.6 mm - 2.5mm	260 ℃	250 ℃	245 °C
> 2.5mm	250 °C	245 °C	245 ℃





7 Revision History

Date	Revision	Description
2023.07.13	V1.0	Initial Release.
2023.09.28	V1.1	Update Pin Definition. Update Features modification.

