AD177A0 Datasheet

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Version：1.0

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AD177A0 Features

CPU

- 32bit DSP
- Maximum speed 160MHz
- Interrupts with 8 priority level

Memory

- Optional built-in flash memory

Clocks

- On-chip 16 MHz clock
- On-chip 200KHz lower-temperature-drift clock

Audio APA

- Support for driving 4 or 8 ohm speaker
- Mono Class-D Speaker Amplifier
  - 0.42W/8Ω@3.7V
  - 0.17W/8Ω@2.4V
  - 0.62W/4Ω@3.7V
  - 0.25W/4Ω@2.4V

Peripherals

- Three multi-function 16-bit timers, support capture and PWM mode
- Two UART Controllers(UART0/1) supports DMA and Flow Control
- One IIC Master controller
- Two SPI Master / Slaver controller with DMA SPI0 support 4bit,SPI1support 2bit
- 16-channel 10-bit general purpose ADC
- 4-channel Advance PWM controller
- 21 Individually programmable and multiplexed GPIO pins
- Digital peripheral crossbar
- Up to 12 external interrupt / wake-up source (low power available,can be multiplexed to any I/O)
- Watchdog

PMU

- Less than 2uA soft off current
- VBAT range : 2.0V to 5.5V
- HPVDD range : 2.0V to 5.5V
- IOVDD range : 2.0V to 3.4V

Packages

- QSOP28

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Sound Toy
- Audio player
- Universal Microcontroller

1 Block Diagram

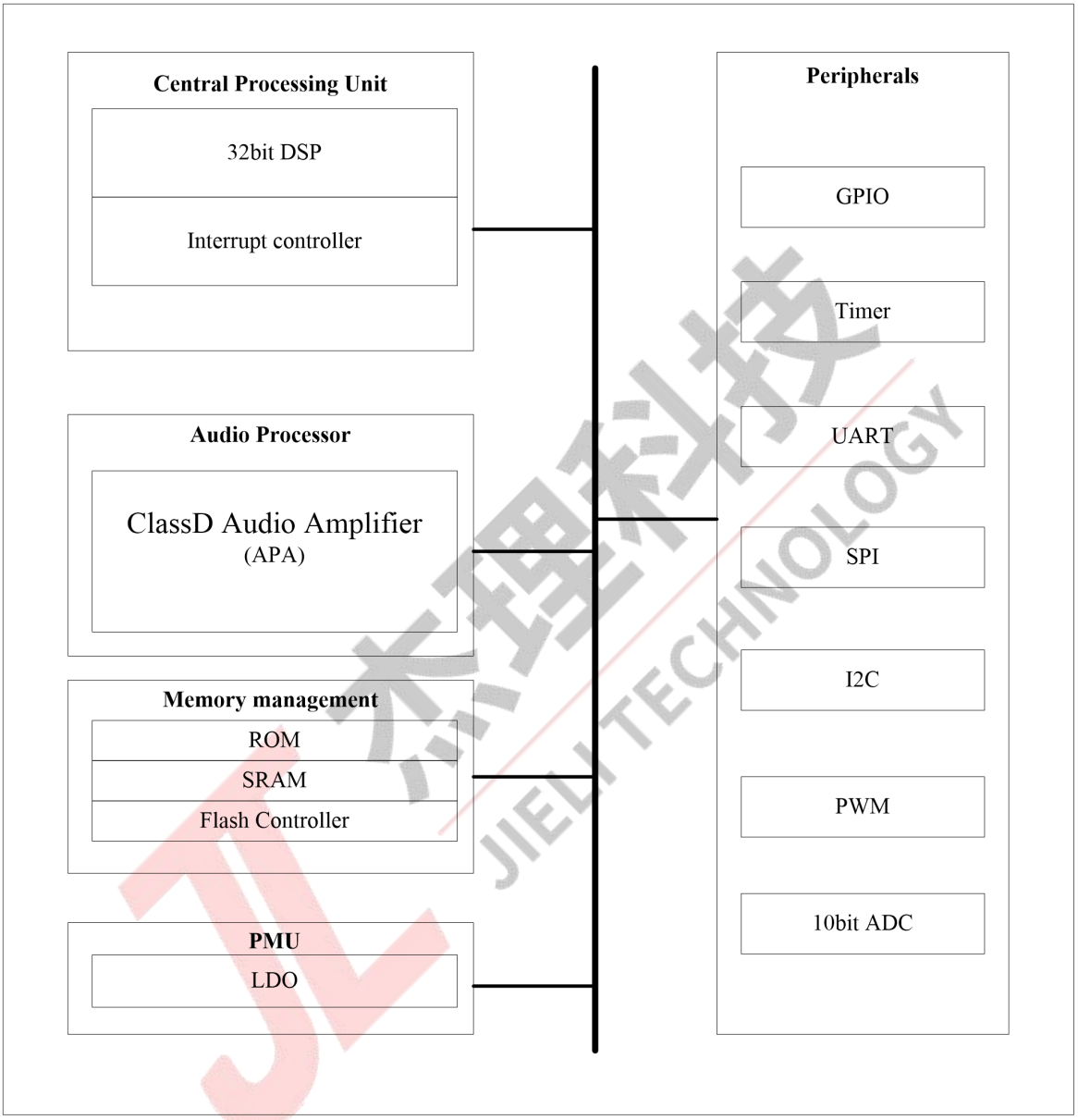


Figure 1-1 AD177A0 Block Diagram

2 Pin Definition

2.1 Pin Assignment

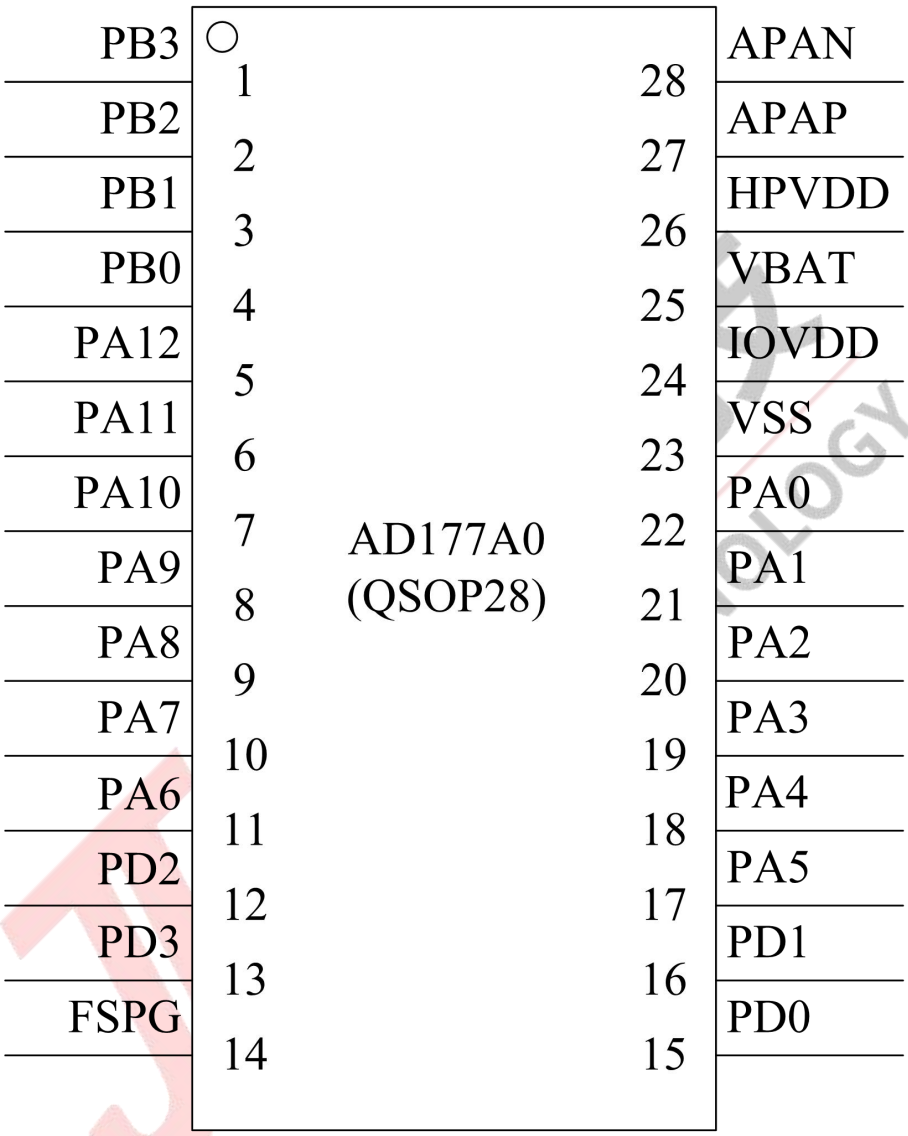


Figure 2-1 AD177A0 Package Diagram

2.2 Pin Description

Table 2-1 AD177A0 Pin Description

PIN NO.	Name	Type	Function	Other Function
1	PB3	I/O	5V tolerant IO	
2	PB2	I/O	5V tolerant IO (pull up)	MCLR:Low level reset; APA_DON;
3	PB1	I/O	5V tolerant IO	Serial port code upgrade pin; APA_DOP;
4	PB0	I/O	5V tolerant IO	
5	PA12	I/O	GPIO	ADC12:ADC Input Channel 12; PWMFP1;
6	PA11	I/O	GPIO	ADC11:ADC Input Channel 11; PWMFP0;
7	PA10	I/O	GPIO	ADC10:ADC Input Channel 10;
8	PA9	I/O	GPIO (pull down)	ADC9:ADC Input Channel 9; Touch cap; CLK OUT2:Internal clock output2;
9	PA8	I/O	GPIO (pull down)	ADC8:ADC Input Channel 8; SPI1DI:SPI1 Data In; WKUP; CLK OUT1:Internal clock output1;
10	PA7	I/O	GPIO (pull down)	ADC7:ADC Input Channel 7; SPI1DO:SPI1 Data Out; UART1RX:Uart1 Data Input; EXTCLK:External clock source; CLKOUT0:Internal clock output0;
11	PA6	I/O	GPIO (pull down)	ADC6:ADC Input Channel 6; SPI1CLK:SPI1 Clk; UART1TX:Uart1 Data Output;
12	PD2	I/O	GPIO	SFCCS:SFC Chip Select;
13	PD3	I/O	GPIO	SFCDI:SFC Data In; ADC14:ADC Input Channel 14;
14	FSPG	O	(pull down)	Flash Power Gate; ADC15:ADC Input Channel 15;
15	PD0	I/O	GPIO	SFCCLK:SFC Clk;
16	PD1	I/O	GPIO	SFCDO:SFC Data Out; ADC13:ADC Input Channel 13;
17	PA5	I/O	GPIO	ADC5:ADC Input Channel 5; PWMCK1; UART1 CTS:Uart1 clear to send; UART1 RTS:Uart1 request to send;

18	PA4	I/O	GPIO	ADC4:ADC Input Channel 4; PWMCK0; SPI0D3:SPI0 Data 3; UART0RX:Uart0 Data Input; PWMCH1H:Motor PWM Channel1(H);
19	PA3	I/O	GPIO	ADC3:ADC Input Channel 3; SPI0D2:SPI0 Data 2; UART0TX:Uart0 Data Output; PWMCH1L:Motor PWM Channel1(L); CAP0:Timer0 Capture; CAP2:Timer2 Capture; PWM0:Timer0 PWM Output;
20	PA2	I/O	GPIO	ADC2:ADC Input Channel 2; SPI0DI(1):SPI1 Data In(1); TMR0:Timer0 Clock Input; TMR2:Timer2 Clock Input; PWM2:Timer2 PWM Output;
21	PA1	I/O	GPIO	ADC1:ADC Input Channel 1; SPI0DO(0):SPI0 Data Out(0); I2C SDA; PWMCH0H:Motor PWM Channel0(H); CAP1:Timer1 Capture; LVD:Low Voltage Detect；
22	PA0	I/O	GPIO (pull up)	Long press reset; ADC0:ADC Input Channel 0; SPI0CLK:SPI0 Clk; I2C SCL; TMR1:Timer1 Clock Input; PWM1:Timer1 PWM Output; PWMCH0L:Motor PWM Channel0(L);
23	VSS	G		System ground;
24	IOVDD	PO	Power supply for GPIO	Built-in linear voltage regulator output;
25	VBAT	PI		Power supply input;
26	HPVDD	PI		Class-D APA Power supply;
27	APAP	O		Class-D APA Positive Output;
28	APAN	O		Class-D APA Negative Output;

Pin Type	**Description**	**Pin Type**	**Description**
P	Power	I/O	Input or Output
PI	Power Input	I	Input
PO	Power Output	O	Output
AO	Analog Output	G	Ground

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	6	V
HPVDD	APA Power supplyVoltage	-0.3	6	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V_{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.0	3.7	5.5	V	_
HPVDD	APA Power supplyVoltage	2.2	3.7	5.5	V	_
IOVDD	Voltage output	2.0	3.0	3.4	V	VBAT = 4.2V, 10mA loading
	Loading current	_	_	100	mA	IOVDD=3.3V@VBAT ≥ 3.6V
V_{LVD}	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection of IOVDD

3.3 IO Input/Output Electrical Logical Characteristics

Table 3-3

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	+5V	V	IOVDD = 3.0V
Resistant IO output characteristics						
Symbol	**Parameter**	**GPIO**	**Typ**		**Unit**	**Test Conditions**
V_{OL}	0.1*IOVDD Drive current	PA0~PA12 PD0~PD3	HD=1 : -7 HD=2 : -22 HD=3 : -27		mA	IOVDD = 3.0V

V_{OL}	0.1*IOVDD Drive current	PB0~PB3	-7	mA	IOVDD = 3.0V
	0.1*HPVDD Drive current APA IO total current limit of 400mA	APAN APAP	-400		VBAT=3.7V
V_{OH}	0.9*IOVDD Drive current	PA0~PA12 PD0~PD3	HD=1 :7 HD=2 : 24 HD=3 : 56	mA	IOVDD = 3.0V
		PB0~PB3	7		
	0.9*HPVDD Drive current APA IO total current limit of 400mA	APAN APAP	400		VBAT=3.7V

3.4 Internal Resistor Characteristics

Table 3-4

Port	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA12,PB0~PB3,PD0~PD3	10K	200K	1. PA0,PB2 default pull up 2. PA6~PA9,FSPG default pull down 3. Internal pull-up/pull-down resistance | accuracy ±20%

3.5 Audio APA Characteristics

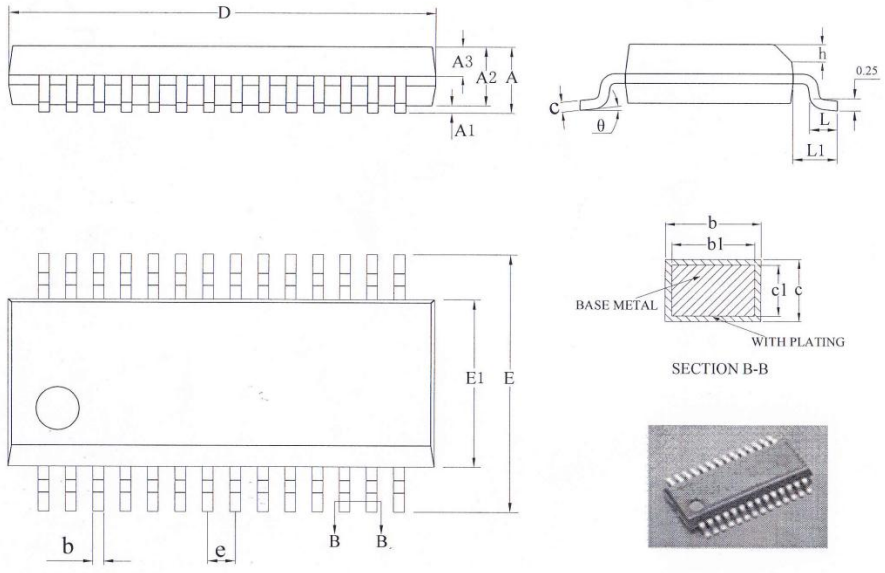
Table 3-5

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions	
Frequency Response		20	_	20K	Hz	R_L=10K,VBAT=3.7V	
Output Swing	Diff (N to P)	_	1.57	_	Vrms	R_L=4Ω	f=1kHz/0dB VBAT=3.7V
		_	1.83	_	Vrms	R_L=8Ω	
		_	2.22	_	Vrms	R_L=10K	
	Single-ended	_	1.11	_	Vrms	R_L=10K	
	Diff (N to P)	_	0.99	_	Vrms	R_L=4Ω	f=1kHz/0dB VBAT=2.4V
		_	1.17	_	Vrms	R_L=8Ω	
		_	1.44	_	Vrms	R_L=10K	
	Single-ended	_	0.72	_	Vrms	R_L=10K	
Output power	Diff (N to P)	_	0.62	_	W	R_L=4Ω	f=1kHz/0dB VBAT=3.7V
		_	0.42	_	W	R_L=8Ω	
		_	0.25	_	W	R_L=4Ω	f=1kHz/0dB VBAT=2.4V
		_	0.17	_	W	R_L=8Ω	
THD+N	Diff (N to P)	_	-31	_	dB	R_L=4Ω	f=1kHz/0dB A-Weighted VBAT=3.7V
		_	-35	_	dB	R_L=8Ω	
		_	-75	_	dB	R_L=10K	
	Single-ended	_	-70	_	dB	R_L=10K	
	Diff (N to P)	_	-31	_	dB	R_L=4Ω	f=1kHz/0dB A-Weighted VBAT=2.4V
		_	-36	_	dB	R_L=8Ω	
		_	-73	_	dB	R_L=10K	
	Single-ended	_	-70	_	dB	R_L=10K	

S/N	Diff (N to P)	_	97	_	dB	R_L=4Ω	f=1kHz/0dB A-Weighted VBAT=3.7V
		_	97	_	dB	R_L=8Ω	
		_	95	_	dB	R_L=10K	
	Single-ended	_	75	_	dB	R_L=10K	
	Diff (N to P)	_	94	_	dB	R_L=4Ω	f=1kHz/0dB A-Weighted VBAT=2.4V
		_	94	_	dB	R_L=8Ω	
		_	88	_	dB	R_L=10K	
	Single-ended	_	72	_	dB	R_L=10K	
Dynamic Range	Diff (N to P)	_	88	_	dB	R_L=4Ω	f=1kHz/-60dB A-Weighted VBAT=3.7V
		_	88	_	dB	R_L=8Ω	
		_	86	_	dB	R_L=10K	
	Single-ended	_	75	_	dB	R_L=10K	
	Diff (N to P)	_	87	_	dB	R_L=4Ω	f=1kHz/-60dB A-Weighted VBAT=2.4V
		_	87	_	dB	R_L=8Ω	
		_	85	_	dB	R_L=10K	
	Single-ended	_	74	_	dB	R_L=10K	

4 Package Information

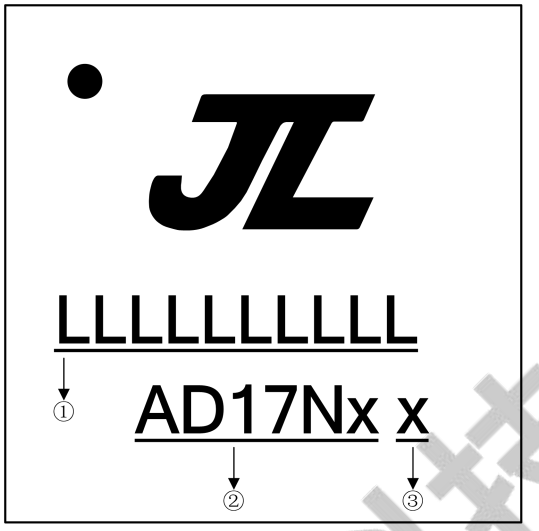
4.1 QSOP28



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0°	—	8°

Figure 4-1 AD177A0 Package

5 IC Marking Information



① LLLLLLLLLL：Production Batch
② AD17Nx：Chip Model
③ Built-in flash size
0: No Flash Memory
2: 2Mbit Flash
4: 4Mbit Flash
8: 8Mbit Flash
6: 16Mbit Flash
3: 32Mbit Flash

6 Solder-Reflow Condition

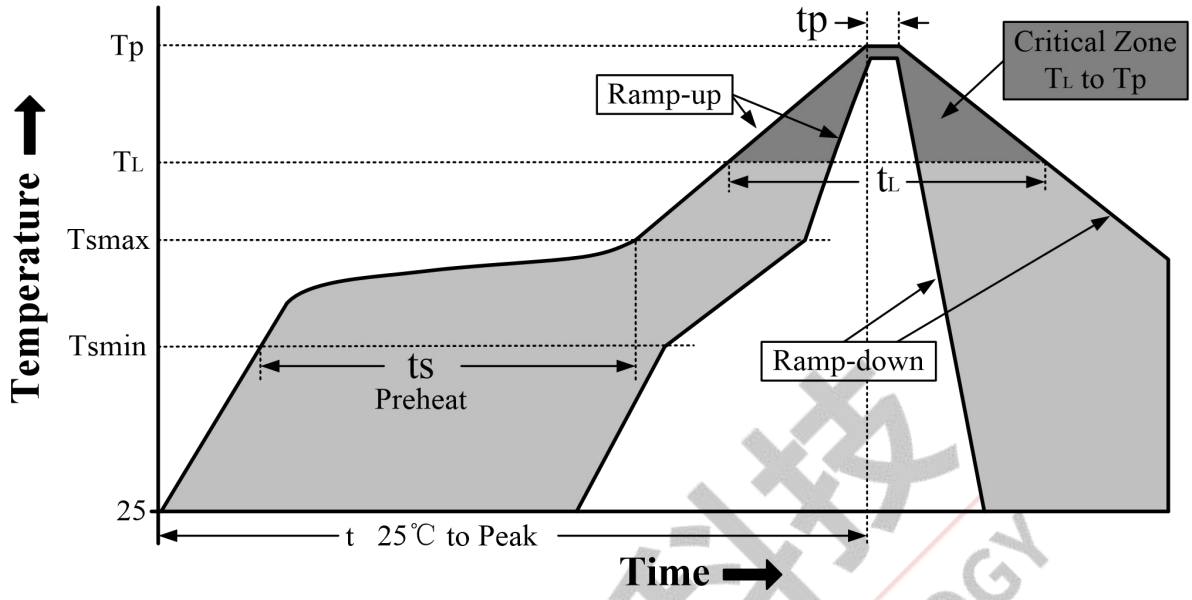


Figure 6-1 Classification Reflow Profile

Classification Profiles **Table 6-1**

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100 ℃	150 ℃
	Temperature Max (T_{smax})	150 ℃	200 ℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3 ℃/second max	3 ℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183 ℃ 60-150 seconds	217 ℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2.	See Table 6-3.
Time within 5°C of actual Peak Temperature (tp)		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6 ℃/second max.	6 ℃/second max.
Time 25 ℃ to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature **Table 6-2**

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5 ℃	225 +0/-5 ℃
≥ 2.5 mm	225 +0/-5 ℃	225 +0/-5 ℃

Pb-free - Classification Temperature **Table 6-3**

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260 ℃	260 ℃	260 ℃
1.6 mm - 2.5mm	260 ℃	250 ℃	245 ℃
> 2.5mm	250 ℃	245 ℃	245 ℃

7 Revision History

Date	Revision	Description
2023.07.13	V1.0	Initial Release.