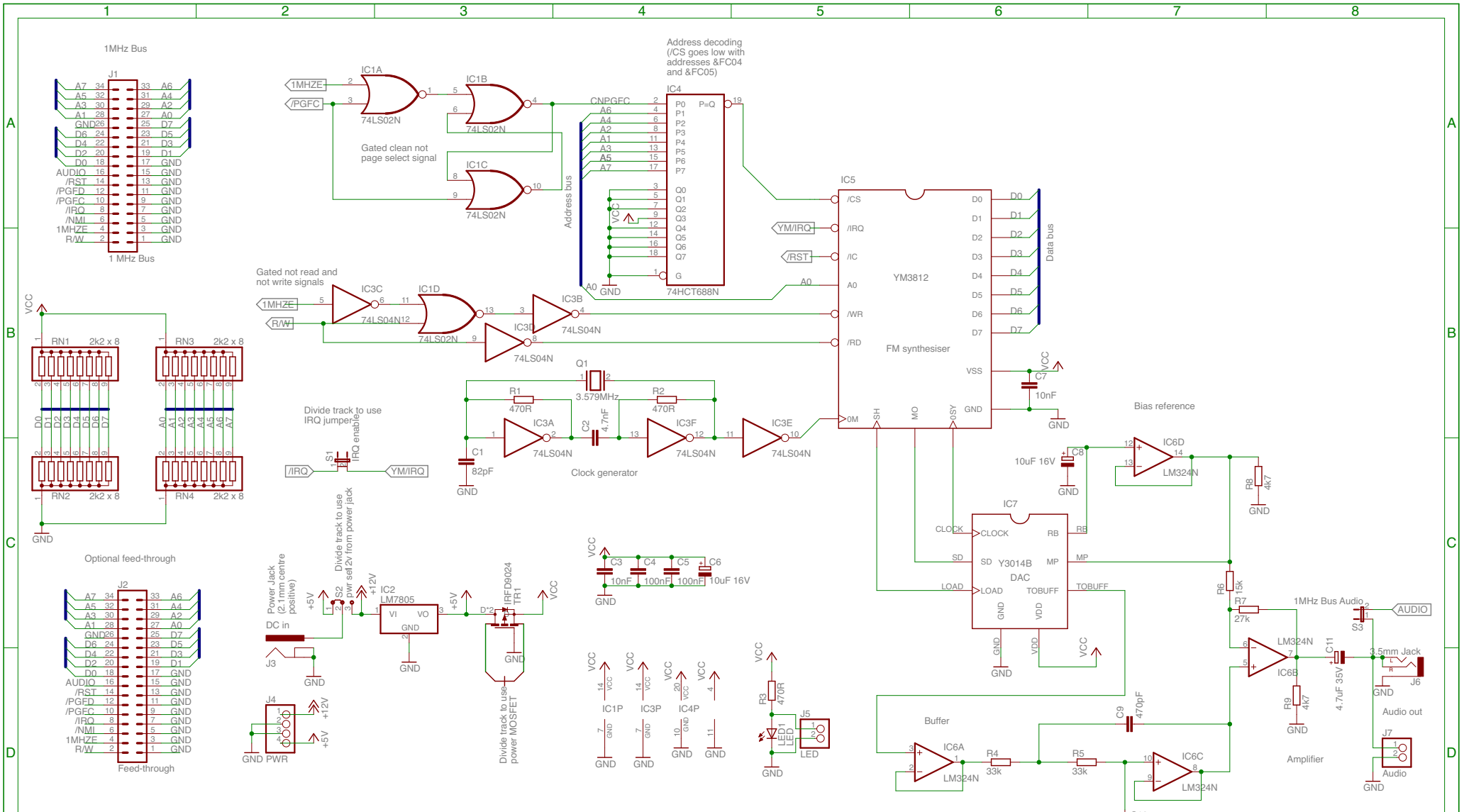
1MHz Bus
J1
1 MHz Bus
IC1A
74LS02N
IC1B
74LS02N
IC1C
74LS02N
Gated clean not page select signal
Address decoding (/CS goes low with addresses &FC04 and &FC05)
IC4
74HCT688N
Address bus
Gated not read and not write signals
IC3C
74LS04N
IC1D
74LS02N
IC3D
74LS04N
IC3B
74LS04N
IC5
YM3812
FM synthesiser
Data bus
Q1
3.579MHz
R1
470R
R2
470R
IC3A
74LS04N
IC3F
74LS04N
IC3E
74LS04N
C1
82pF
C2
4.7nF
Clock generator
Divide track to use IRQ jumper
IRQ enable
S1
RN1
2k2 x 8
RN2
2k2 x 8
RN3
2k2 x 8
RN4
2k2 x 8
Optional feed-through
J2
Feed-through
Power Jack (2.1mm centre positive)
DC in
J3
Divide track to use pwr set 2v from power jack
S2
IC2
LM7805
IRFD9024
TR1
Divide track to use power MOSFET
J4
GND PWR
C3
10nF
C4
100nF
C5
100nF
C6
10uF 16V
IC1P
IC3P
IC4P
R3
470R
LED1
J5
LED
Bias reference
IC6D
LM324N
C8
10uF 16V
R8
4k7
IC7
Y3014B
DAC
R6
15k
R7
27k
1MHz Bus Audio
S3
AUDIO
IC6B
LM324N
C11
4.7uF 35V
3.5mm Jack
J6
R9
4k7
Amplifier
Audio out
J7
Audio
Buffer
IC6A
LM324N
R4
33k
R5
33k
C9
470pF
IC6C
LM324N
C10
220pF
15 kHz low-pass filter
TITLE: BeebOPL
REVISION: 1.00
DATE: 2 October 2016
open hardware
Robert Lazarus
https://github.com/lazarusr/beebopl