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Combinational Circuits (2)

1. Using four half adders, design a combinational circuit that adds one to a 4-bit binary number (an incrementer).

2. Using one half-adder and three full adders, design a combinational circuit that subtract one from a 4-bit binary number (a decrementer).

3. Using three half adders and one full adder, design a combinational circuit that adds three to a 4-bit binary number.

4. Using the minimum number of half adders and full adders to add 5 to a 4-bit binary number.

5. Using AND gates and half adders, design a combinational circuit that multiply two-bit binary numbers.

6. Using two 4-bit adders and one half adder to add three 4-bit numbers.

7. Using two 4-bit adders and any simple gates (OR- AND- NOT) you may need, design a circuit that add two BCD numbers.

8. Using only a 4-bit adder; construct a BCD to excess-3 converter.

9. Use only two 4-bit adders and an inverter, design a circuit that add two numbers represented in a special code, known that the correction after adding the two digits with a 4-bit binary adder is as follows:
   The output carry is equal to the carry from the binary adder.
   If the output carry = 1, then add 0011.
   If the output carry = 0, then add 1101.

10. Using only two 4-bit adders and an inverter, design a circuit that add two 4-bit binary numbers, then do the following:
    If the result is between 0 and 15 included add 5.
    If the result is between 16 and 31 included subtract 5.

11. Using two 4-bit adders and any simple gates (OR- AND- NOT) you may need, design a circuit that add two 4-bit binary numbers, then do the following:
    If the result is between 10 and 15 included add 2.
    If the result is between 16 and 19 included add 4.
    If the result is between 20 and 25 included add 6.
    Otherwise, leave the result as it is.

12. Using simple gates (NOT, AND, OR) to design a combinational circuit with three inputs A, B and C, if the binary input is ≤3, the output binary value is one greater than the input,

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otherwise the output binary value is one less than the input. Then design the same circuit using a full adder and an inverter.

13. Using one 4-bit adder and one half adder to design a circuit that implements the following function Y=25X, where X is 4-bit binary number.

14. Using only one 4-bit adder to design a circuit to that implements the following function: Y=20X+107, where X is 3-bit binary number.

15. Design each of the following functions F using
    i. A decoder and an OR *(First decide the optimal size of the chip needed).*
    ii. A decoder and a NOR *(First decide the optimal size of the chip needed).*
    iii. A multiplexer *(First decide the optimal size of the chip needed).*
        a. $F(A,B) = \overline{A}B + AB$
        b. $F(A,B,C) = \sum_m (0,1,7)$
        c. $F(A,B,C) = \sum_m (2,6,4)$
        d. $F(X,Y,Z) = \sum_m (0,1,3,5,6)$
        e. $F(A,B,C) = \prod_M (3,6,7)$
        f. $F(A,B,C) = \overline{A} + (BC + \overline{C})(ABC + \overline{B})$
        g. $F(A,B,C) = \overline{A}\,\overline{B} + \overline{A}B\overline{C}$
        h. $F(X,Y,Z) = (\overline{X} + \overline{Y} + Z)(\overline{X} + Y + Z)$
        i. $F(X,Y,Z) = X + Y(X + Z)(\overline{X} + \overline{Z})$
        j. $F(A,B,C,D) = \sum_m (0,1,2,5,6)$
        k. $F(A,B,C,D) = \sum_m (0,1,2,3,4,6,8,9,10,11)$
        l. $F(A,B,C,D) = \sum_m (0,5,8,9,11,12,13,14)$
        m. $F(W,X,Y,Z) = \sum_m (0,1,4,5,10,12,14)$
        n. $F(W,X,Y,Z) = \prod_M (0,2,5,6,9,11,12,15)$
        o. $F(W,X,Y,Z) = \prod_M (3,5,7,11,13,15)$
        p. $F(A,B,C,D) = AB\overline{C} + \overline{B}C\overline{D} + BCD + AC\overline{D} + \overline{A}\,\overline{B}C + \overline{A}B\overline{C}D$
        q. $F(A,B,C,D) = B\overline{C} + \overline{A}B + BC\overline{D} + \overline{A}\,\overline{B}D + A\overline{B}\,\overline{C}D$
        r. $F(A,B,C,D) = \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + CD + \overline{A}\,\overline{D}$
        s. $F(W,X,Y,Z) = (W + X + \overline{Y} + \overline{Z})(\overline{X} + \overline{Y} + Z)(\overline{W} + Y + \overline{Z})$
        t. $F(V,W,X,Y,Z) = \overline{V}WX + W\overline{X}\,\overline{Y} + WZ + \overline{X}\,\overline{Z}$
        u. $F(A,B,C,D,E) = \overline{A}\,\overline{B}C\overline{E} + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{B}C\overline{D} + CD\overline{E} + BD\overline{E}$
        v. $F(A,B,C,D,E) = ABE(\overline{C}D + \overline{D}) + \overline{A}(\overline{C}E + \overline{B}D)$
        w. $F(V,W,X,Y,Z) = \sum m\ (1,3,9,13,26,27,30,31)$
        x. $F(A,B,C,D,E) = \Pi M\ (0,1,5,11,16,18,22,25,29,31)$

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y. $F(A,B,C,D,E) = \Pi M\ (0,4,8,12,16,20,24,28)$

z. $F(A,B,C,D,E) = (A+\overline{B}+\overline{C})(\overline{A}+D+\overline{E})(\overline{C}+\overline{D}+E)(B+\overline{C})$

16. Construct a 4x16 decoder using:
    a. Two 3x8 decoders. b. Five 2x4 decoders.

17. Use a 4x16 decoder and a 16x4 encoder to convert a BCD number to excess-3.

18. Construct a 16x1 multiplexer using two 8x1 and one 2x1 multiplexers.

19. Having two inputs A,B and a number of select lines and an output F. Design the following functions using a multiplexer (with the mentioned size) and any other gate you need:
    a. If (S=0) then F= $\overline{A}$
       If (S=1) then F=A+B
       If (S=2) then F=AB
       If (S=3) then F=A⊕B — 4x1 Multiplexer
    b. If (S =0) then F=A
       If (S=1) then F=AB
       If (S=2) then F=A+B
       If (S=3) then F=A⊕B
       If (S=4) then F= $\overline{A}$
       If (S=5) then F= $\overline{AB}$
       If (S=6) then F= $\overline{A+B}$ — By two ways the first with 4x1 Multiplexer
       If (S=7) then F= $\overline{A \oplus B}$ — and the other by 8x1 Multiplexer
    c. If (S=0) then F=A
       If (S=1) then F=A+B (Addition)
       If (S=2) then F=A-B
       If (S=3) then F=0 — 4x1 Multiplexer and a full adder and an XOR

20. Design each of the following functions F using a multiplexer with the mentioned size:
    a. $F(X,Y,Z) = \sum_m (0,1,3,5,6)$ — 8x1 Multiplexer
    b. $F(W,X,Y,Z) = \sum_m (0,1,4,5,10,12,14)$ — 4x1 Multiplexer
    c. $F(W,X,Y,Z) = \prod_M (0,2,5,6,9,11,12,15)$ — 4x1 Multiplexer
    d. $F(A,B,C,D) = \overline{AB} + \overline{B}\overline{C} + CD + \overline{AD}$ — 4x1 Multiplexer
    e. $F(A,B,C,D,E) = ABE(\overline{C}D + \overline{D}) + \overline{A}(\overline{C}E + \overline{B}D)$ — 8x1 Multiplexer
    f. $F(V,W,X,Y,Z) = \sum m\ (1,3,9,13,26,27,30,31)$ — 4x1 Multiplexer

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21. Having a number of four digits A,B,C,D and an output F, use a multiplexer to design the following functions *(First determine its optimal size)*:

a.

B	C	F
0	X	1
1	0	0
1	1	$\overline{A}$

b.

A	B	F
0	0	0
0	1	1
1	0	C
1	1	D

c.

A	B	C	F
0	0	0	C
0	0	1	A
0	1	0	B
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	$\overline{D}$
1	1	1	0

d.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	X	A
0	1	0	0	B
0	1	0	1	0
0	1	1	X	$\overline{C}$
1	X	X	X	A

e. If (A=0) then F=$\overline{C}$ else F=B
f. If (A=1) then F=D else F=C
g. If (A=B) then F=D else F=$\overline{C}$
h. If (A<>B) then F=0 else F=1
i. If (ABC=000) then F=C else F=$\overline{C}$
j. If (A=B=C) then F=D else F=C
k. If (A=B and C=D) then F=1 else F=0
l. If (A=0 and B=1 or C<>D) then F=D else F=ABC
m. If (ABCD is an odd number) F=1 else F=0
n. If (AB=CD) then F=1
    else If (AB=11 or CD=11) then F=1
        else If (AB=00 and CD=10) then F=0
            else F=AB

22. Using a 4-bit comparator and a Quad 2-1 multiplexer, design a circuit that outputs the larger of two numbers.

23. Design a combinational circuit whose inputs are two 8-bit binary number X and Y, and a control signal Min/Max. The output of the circuit is a 8-bit binary number Z, such that Z=0 if X=Y; otherwise Z=min(X,Y) if Min/Max=1, and Z=max(X,Y) if Min/Max=0.

24. Using Quad 8x1 multiplexer to build the functions in this table, where A, B and F are 4-bit I/O.

Inputs			
S_2	S_1	S_0	Function
0	0	0	F=0000

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0	0	1	F=B minus A plus CIN
0	1	0	F=A minus B plus CIN
0	1	1	F=A plus B plus CIN
1	0	0	F=A xor B
1	0	1	F=A or B
1	1	0	F=A and B
1	1	1	F=1111

25. Calculate the propagation delays for the following circuit known the propagation delay of the following gates: NOT gate = 3 nsec

OR gate = 10 nsec	AND gate = 10 nsec	NOR gate = 13 nsec
NAND gate = 13 nsec	XOR gate = 20 nsec	XNOR gate = 23 nsec

a. Full adder.
b. 3x8 decoder.
c. 16x1 Multiplexer.