



Faculty of Computers and Artificial Intelligence  
Cairo University

Midterm Exam



Program: Computer Science / Software Engineering  
Course Name: Computer Organization and Architecture  
Course Code: CS331  
Instructor(s): Dr. Amin Allam

Date: 27/11/2021  
Duration: 1 hour  
Total Marks: 20 marks

تعليمات هامة:

- حيلة التليفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضروري الدخول بالمحمول فيوضع مغلقة في الحقيبة.
- لا يسمح بدخول سماعة الأذن أو البلوتوث.
- لا يسمح بدخول أي كتب أو ملزم أو أوراق داخل اللجنة والمخالفة تعتبر حالة غش.

- Exam consists of 20 multiple-choice questions in 3 pages. Each question weights 1 mark.
- Record in the bubble sheet exactly ONE answer for each question.

Qa ⇒ Given the characteristic table of the JK flip-flop:

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

For questions 1 to 4, consider an electronic circuit which consists of the following items:

- A positive edge-triggered JK flip-flop with inputs: clock,  $J_0$ ,  $K_0$ , and output:  $A_0$ .
- Another positive edge-triggered JK flip-flop with inputs: clock,  $J_1$ ,  $K_1$ , and output:  $A_1$ .
- Logic 1 is connected to both  $J_0$  and  $K_0$ .
- $A_0$  is connected to both  $J_1$  and  $K_1$ .

1 Assuming  $A_1 = 0$  and  $A_0 = 0$  while clock input is logic 0. After the clock input becomes logic 1, the values of  $A_1$  and  $A_0$  become:

- ☐ A  $A_1 = 0, A_0 = 0$  ☐ B  $A_1 = 0, A_0 = 1$  ☐ C  $A_1 = 1, A_0 = 0$  ☒ D  $A_1 = 1, A_0 = 1$  ☐ E unknown

2 Assuming  $A_1 = 0$  and  $A_0 = 1$  while clock input is logic 0. After the clock input becomes logic 1, the values of  $A_1$  and  $A_0$  become:

- ☒ A  $A_1 = 0, A_0 = 0$  ☐ B  $A_1 = 0, A_0 = 1$  ☐ C  $A_1 = 1, A_0 = 0$  ☐ D  $A_1 = 1, A_0 = 1$  ☐ E unknown

3 Assuming  $A_1 = 1$  and  $A_0 = 1$  while clock input is logic 0. After the clock input becomes logic 1, the values of  $A_1$  and  $A_0$  become:

- ☐ A  $A_1 = 0, A_0 = 0$  ☐ B  $A_1 = 0, A_0 = 1$  ☒ C  $A_1 = 1, A_0 = 0$  ☐ D  $A_1 = 1, A_0 = 1$  ☐ E unknown

4 The above circuit is:

- ☐ A half adder ☒ B shift register ☐ C binary counter ☐ D bus ☐ E other

**Qb**

$\Rightarrow$  A  $4 \times 1$  multiplexer with selection inputs  $S_1$  and  $S_0$  selects input 0 when  $S_1 S_0 = 00$ , selects input 1 when  $S_1 S_0 = 01$ , selects input 2 when  $S_1 S_0 = 10$ , and selects input 3 when  $S_1 S_0 = 11$ .

For questions 5 to 10, consider an electronic circuit which has:

- Inputs:  $S_1, S_0, C_0$ , the binary number  $F = F_1 F_0$ , and the binary number  $G = G_1 G_0$ .
- output: the binary number  $V = V_1 V_0$ .

The circuit consists of the following items:

- A  $4 \times 1$  multiplexer with selection inputs  $S_1, S_0$ , and 4 inputs:  $Q_0, Q_1, Q_2, Q_3$ , and output:  $M_0$ .
- Another  $4 \times 1$  multiplexer with selection inputs  $S_1, S_0$ , and 4 inputs:  $R_0, R_1, R_2, R_3$ , and output:  $M_1$ .
- A full-adder with inputs:  $F_0, M_0, C_0$  and outputs:  $C_1$  (carry),  $V_0$  (sum).
- Another full-adder with inputs:  $F_1, M_1, C_1$  and outputs:  $C_2$  (carry),  $V_1$  (sum).
- $\overline{G_0}$  is connected to  $Q_0$ . •  $\overline{G_1}$  is connected to  $R_0$ . •  $G_0$  is connected to  $Q_1$ . •  $G_1$  is connected to  $R_1$ .
- Logic 1 is connected to both  $Q_2$  and  $R_2$ . • Logic 0 is connected to both  $Q_3$  and  $R_3$ .

**5** After  $S_1 = 0, S_0 = 0, C_0 = 0$ , the output  $V$  will equal to:

- ☐ A  $F + G$  ☐ B  $F - G$  ☐ C  $F + G + 1$  ☒ D  $F - G - 1$  ☐ E  $F - G + 1$

**6** After  $S_1 = 0, S_0 = 0, C_0 = 1$ , the output  $V$  will equal to:

- ☐ A  $F + G$  ☒ B  $F - G$  ☐ C  $F + G + 1$  ☐ D  $F - G - 1$  ☐ E  $F - G + 1$

**7** After  $S_1 = 0, S_0 = 1, C_0 = 1$ , the output  $V$  will equal to:

- ☐ A  $F + G$  ☐ B  $F - G$  ☒ C  $F + G + 1$  ☐ D  $F - G - 1$  ☐ E  $F - G + 1$

**8** After  $S_1 = 1, S_0 = 0, C_0 = 0$ , the output  $V$  will equal to:

- ☐ A  $F + G$  ☐ B  $F - G$  ☐ C  $F + 1$  ☒ D  $F - 1$  ☐ E  $F$

**9** After  $S_1 = 1, S_0 = 0, C_0 = 1$ , the output  $V$  will equal to:

- ☐ A  $F + G$  ☐ B  $F - G$  ☐ C  $F + 1$  ☐ D  $F - 1$  ☒ E  $F$

**10** After  $S_1 = 1, S_0 = 1, C_0 = 1$ , the output  $V$  will equal to:

- ☐ A  $F + G$  ☐ B  $F - G$  ☒ C  $F + 1$  ☐ D  $F - 1$  ☐ E  $F$

**Qc** **11** The outputs of 16 registers are connected to the inputs of a bus. Each register stores 32 bits. The bus selects the outputs of one of the input registers according to the selection inputs of the bus. The bus must have the following number of **selection inputs**:

- ☐ A 3 ☐ B 4 ☐ C 5 ☒ D 16 ☐ E 32

**12** The outputs of 16 registers are connected to the inputs of a bus. Each register stores 32 bits. The bus selects the outputs of one of the input registers according to the selection inputs of the bus. The bus must have the following number of **multiplexers**:

- ☐ A 3 ☐ B 4 ☐ C 5 ☒ D 16 ☐ E 32

**13** A memory unit contains 2048 words. Each word is 32 bits. The number of **input address lines** to this memory unit is:

- ☐ A 5 ☐ B 10 ☒ C 11 ☐ D 16 ☐ E 32

**14** A memory unit contains 2048 words. Each word is 32 bits. The number of **data output lines** out of this memory unit is:

- ☐ A 5 ☐ B 10 ☐ C 11 ☐ D 16 ☒ E 32

**15** After applying **arithmetic shift right** to a 6-bit register containing the binary number 101100 it becomes:

- ☐ A 010110 ☒ B 110110 ☐ C 011001 ☐ D 011000 ☐ E 111100

**16** Comparing two numbers to know whether they are equal or not equal, can be done by:

- ☐ A bitwise and ☐ B bitwise or ☒ C bitwise xor ☐ D bitwise complement ☐ E arithmetic shift

**17** Consider the ADD instruction which increases the value of the accumulator register by the value located at the effective address. If the instruction uses **direct** addressing and it contains the address 10 in its address field. The memory word at address 10 contains the value 30, and the memory word at address 30 contains the value 45. After the instruction is executed, the accumulator register increases by:

- ☐ A 10 ☒ B 30 ☐ C 40 ☐ D 45 ☐ E 75

**18** Consider the ADD instruction which increases the value of the accumulator register by the value located at the effective address. If the instruction uses **indirect** addressing and it contains the address 10 in its address field. The memory word at address 10 contains the value 30, and the memory word at address 30 contains the value 45. After the instruction is executed, the accumulator register increases by:

- ☐ A 10 ☐ B 30 ☐ C 40 ☒ D 45 ☐ E 75

**19** The following register contains the address of the instruction that is going to be executed:

- ☒ A Program counter ☐ B Accumulator ☐ C Instruction register ☐ D Input register ☐ E Data register

**20** Assume that 2 clock cycles are required on average to execute any instruction. The time required to execute a program containing 10,000 instructions on a computer with a clock rate of 5,000,000 clock cycles per second is:

- ☐ A 0.001 seconds ☐ B 0.002 seconds ☒ C 0.004 seconds ☐ D 500 seconds ☐ E 1000 seconds