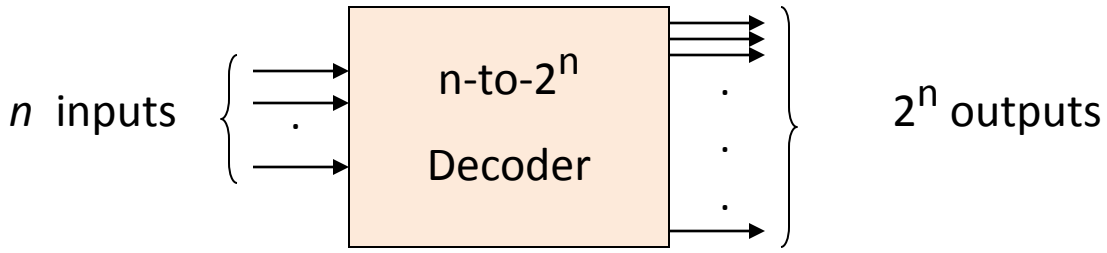
Sheet 5- Decoder and Multiplexer

Decoder



- A binary decoder is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs
- A decoder is a minterm generator
- Minterm of F= Maxterm of F’

Question 12(m)

- Design each of the following functions F using a decoder *(First decide the optimal size of the chip needed)*

  m) $F(W,X,Y,Z) = \sum_m (0,1,4,5,10,12,14)$

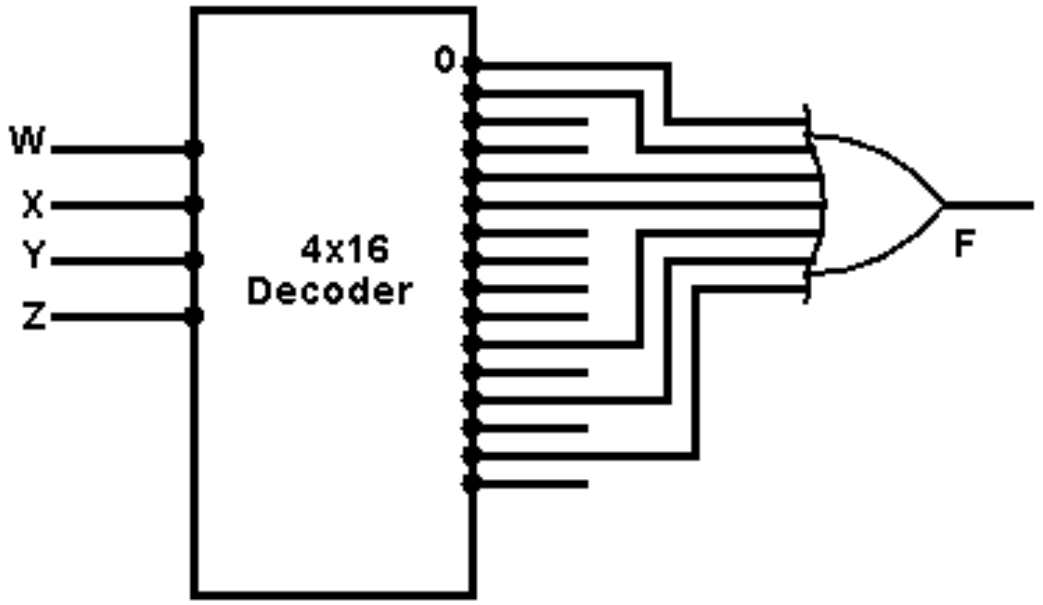
Using OR

Solution 12(m)

Number of inputs =4

So decoder size is $4x\mathbf{2^4}=4x16$

$F(W,X,Y,Z) = \sum_m (0,1,4,5,10,12,14)$



Question 12(e)

- Design each of the following functions F using a decoder *(First decide the optimal size of the chip needed)*

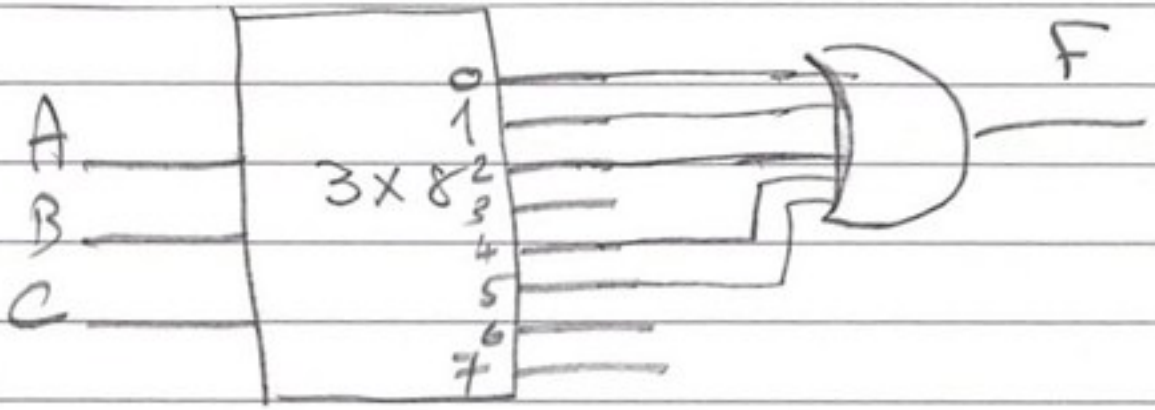
e) $F(A,B,C) = \prod_M (3,6,7)$

Question 12(e)

$F(A, B, C) = \Pi M(3, 6, 7)$ Using OR

$= \Sigma m(0, 1, 2, 4, 5)$ OR → minterms

3 inputs → 3×8 decoder



Question 12(i)

- Design each of the following functions F using a decoder *(First decide the optimal size of the chip needed)*

  i) $F(X,Y,Z) = X + Y(X+Z)(\overline{X}+\overline{Z})$

Question 12(i)

i) $F(X,Y,Z) = X + Y(X+Z)(\bar{X}+\bar{Z})$ → maxterms (using NOR)

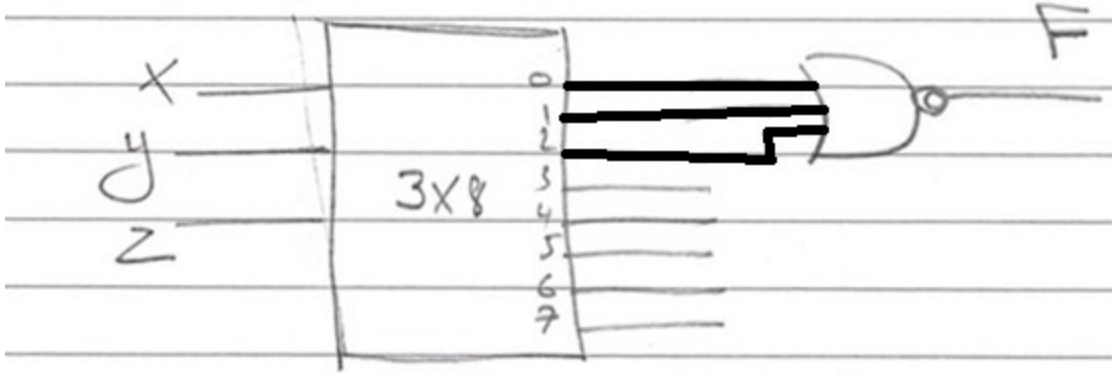
$= X + Y(X\bar{X} + X\bar{Z} + \bar{X}Z + Z\bar{Z})$

$= X + XY\bar{Z} + \bar{X}YZ$

X \ YZ	00	01	11	10
0			1	
1	1	1	1	1

$F(X,Y,Z) = \overline{\Pi M}\,(0,1,2)$

3 inputs → 3x8 decoder



Question 12(s)

- Design each of the following functions F using a decoder *(First decide the optimal size of the chip needed)*

s) $F(W,X,Y,Z) = (W + X + \overline{Y} + \overline{Z})(\overline{X} + \overline{Y} + Z)(\overline{W} + Y + \overline{Z})$

Question 12(s)

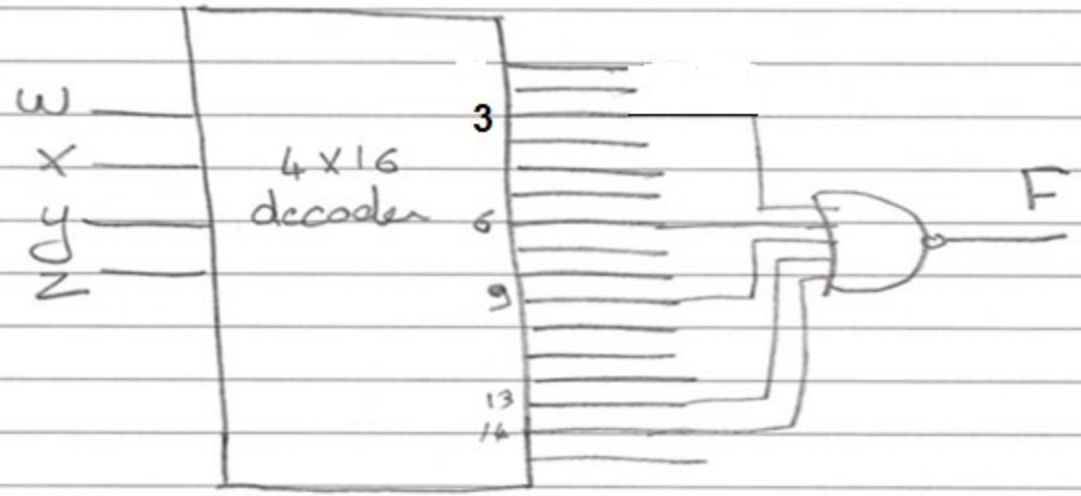
(s) $F(w, x, y, z) = (w + x + \bar{y} + z)(\bar{x} + \bar{y} + z)(\bar{w} + y + \bar{z})$

wx \ yz	00	01	11	10
00			0	
01				0
11		0		0
10		0		

Using NOR → max terms

$F(w, x, y, z) = \Pi M(3, 6, 9, 13, 14)$

4 inputs → 4 × 16 decoder



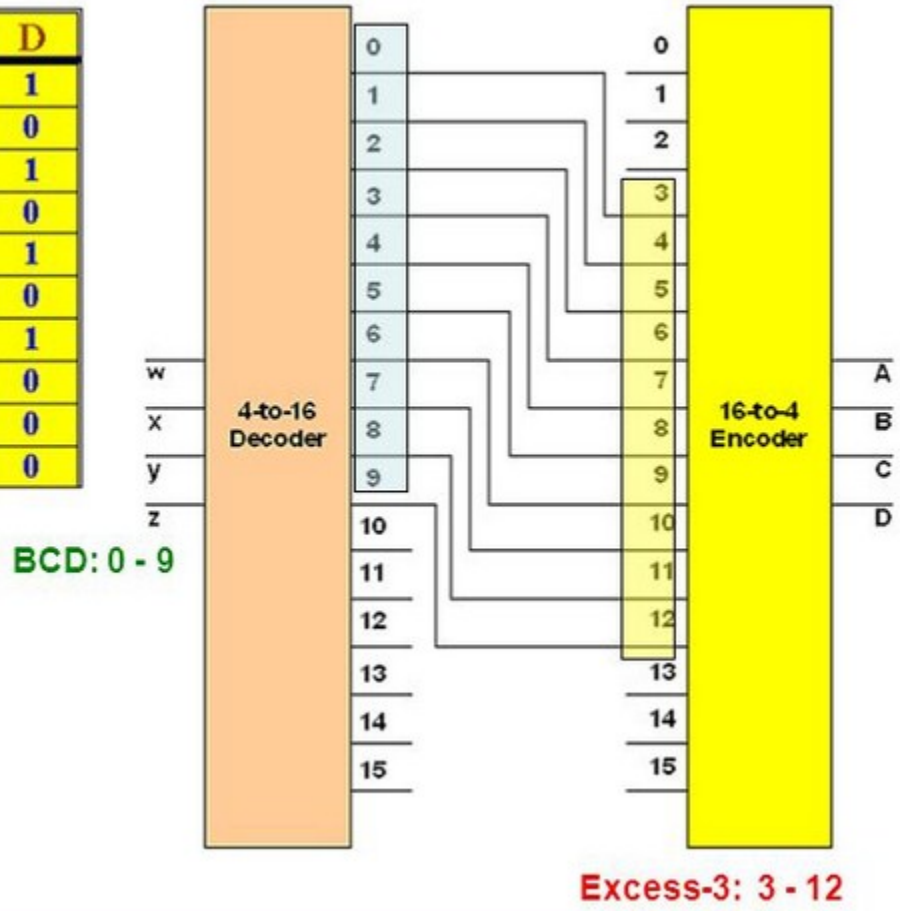
Question 14 covered in Lec.

14. Use a 4x16 decoder and a 16x4 encoder to convert a BCD number to excess-3.

Question 14

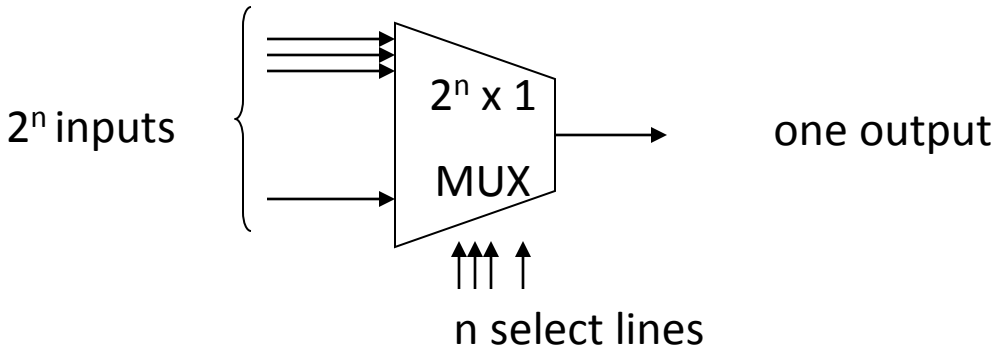
14. Use a 4x16 decoder and a 16x4 encoder to convert a BCD number to excess-3.

	BCD				Excess-3			
Index	w	x	y	z	A	B	C	D
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	0
9	1	0	0	1	1	1	0	0



Multiplexers

- Is a combinational circuit
- Has a single output
- Directs one of 2^n input to the output
- Input to output direction is done based on a set of n select bits



Question 17 (a)

17. Having two inputs A,B and a number of select lines and an output F. Design the following functions using a multiplexer (with the mentioned size) and any other gate you need:

a. If (S=0) then F= $\overline{A}$

If (S=1) then F=A+B

If (S=2) then F=AB

If (S=3) then F=A⊕B 4x1 Multiplexer

Question 17 (a)

17. Having two inputs A,B and a number of select lines and an output F. Design the following functions using a multiplexer (with the mentioned size) and any other gate you need:

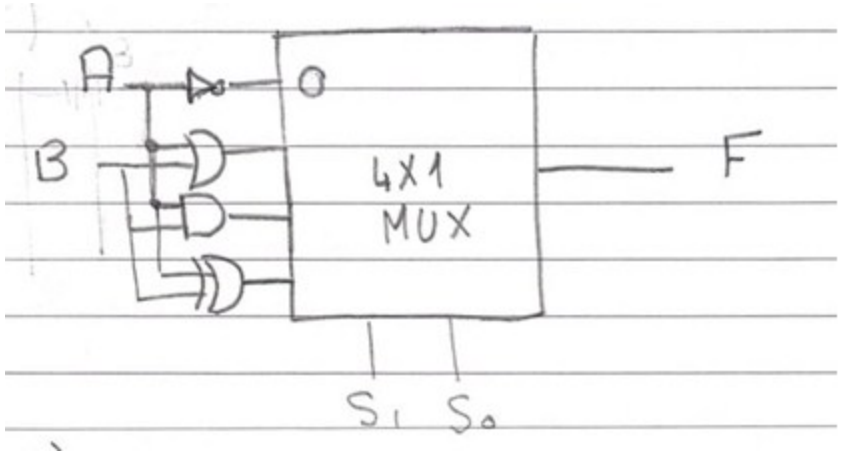
a. If (S=0) then F= $\overline{A}$

If (S=1) then F=A+B

If (S=2) then F=AB

If (S=3) then F=A⊕B

4x1 Multiplexer



Question 15(q)

- Design each functions F in problem 12 using multiplexer *(First decide the optimal size of the chip needed).*

q) $F(A,B,C,D) = B\overline{C} + \overline{A}B + BC\overline{D} + \overline{A}\overline{B}D + A\overline{B}\overline{C}D$

Solution 15(q)

$$F(A,B,C,D) = B\overline{C} + \overline{A}B + BC\overline{D} + \overline{A}\,\overline{B}D + A\overline{B}\,\overline{C}D$$

Number of inputs =4

So Number of the multiplexer Selectors =

Number of inputs -1= 4-1=3

So Number of the Inputs' multiplexer is $\mathbf{2^3}$=8

So Size of the multiplexer = 8x1

We need to get the truth table of the function. The easiest way is to get the minterms using k-map.

Solution 15(q)

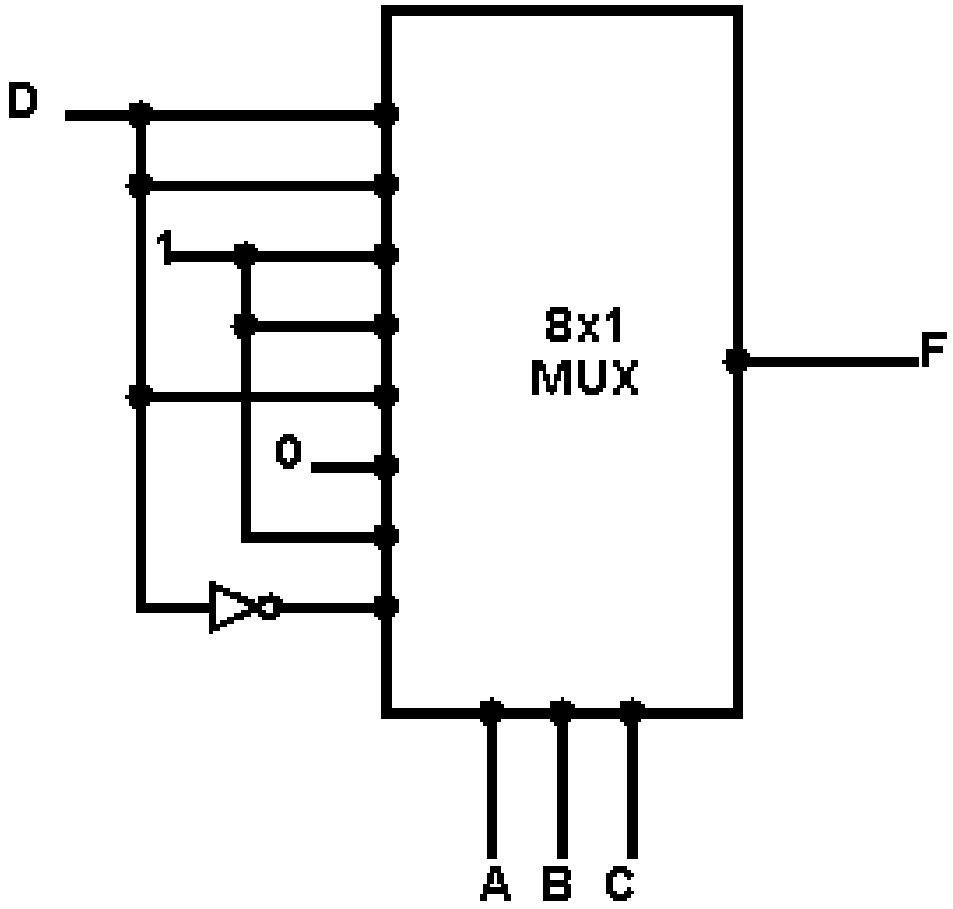
$$F(A,B,C,D) = B\overline{C} + \overline{A}B + BC\overline{D} + \overline{A}\overline{B}D + A\overline{B}\overline{C}D$$

AB \ CD	00	01	11	10
00		1	1	
01	1	1	1	1
11	1	1		1
10		1		

$F(A,B,C,D) = \sum_m (1,3,4,5,6,7,9,12,13,14)$

Solution 15(q)

	A	B	C	D	F	
0	0	0	0	0	0	F=D
1	0	0	0	1	1	
2	0	0	1	0	0	F=D
3	0	0	1	1	1	
4	0	1	0	0	1	F=1
5	0	1	0	1	1	
6	0	1	1	0	1	F=1
7	0	1	1	1	1	
8	1	0	0	0	0	F=D
9	1	0	0	1	1	
10	1	0	1	0	0	F=0
11	1	0	1	1	0	
12	1	1	0	0	1	F=1
13	1	1	0	1	1	
14	1	1	1	0	1	F=D’
15	1	1	1	1	0	



Question 15(l)

- Design the below function F using 4*1 multiplexer
- l) $F(A,B,C,D) = \sum_m (0,5,8,9,11,12,13,14)$

Question 15(l)

Sometimes they ask for a specific size of MUX to be used e.g. for

$F(A,B,C,D) = \sum m(0,5,8,9,11,12,13,14)$

The optimal size to be used is 8 X 1

It is needed to build it using 4 X 1 MUX

Question 15(l)

Used as selectors

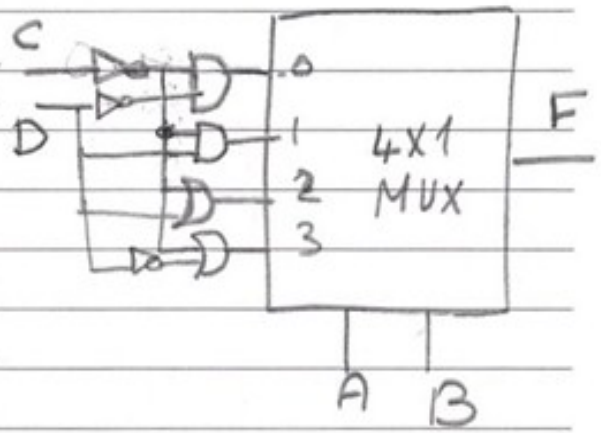
	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

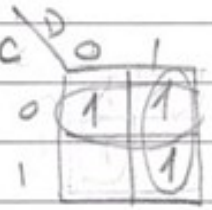
$F = \bar{C}\bar{D}$

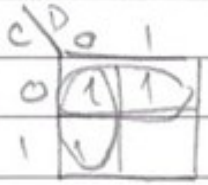
$F = \bar{C}D$

$F = \bar{C} + D$

$F = \bar{C} + \bar{D}$



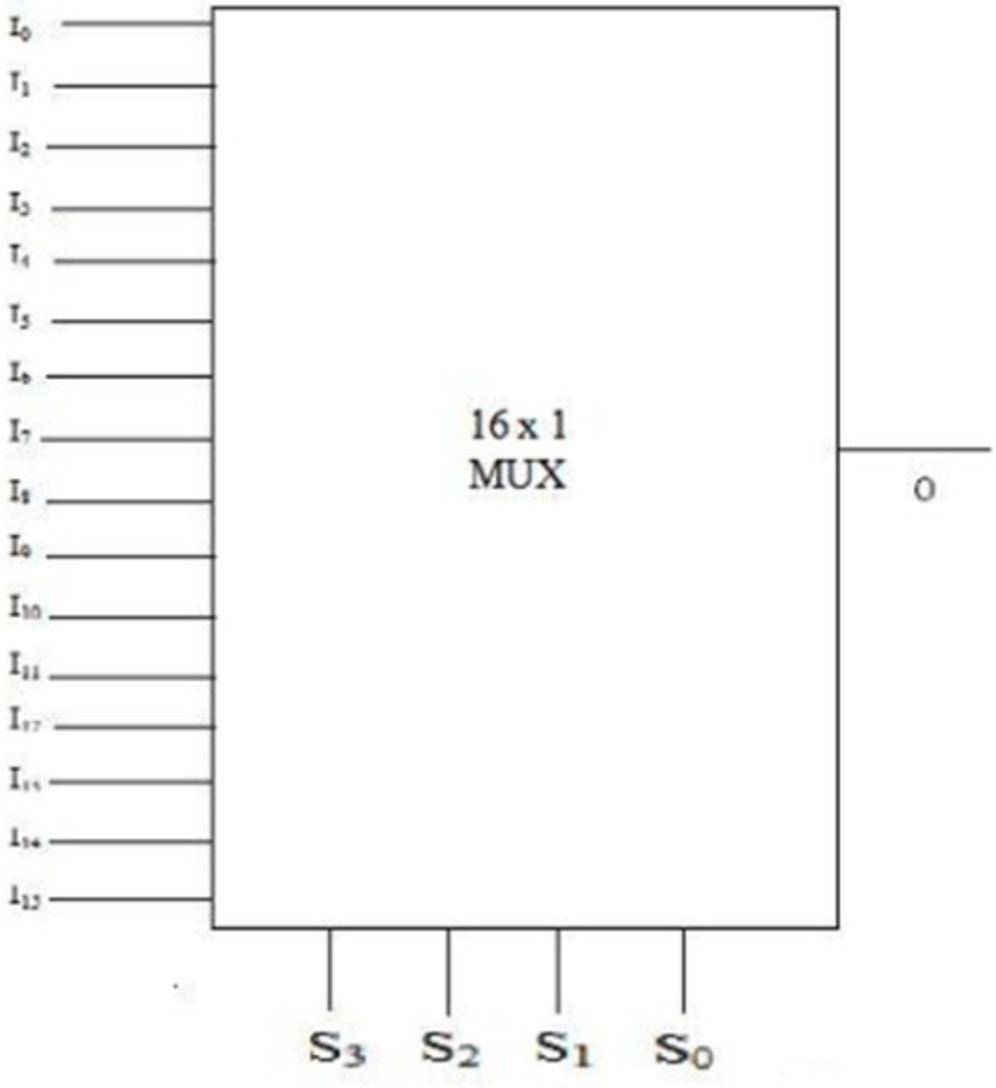




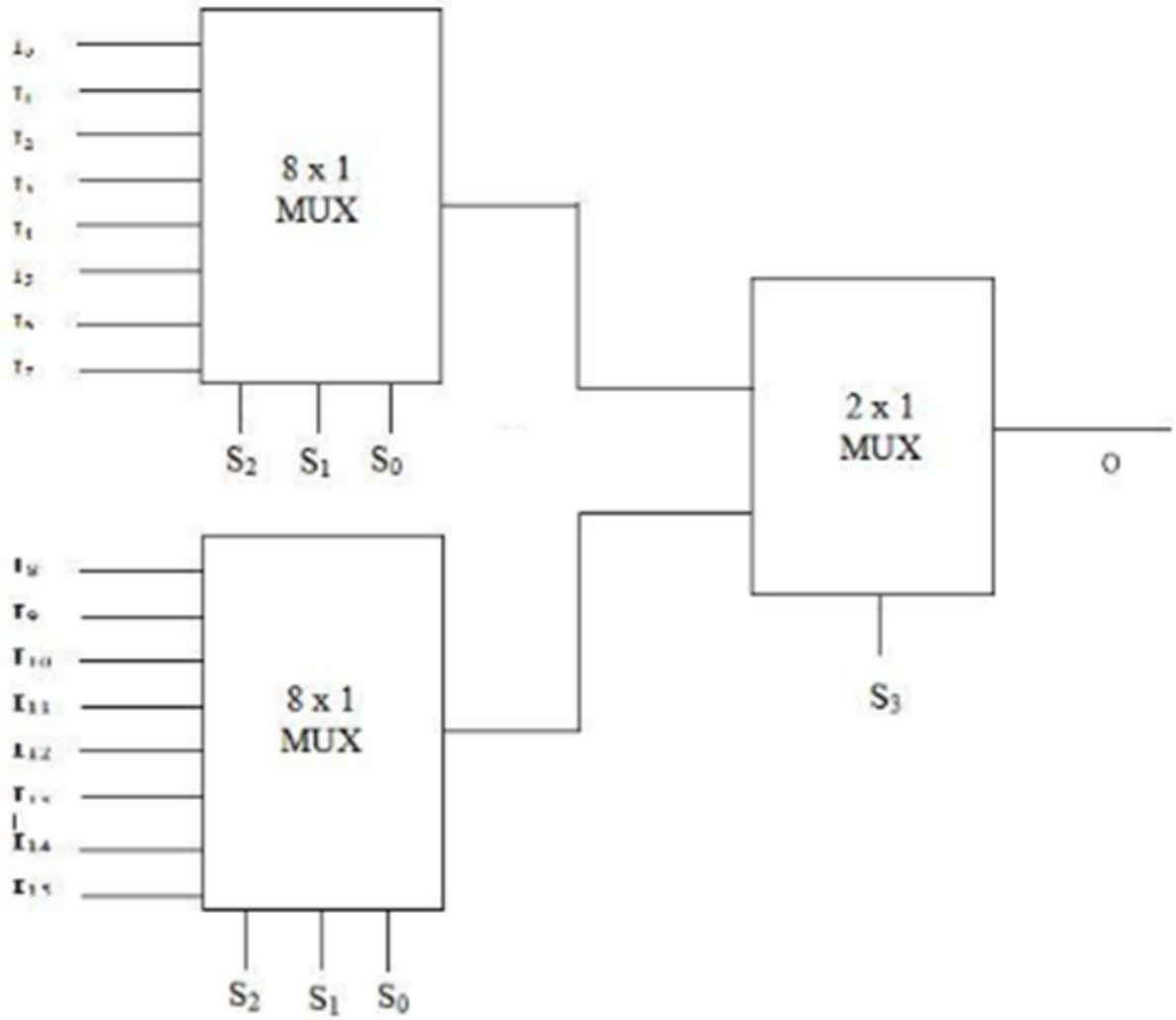
Question 16

- Construct a 16x1 multiplexer using two 8x1 and one 2x1 multiplexers

Solution 16



Solution 16



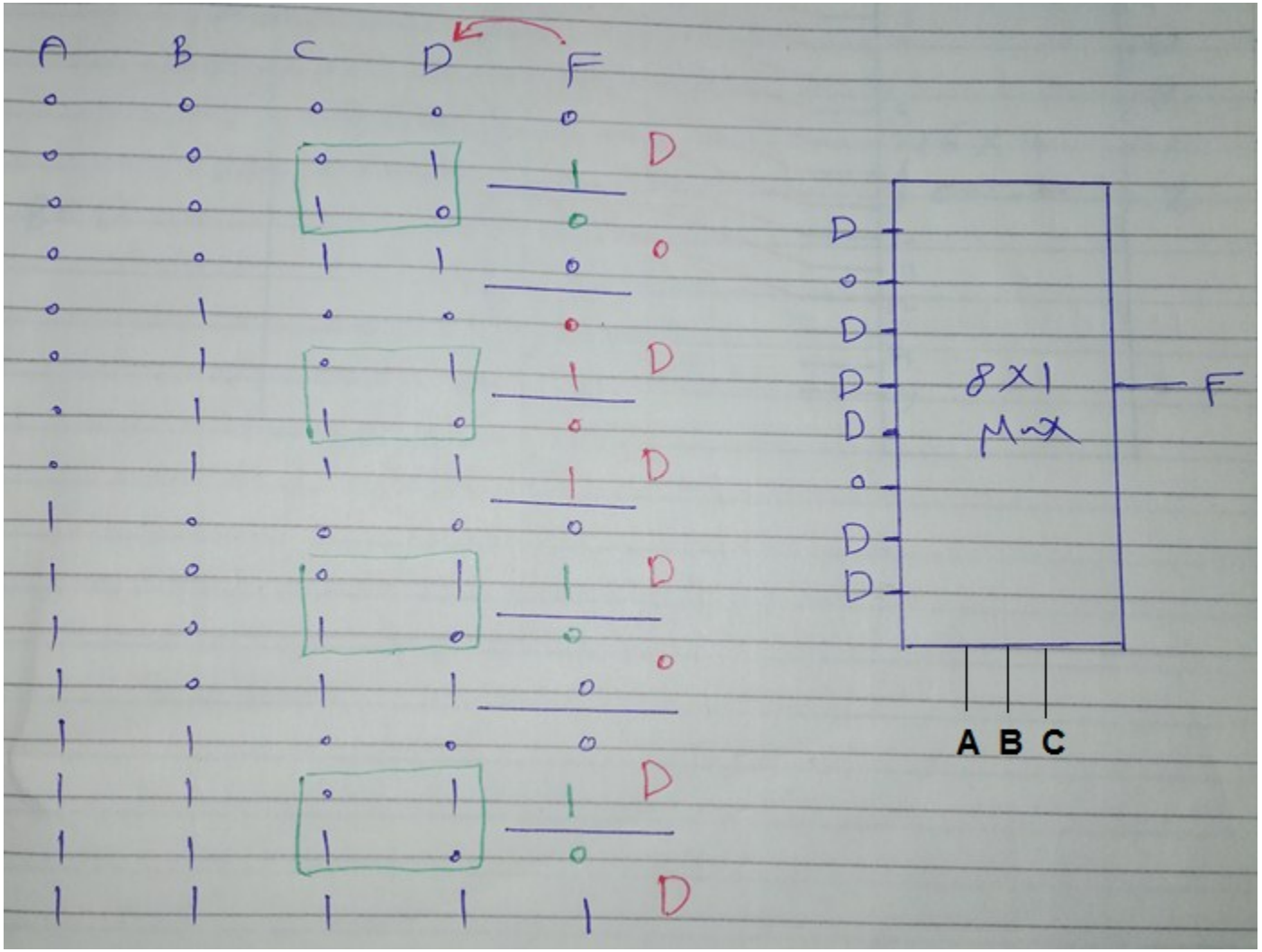
Question 18(k)

18. Having a number of four digits A,B,C,D and an output F, use a multiplexer to design the following functions *(First determine its optimal size)*:

k. If (A=0 and B=1 or C<>D) then F=D else F=ABC

Question 18(k)

k. If (A=0 and B=1 or C<>D) then F=D else F=ABC



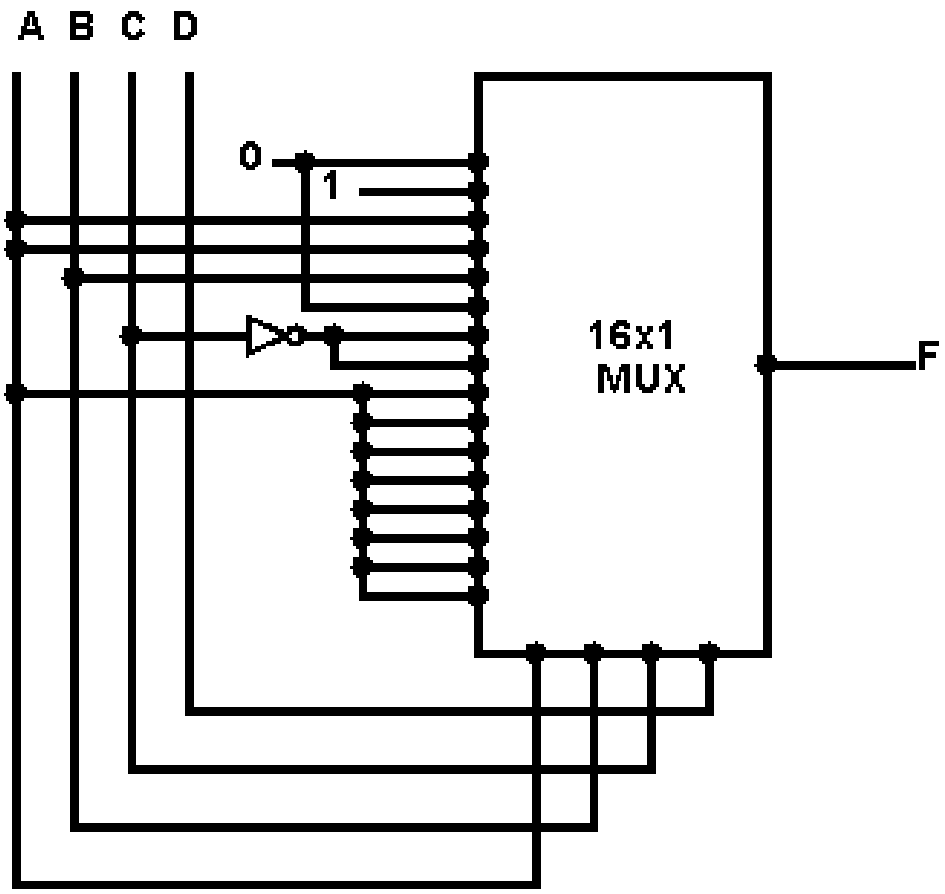
Question 18 (c)

Having a number of four digits A,B,C,D and an output F, use a multiplexer to design the following functions (First determine its optimal size)

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	X	A
0	1	0	0	B
0	1	0	1	0
0	1	1	X	C’
1	X	X	X	A

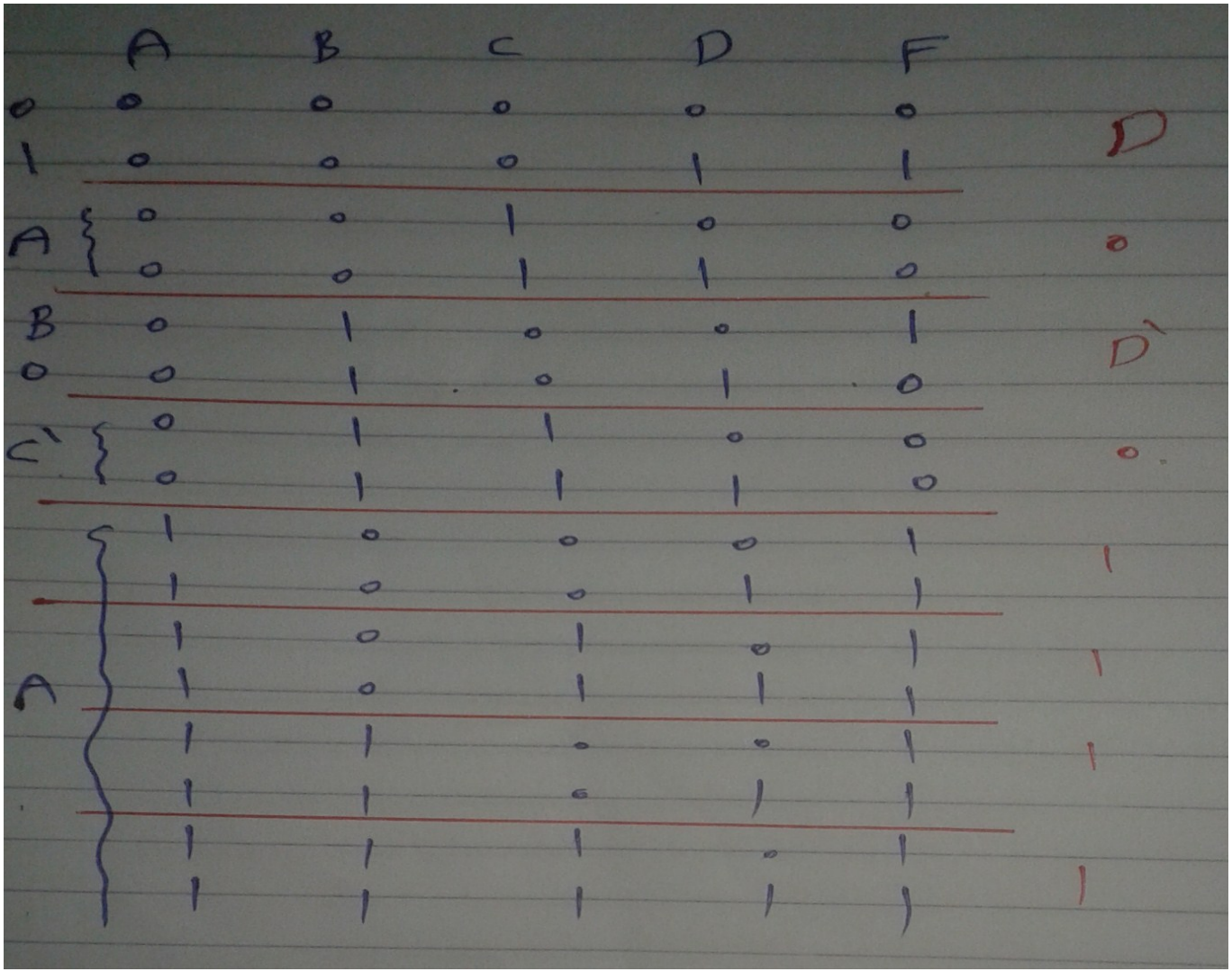
Solution 18(c)

	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	A
3	0	0	1	1	A
4	0	1	0	0	B
5	0	1	0	1	0
6	0	1	1	0	C’
7	0	1	1	1	C’
8	1	0	0	0	A
9	1	0	0	1	A
10	1	0	1	0	A
11	1	0	1	1	A
12	1	1	0	0	A
13	1	1	0	1	A
14	1	1	1	0	A
15	1	1	1	1	A

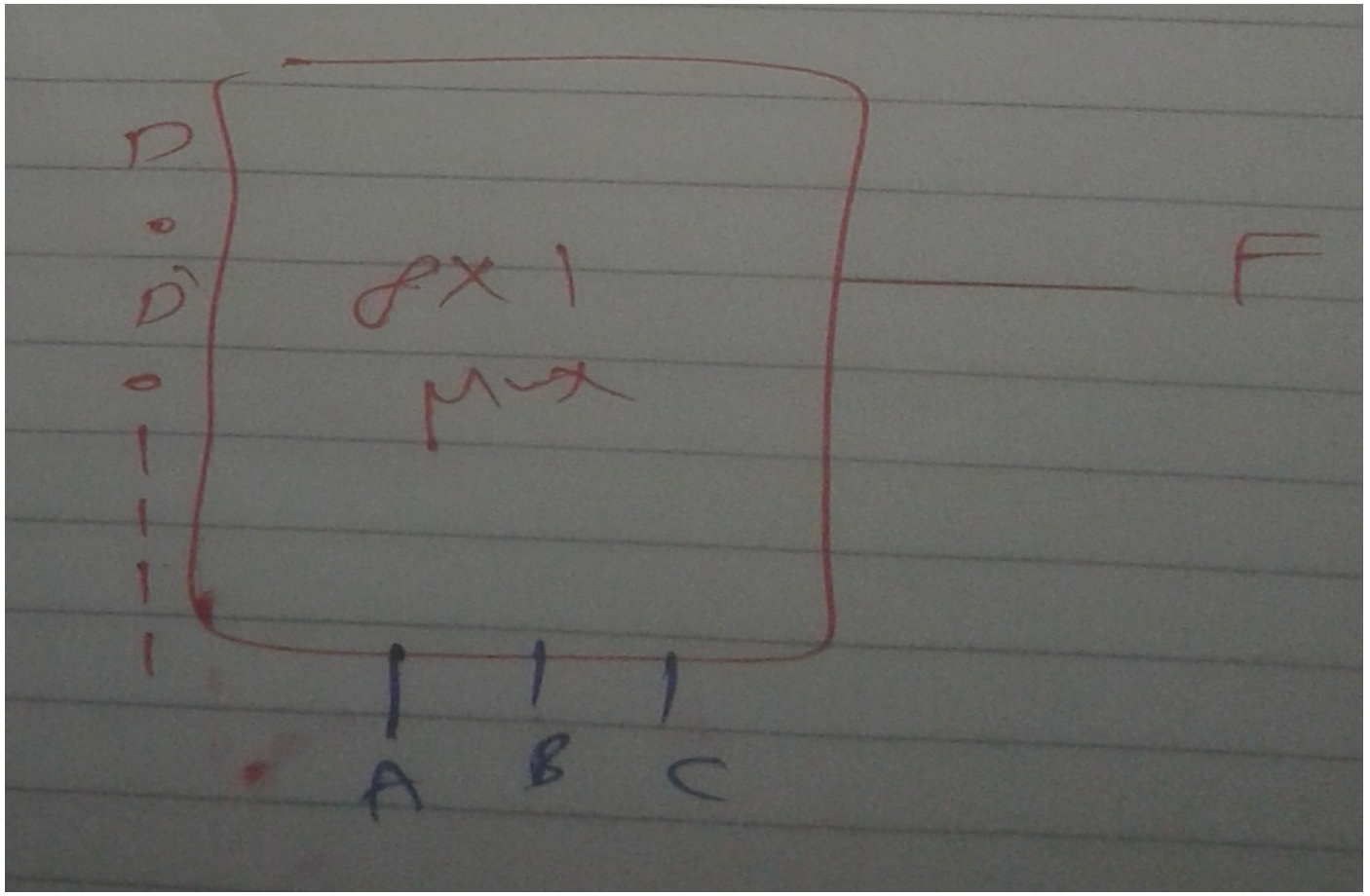


as F column includes variables not only ones and zeros so in this case Dr. allow you to consider No. of selectors = No. of inputs.

Solution 18(c)



Solution 18(c)



Question 18(g)

18. Having a number of four digits A,B,C,D and an output F, use a multiplexer to design the following functions *(First determine its optimal size)*:

g. If (A<>B) then F=0 else F=1

Question 18(g)

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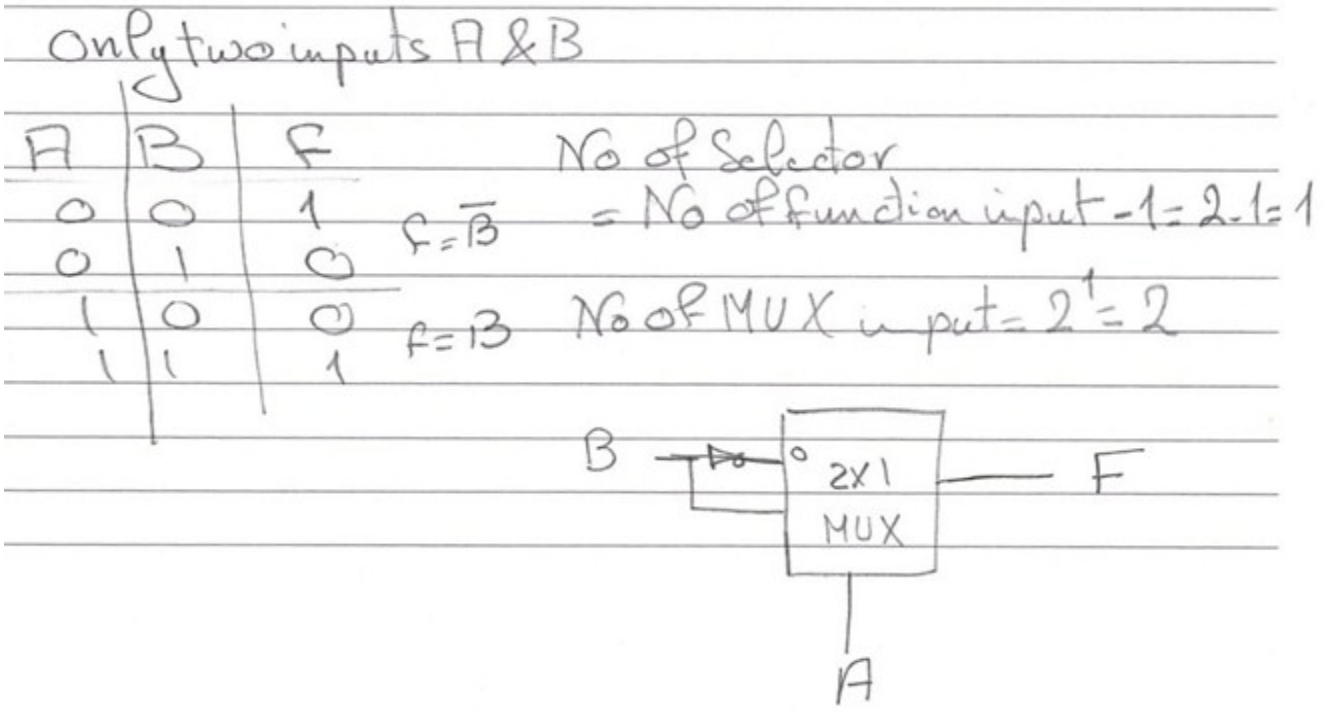


Question 18(l)

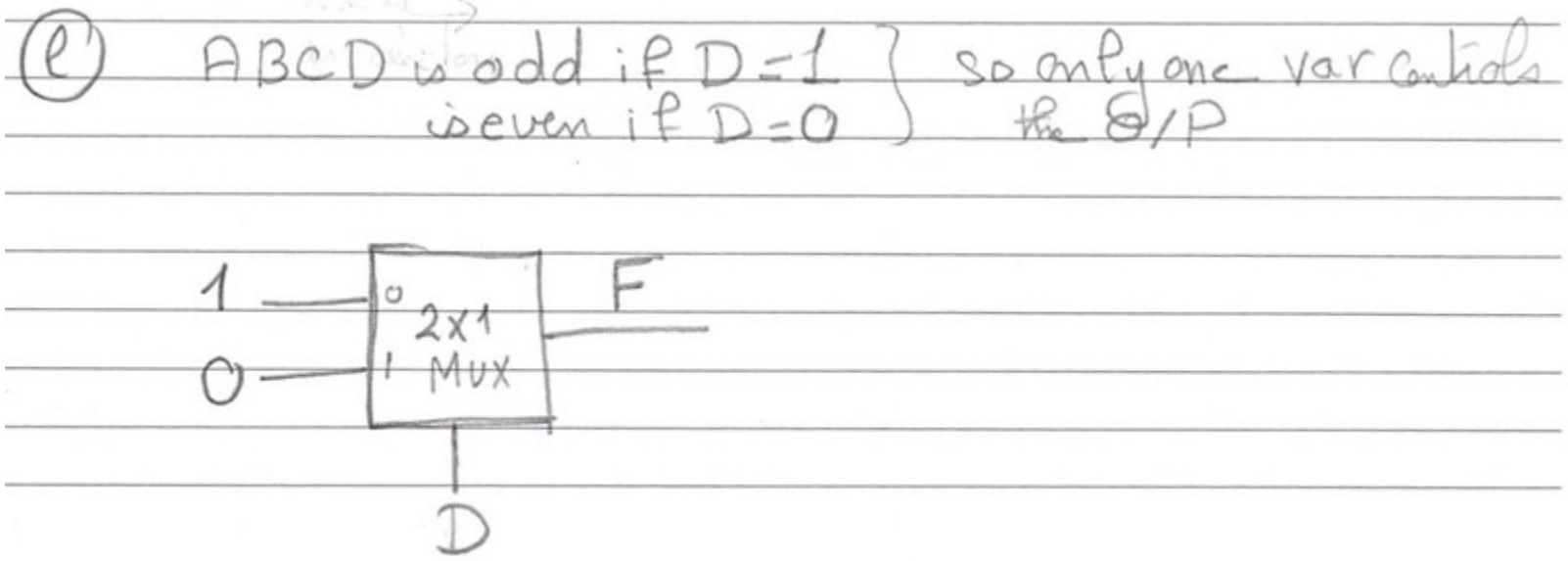
18. Having a number of four digits A,B,C,D and an output F, use a multiplexer to design the following functions *(First determine its optimal size)*:

l. If (ABCD is an odd number) F=0 else F=1

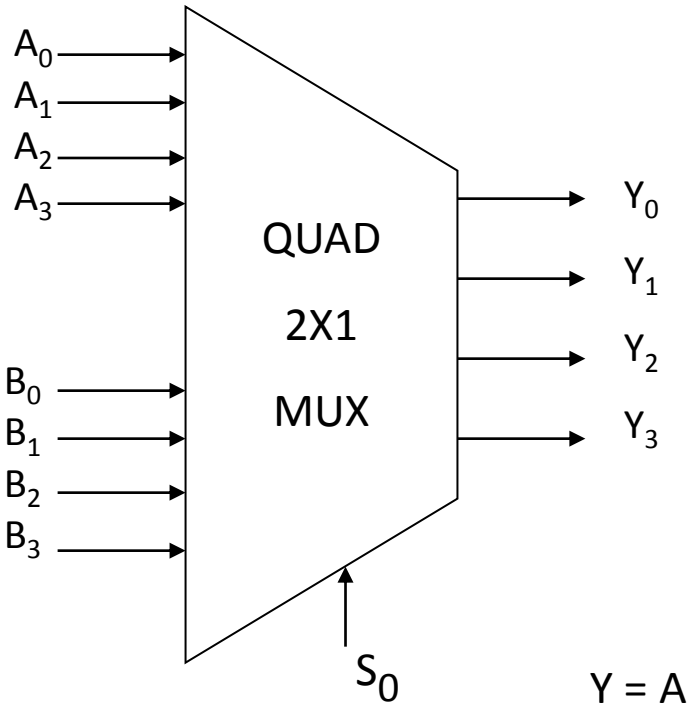
Question 18(l)

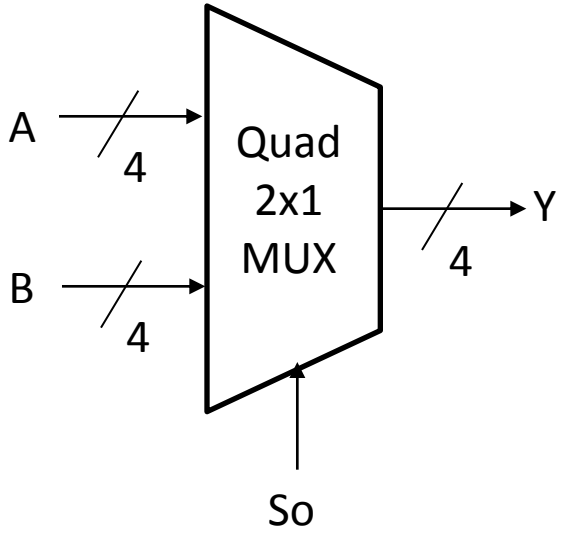
18. Having a number of four digits A,B,C,D and an output F, use a multiplexer to design the following functions *(First determine its optimal size)*:

l. If (ABCD is an odd number) F=0 else F=1



Quad 2x1 MUX





$Y = A$ If $S_0 = 0$

$Y = B$ if $S_0 = 1$

Question 19

19. Using a 4-bit comparator and a Quad 2-1 multiplexer, design a circuit that outputs the larger of two numbers.

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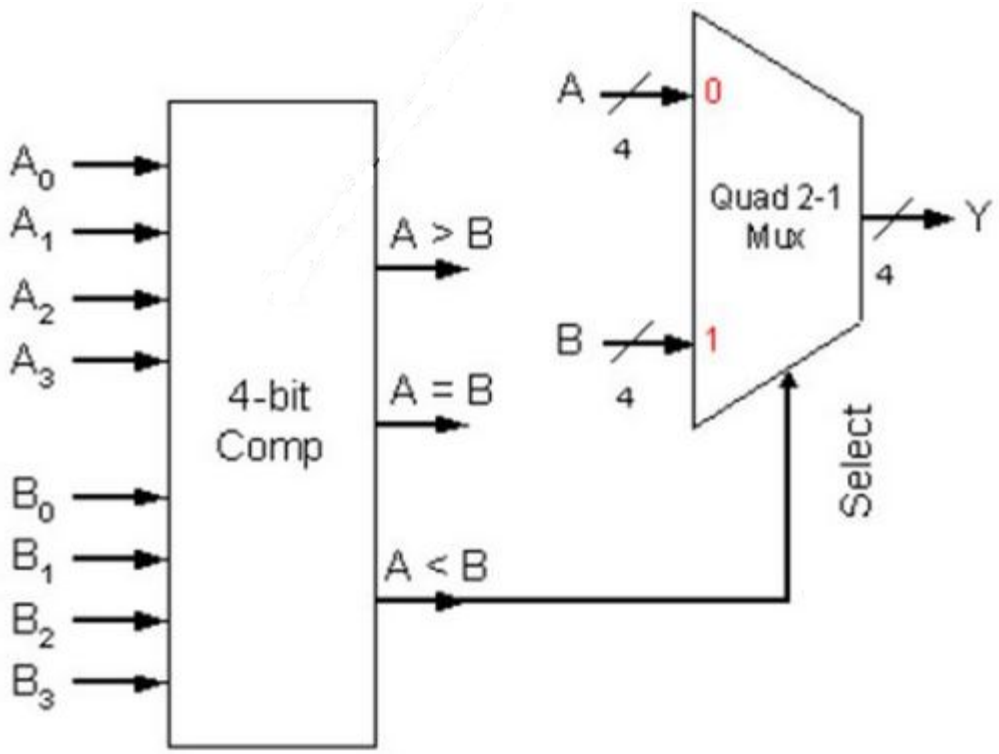
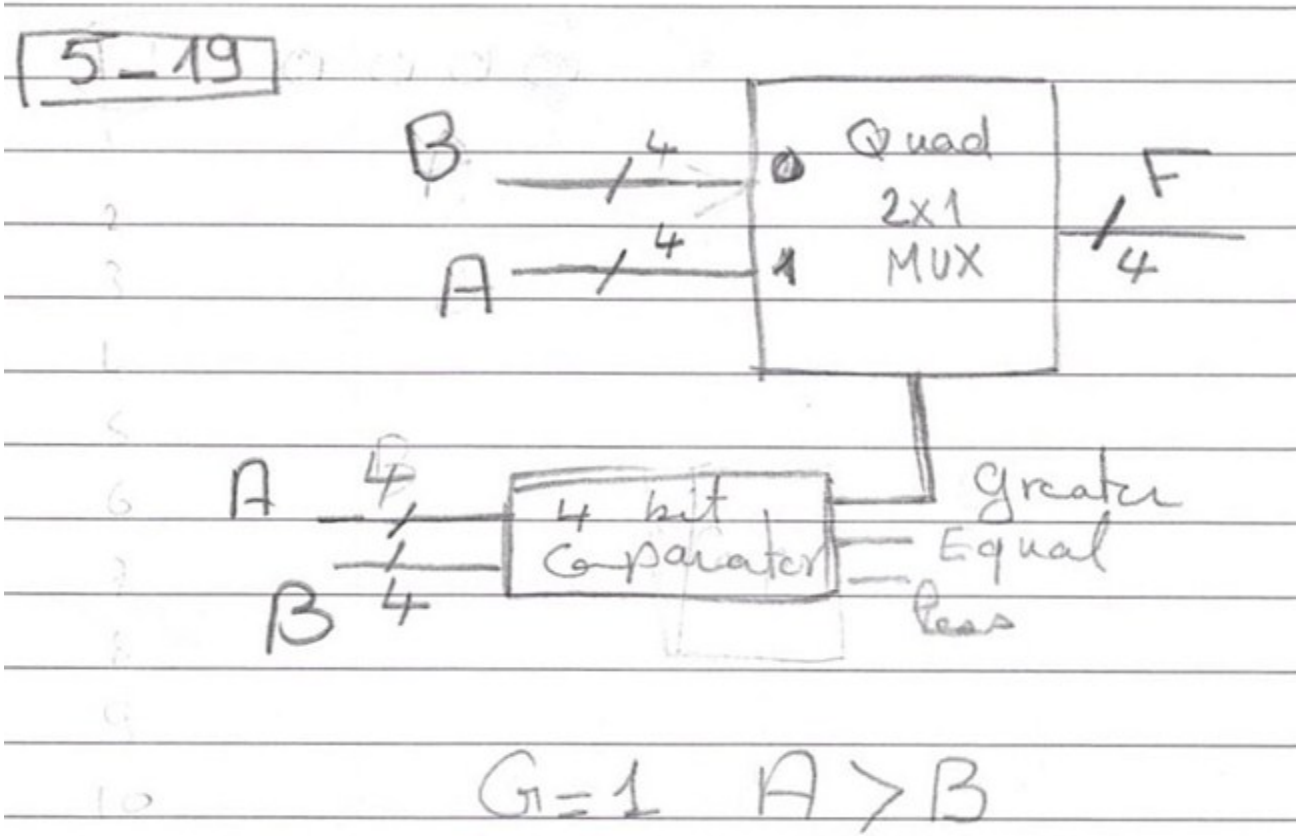


Question 19

19. Using a 4-bit comparator and a Quad 2-1 multiplexer, design a circuit that outputs the larger of two numbers.



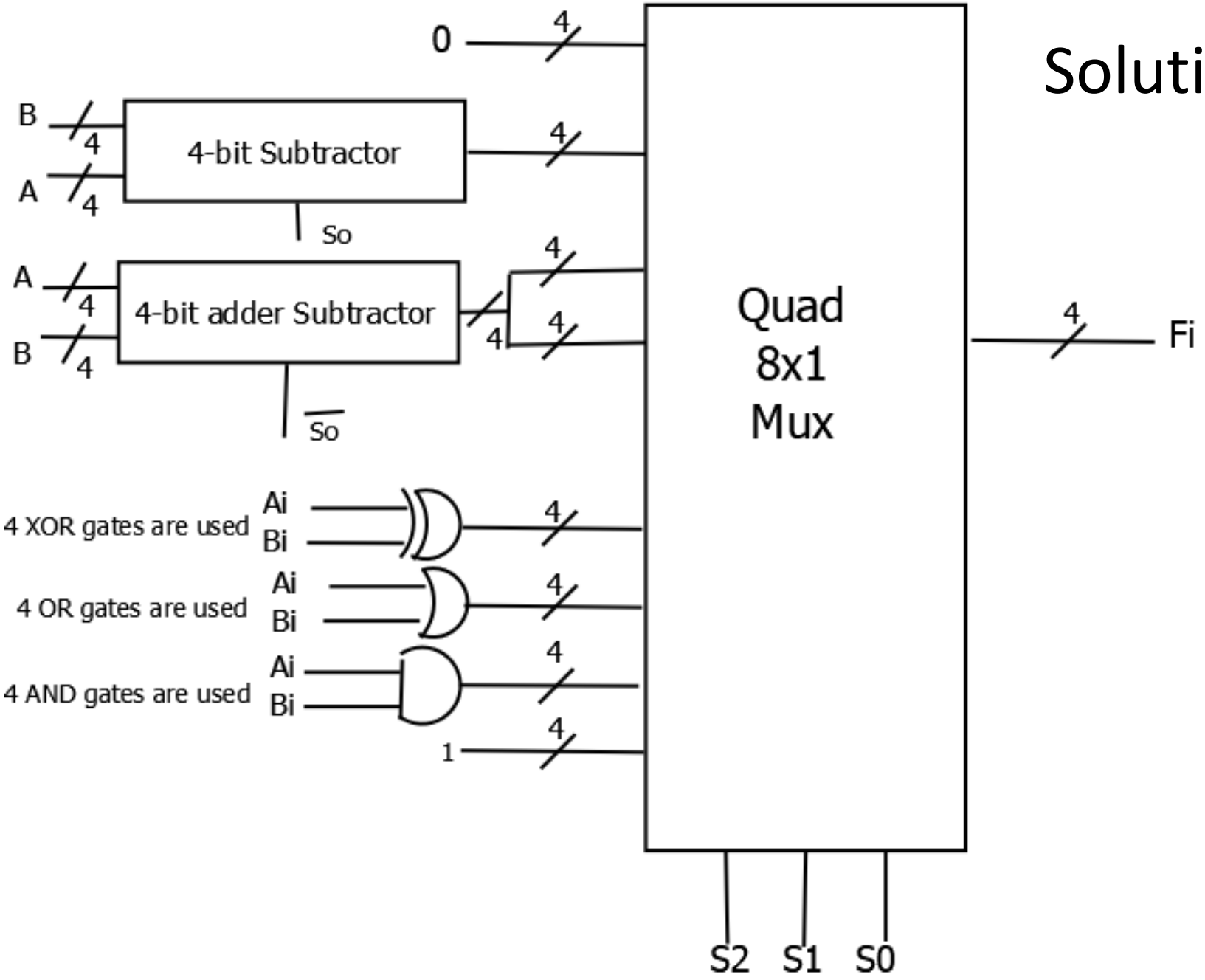
Question 21

Using Quad 8x1 multiplexer to build the functions in this table, where A, B and F are 4-bit I/O.

Inputs			Functions
S_2	S_1	S_0	
0	0	0	F=0000
0	0	1	F=B minus A (B-A)
0	1	0	F=A minus B (A-B)
0	1	1	F=A plus B (A+B)
1	0	0	F=A XOR B
1	0	1	F=A OR B
1	1	0	F=A AND B
1	1	1	F=1111

8 inputs means 3 Selectors
Quad means each input is 4 bits, also the output is 4 bits

Solution 21


0
4
B
4
A
4
4-bit Subtractor
4
So
A
4
4-bit adder Subtractor
B
4
4
4
4
So
Quad
8x1
Mux
4
Fi
4 XOR gates are used
Ai
Bi
4
4 OR gates are used
Ai
Bi
4
4 AND gates are used
Ai
Bi
4
1
4
S2
S1
S0

Revision

Having a Boolean function $F(A, B, C) = \acute{A}C + B\acute{C}$, without simplification, do the following:

- Construct the full truth table, then list the minterms, maxterms
- Draw the logic diagram of F.

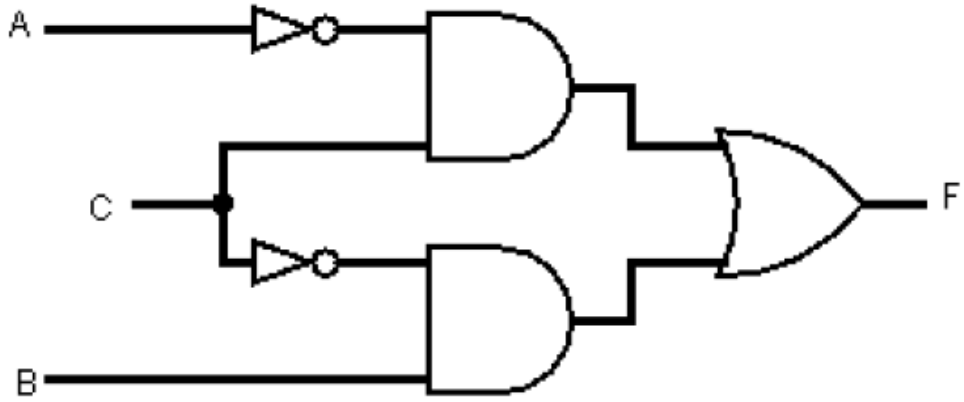
Having a Boolean function $F(A,B,C)=\acute{A}C+B\acute{C}$, without simplification, do the following:

- Construct the full truth table, then list the minterms, maxterms
- Draw the logic diagram of F.

	A	B	C	$\bar{A}$	$\bar{A}C$	$\bar{C}$	$B\bar{C}$	F
0	0	0	0	1	0	1	0	0
1	0	0	1	1	1	0	0	1
2	0	1	0	1	0	1	1	1
3	0	1	1	1	1	0	0	1
4	1	0	0	0	0	1	0	0
5	1	0	1	0	0	0	0	0
6	1	1	0	0	0	1	1	1
7	1	1	1	0	0	0	0	0

$$F(A,B,C)=\sum m(1,2,3,6)$$

$$F(A,B,C)=\Pi_M(0,4,5,7)$$



Having a Boolean function $F(A,B,C)=(\acute{A}+C)(B+\acute{C})$, without simplification, do the following:

- Construct the full truth table, then list the minterms, maxterms
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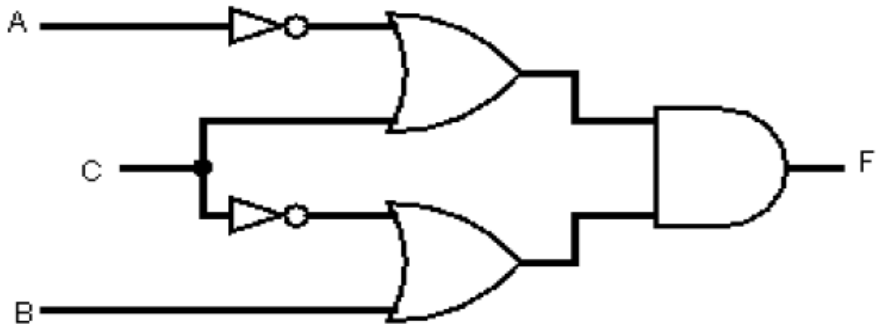
Having a Boolean function $F(A,B,C)=(\acute{A}+C)(B+\acute{C})$, without simplification, do the following:

- Construct the full truth table, then list the minterms, maxterms
- Draw the logic diagram of F.

	A	B	C	$\bar{A}$	$\bar{A}$+C	$\bar{C}$	B + $\bar{C}$	F
0	0	0	0	1	1	1	1	1
1	0	0	1	1	1	0	0	0
2	0	1	0	1	1	1	1	1
3	0	1	1	1	1	0	1	1
4	1	0	0	0	0	1	1	0
5	1	0	1	0	1	0	0	0
6	1	1	0	0	0	1	1	0
7	1	1	1	0	1	0	1	1

$F(A,B,C)=\sum m(0,2,3,7)$

$F(A,B,C)=\Pi_M(1,4,5,6)$

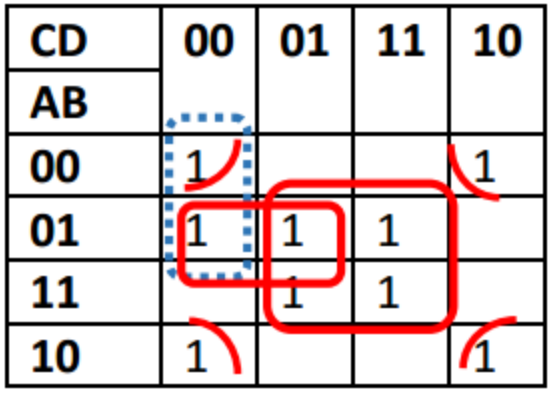


Use a K-map to simplify the following Boolean function as a Sum of Product:

$$F(A, B, C, D) = \pi_M(1, 3, 6, 9, 11, 12, 14)$$

Use a K-map to simplify the following Boolean function as a Sum of Product:

$$F(A, B, C, D) = \pi_M(1, 3, 6, 9, 11, 12, 14)$$



$F = A'BC' + BD + B'D'$

OR $F = A'C'D' + BD + B'D'$

Simplify function in Product-of-Sum form using k-maps:

F(A,B,C) = A'B'C + AB'C' + BC

Simplify function in Product-of-Sum form using k-maps:

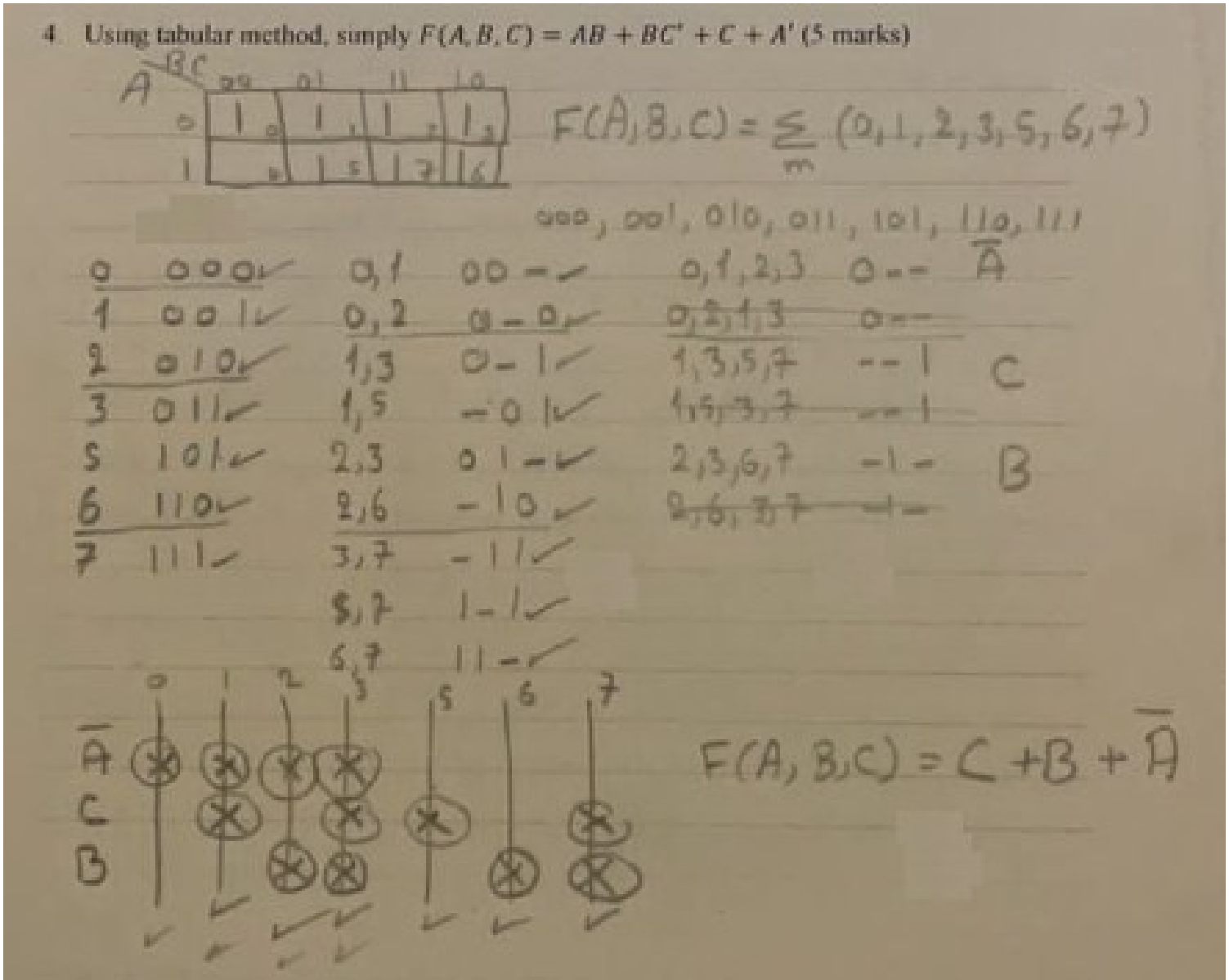
$$F(A,B,C) = A'B'C + AB'C' + BC$$

A/BC	00	01	11	10
0	0	1	1	0
1	1	0	1	0

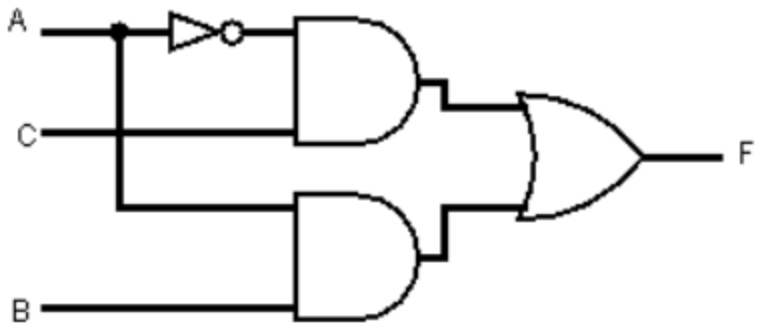
$$F = (A+C)(B'+C)(A'+B+C')$$

Using tabular method, simply $F(A, B, C) = AB + BC' + C + A'$

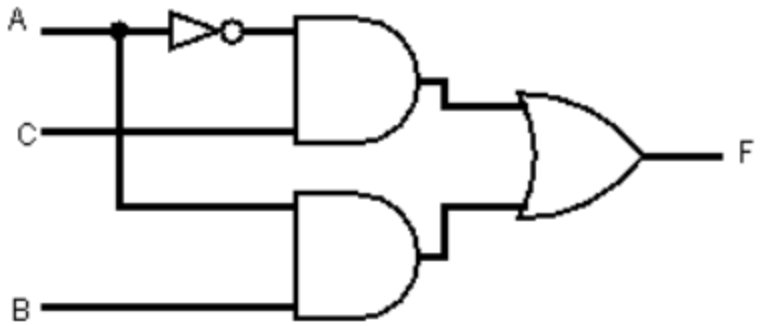
Using tabular method, simply $F(A,B,C) = AB + BC' + C + A'$

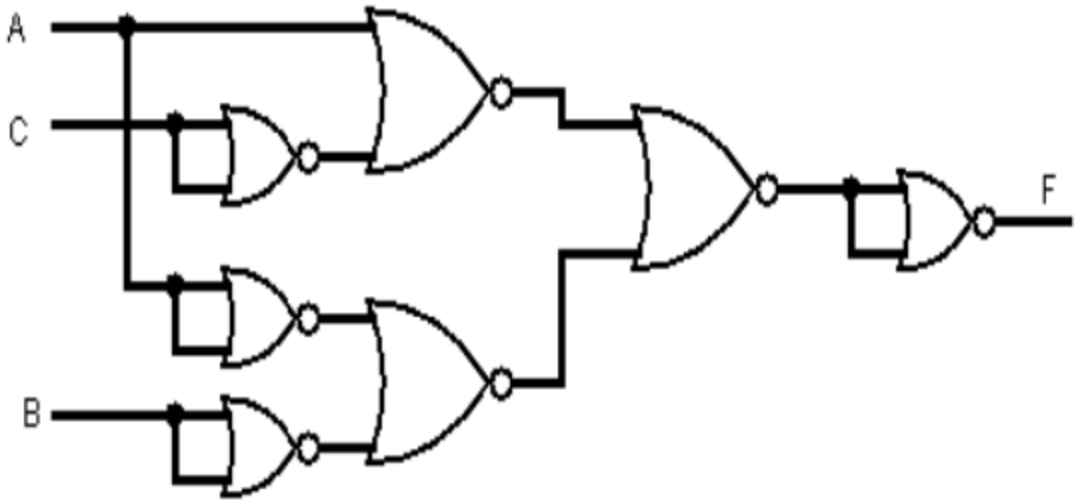


Build the following function using only NORs

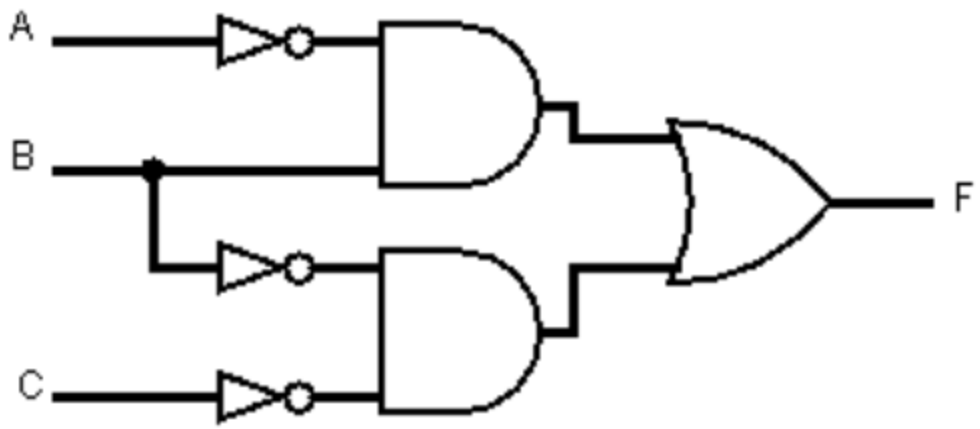


Build the following function using only NORs

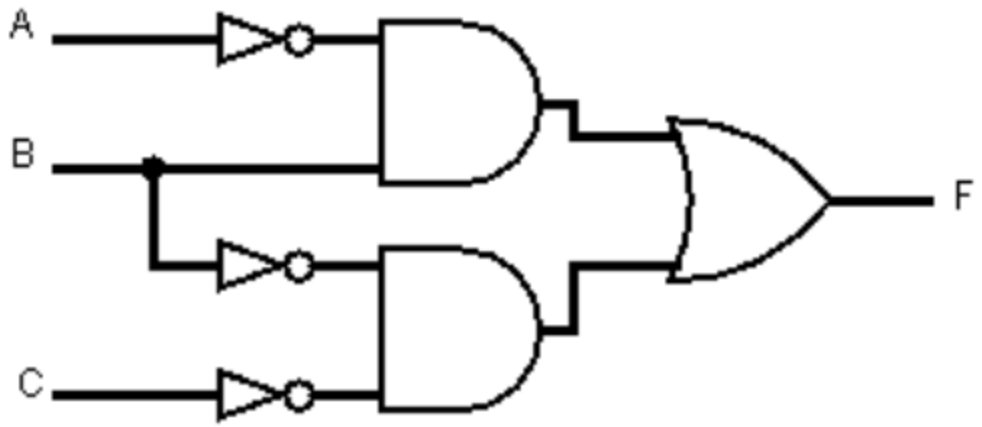


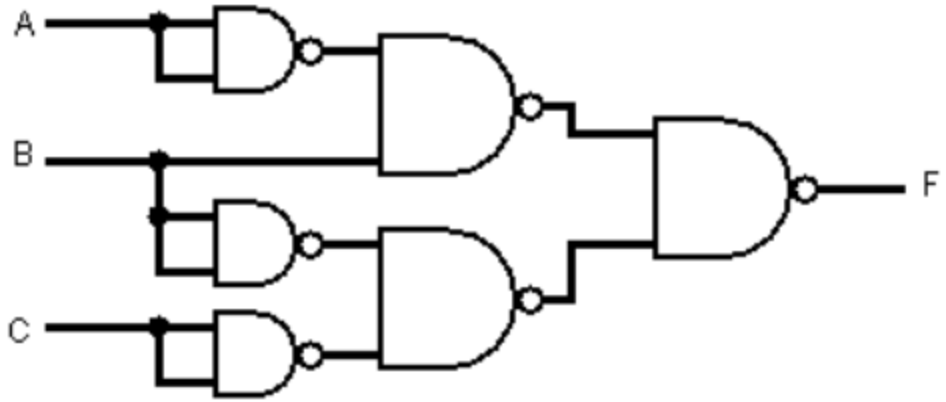


Build the following function using only NANDs



Build the following function using only NANDs





Design a logic circuit
to **translate** a **BCD** code to
a **2421** code.

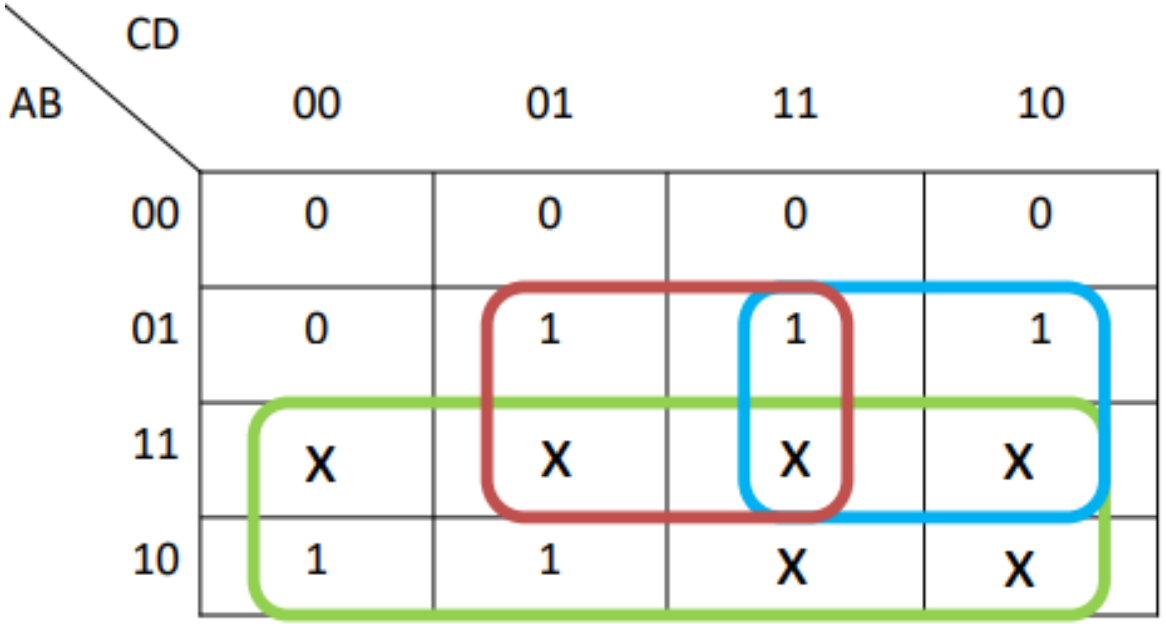
Design a logic circuit to **translate** a **BCD** code to a **2421** code.

- Step 1: how many inputs and how many outputs?
  - four inputs and four outputs
- Step 2: – Obtain the truth table
- Step 3: Obtain simplified Boolean expression for each output
- Step 4: Draw the logic diagram

	Inputs				Outputs			
	BCD				2421			
	A	B	C	D	x	y	z	t
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	1	0	0
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1

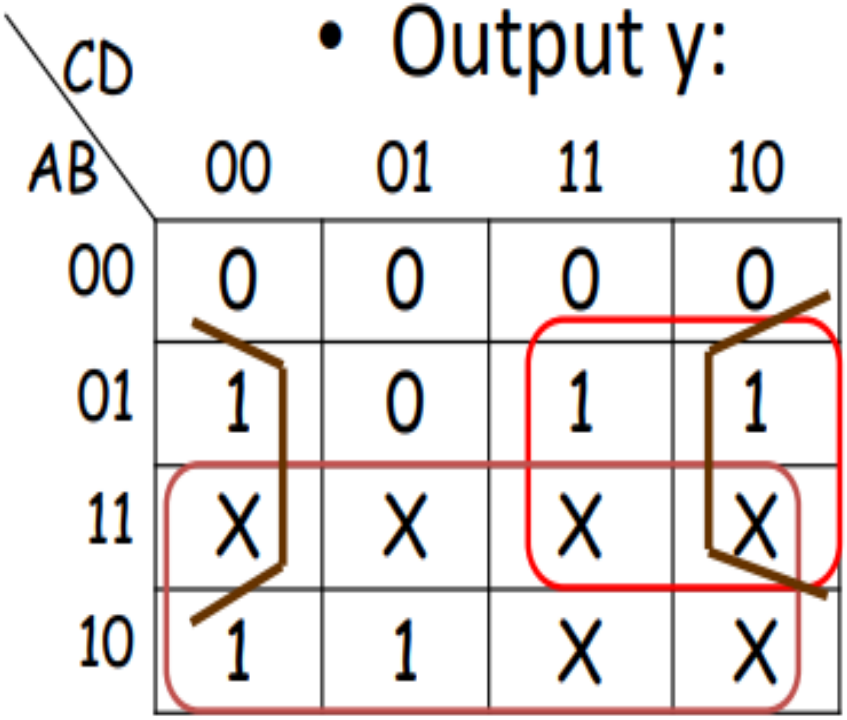
- Step 3: Obtain simplified Boolean expression for each output
- Output x:

A	B	C	D	x
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
The rest				X



$x = BD + BC + A$

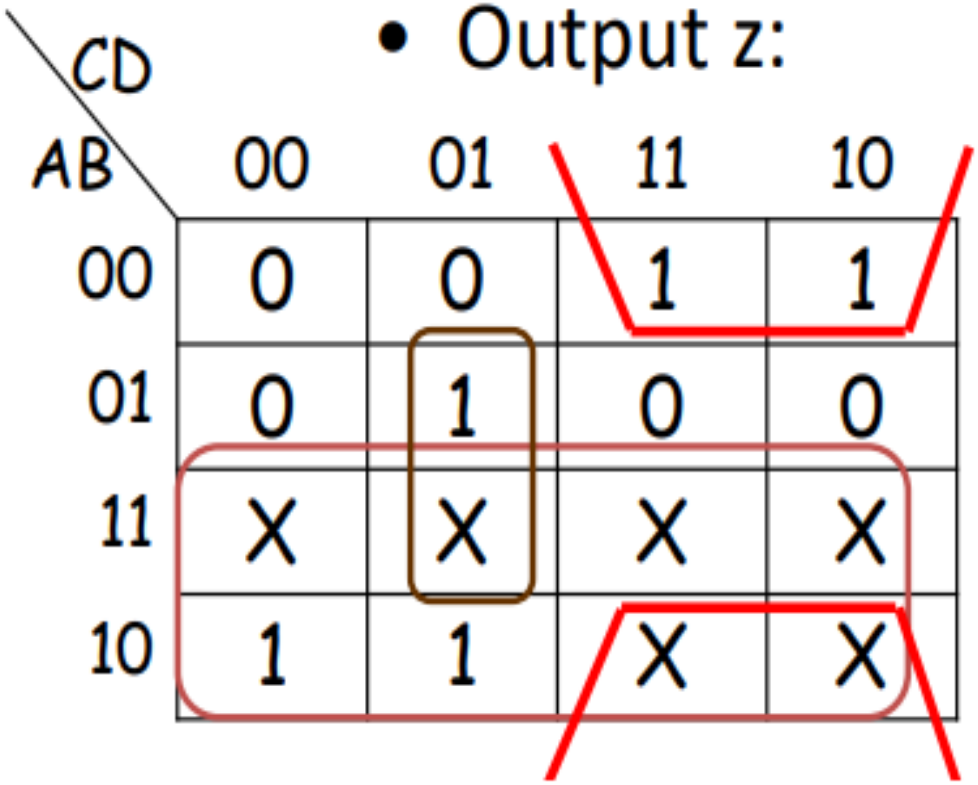
- Output y:



$$y = A + BD' + BC$$

A	B	C	D	y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
The rest				X

- Output z:



$z = A + B'C + BC'D$

A	B	C	D	z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
The rest				X

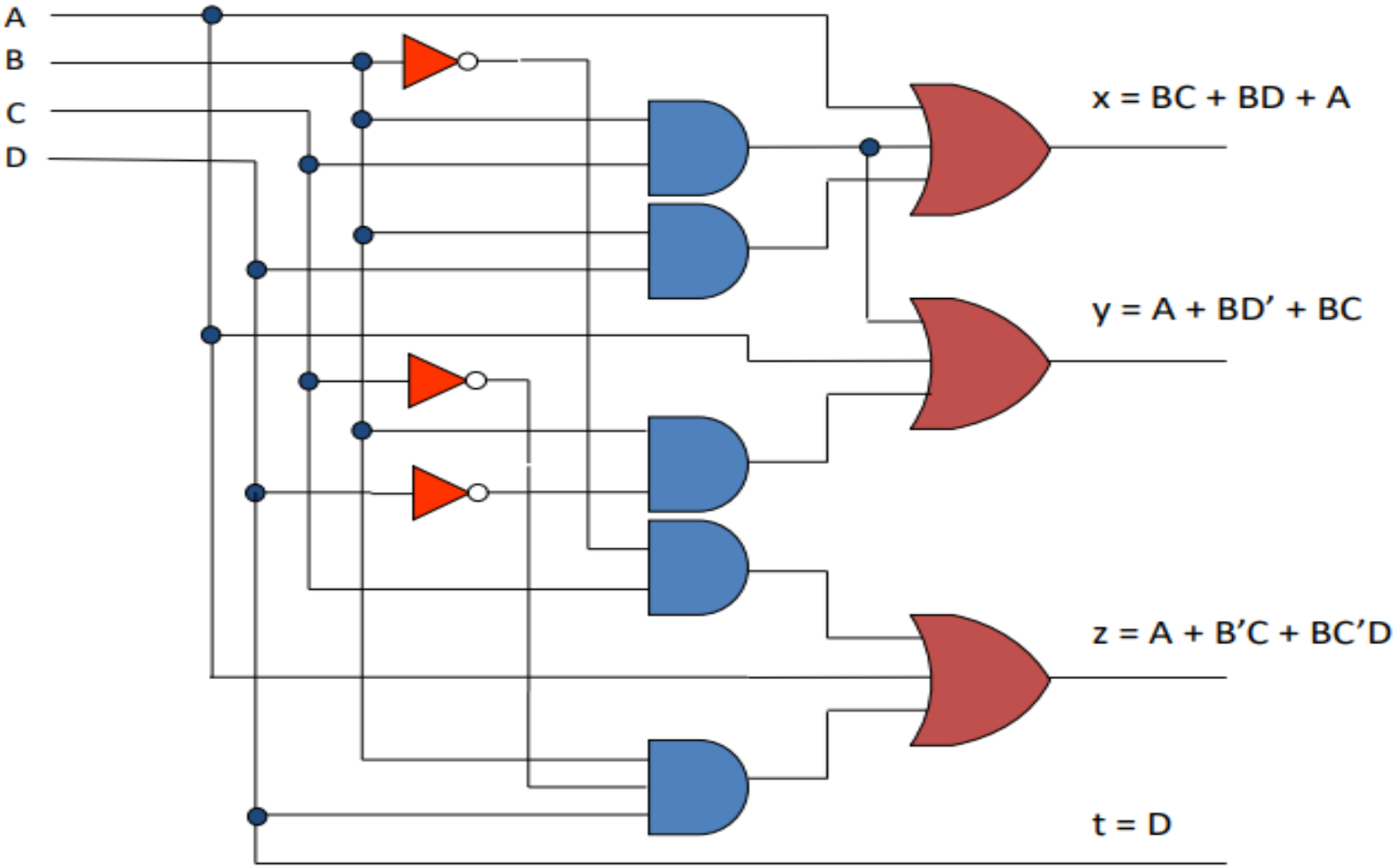
- Output t:

AB \ CD	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	X	X	X	X
10	0	1	X	X

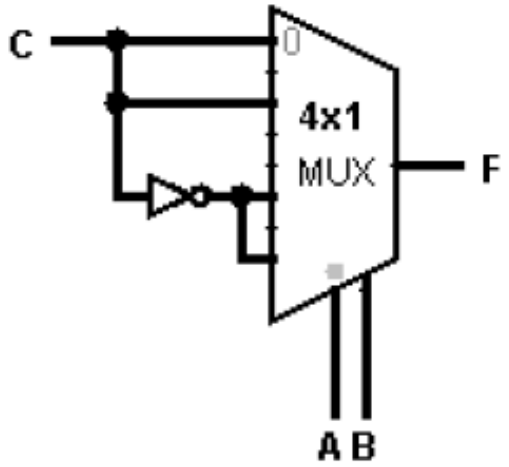
t = D

A	B	C	D	T
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
The rest				X

Logic Diagram

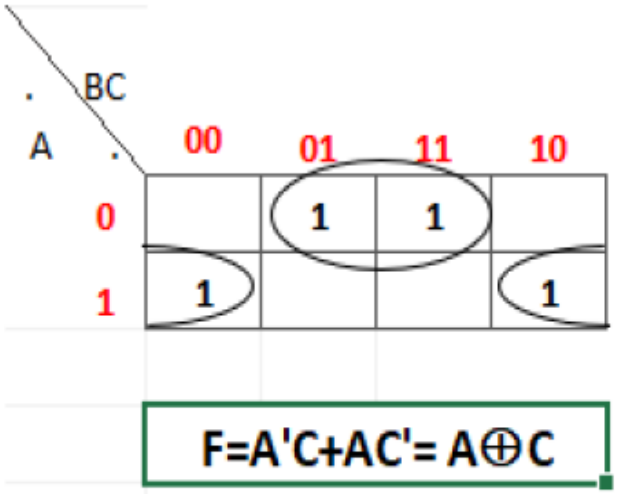


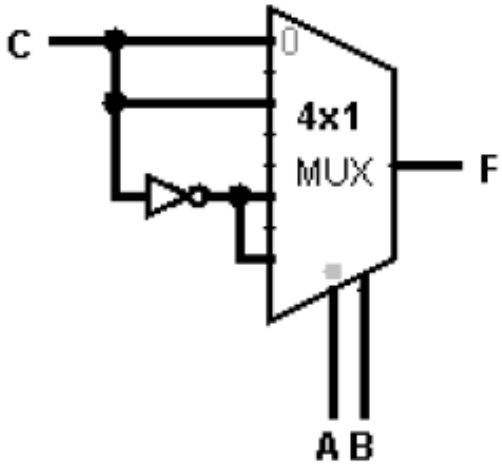
Derive a function F(A,B,C) using a single gate.



Derive a function F(A,B,C) using a single gate.

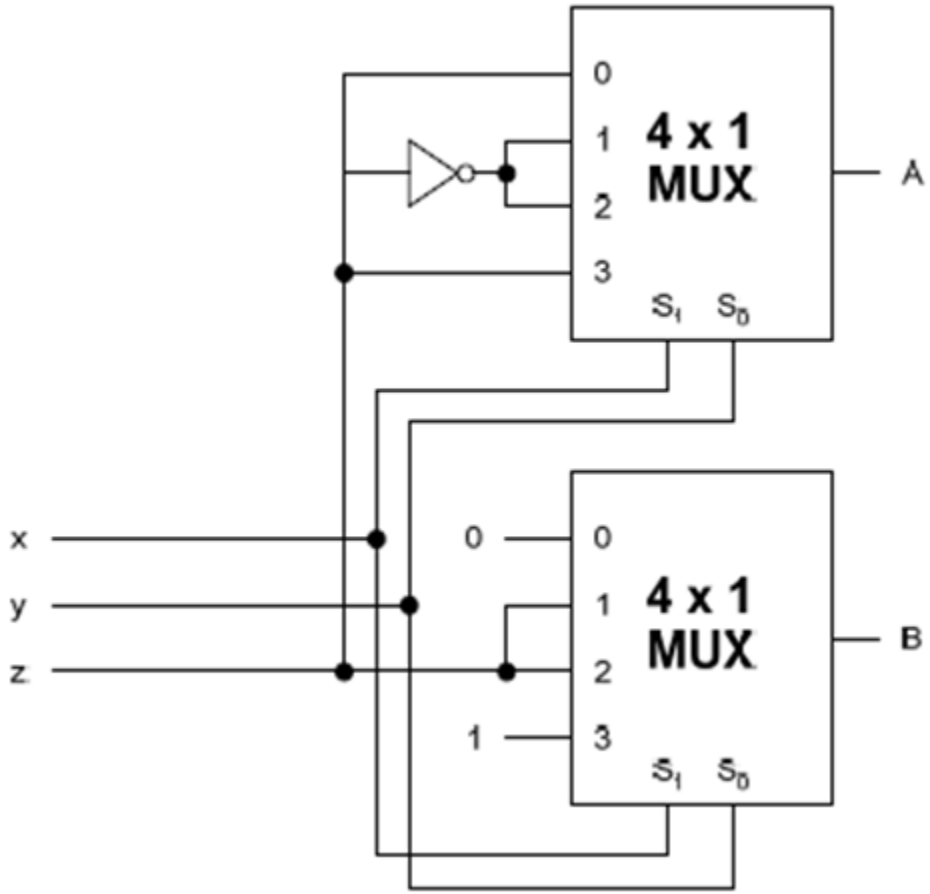
	A	B	C	F	
0	0	0	0	0	F=C
1	0	0	1	1	
2	0	1	0	0	F=C
3	0	1	1	1	
4	1	0	0	1	F=C'
5	1	0	1	0	
6	1	1	0	1	F=C'
7	1	1	1	0	





Determine the outputs of functions (two functions) *A* and *B* as sums of minterms for the following circuit**.**

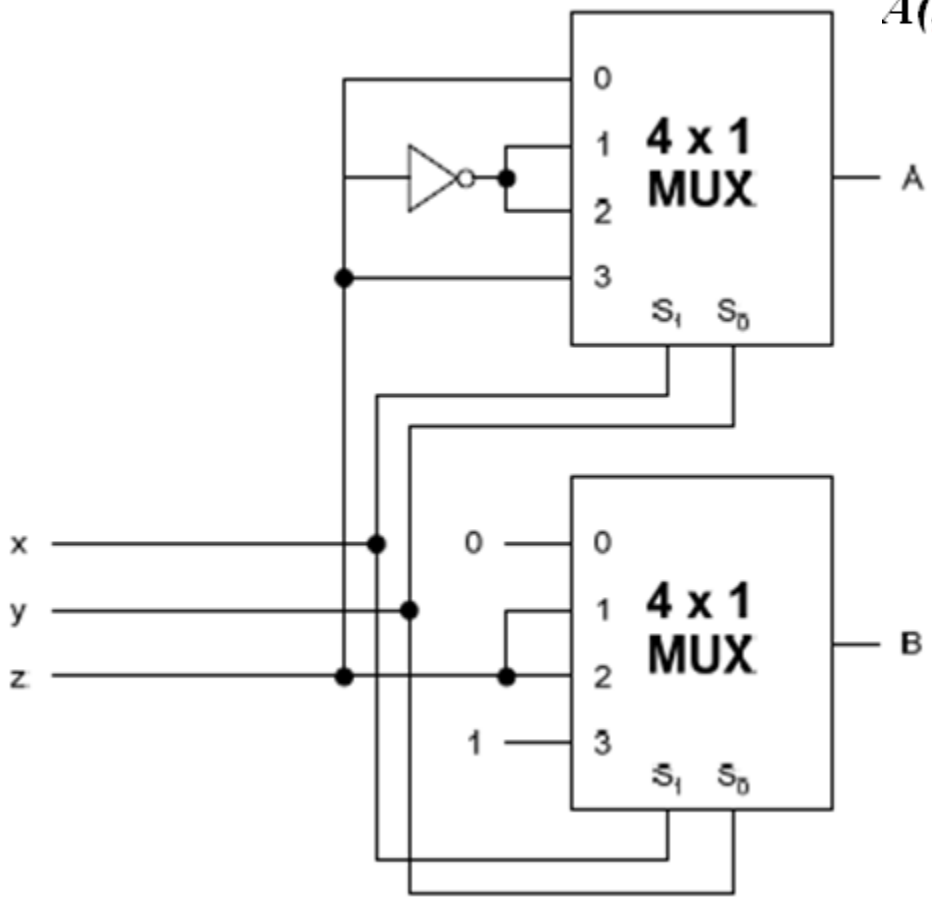
The circuit shown in has a functionality of a commonly used arithmetic component. What does the circuit do and what are other names for A and B?



Determine the outputs of functions (two functions) *A* and *B* as sums of minterms for the following circuit**.**

The circuit shown in has a functionality of a commonly used arithmetic component. What does the circuit do and what are other names for A and B?

$A(x,y,z)=\sum m(1,2,4,7)$ $B(x,y,z)=\sum m(3,5,6,7)$



A is a sum of full adder
B is a carry of full adder

Thanks