Cairo University
Faculty of Computers and Artificial Intelligence
Final Exam (Form A)

Department: Information Technology | **Date: 22 June 2021**
Course Name: Logic Design | **Duration: 2 hours**
Course Code: SIT213/IT212 | **Number of pages: 8**
Instructor(s): Prof. Imane Aly Saroit / Dr. Dina Tarek Mohamed | **Total Marks: 60**

تعليمات هامة

- **حيازة التليفون المحمول مفتوحا داخل لجنة الإمتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضرورى الدخول بالمحمول فيوضع مغلقا فى الحقائب.**
- **لا يسمح بدخول سماعة الأذن أو البلوتوث.**
- **لايسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة والمخالفة تعتبر حالة غش.**

Note: *None* in the answers means that none of the mentioned solutions is right.

A. Using k-map to simplify the following Boolean function as a Product of Sum (PoS):

$$F(A,B,C,D) = (A+B)(C+D)(A+C+D)(\bar{A}+B)(A+B+C+D)(B+D) + d(\bar{B}+\bar{C}+D)$$

1. **Which of the following is a minterm of F?**
   a. 11 b. 12 c. 13 d. 14 e. None

2. **Which of the following is a maxterm of F?**
   a. 5 b. 6 c. 7 d. 8 e. None

3. **How many terms exit in the simplified PoS function?**
   a. 1 b. 2 c. 3 d. 4 e. None

4. **Which of the following is a term in the simplified PoS function?**
   a. $\bar{A}+B$ b. A+B c. $A\bar{B}$ d. $\bar{A}+\bar{B}$ e. None

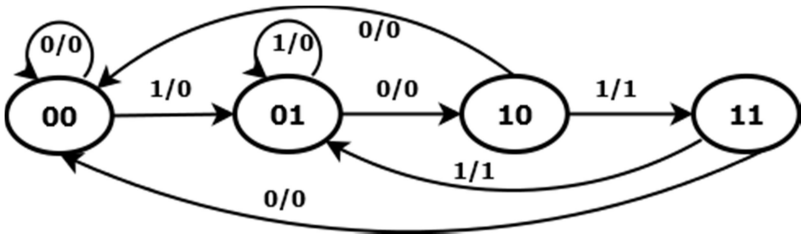
5. **Which of the following is a term in the simplified PoS function?**
   a. B+D b. B+C c. A+D d. D+C e. None

6. **How many AND gates are needed to build the simplified PoS function?**
   a. 0 b. 1 c. 2 d. 3 e. None

7. **How many OR gates are needed to build the simplified PoS function?**
   a. 0 b. 1 c. 2 d. 3 e. None

8. **If the propagation delay of NOT, AND, OR gates are 3, 10 and 10 nsec respectively. What is the propagation delay of the simplified PoS function?**
   a. 20 nsec b. 23 nsec c. 10 nsec d. 13 nsec e. None

B. **For the shown state diagram of a sequential circuit with an input X, two JK flip flops A and B and an output Y.**



9. **What is the next state for a present state 00 & an input of 1?**
   a. 00 **b. 01** **c. 10** **d. 11** **e. None**

10. **What is the next state for a present state 01 & an input of 1?**
    a. 00 **b. 01** **c. 10** **d. 11** **e. None**

11. **What is the next state for a present state 10 & an input of 0?**
    a. 00 **b. 01** **c. 10** **d. 11** **e. None**

12. **What is the next state for a present state 11 & an input of 1?**
    a. 00 **b. 01** **c. 10** **d. 11** **e. None**

	Present State		Input
	A	B	X
13.	0	0	0
14.	0	1	0
15.	0	1	1
16.	1	0	0
17.	1	0	1
18.	1	1	1

This table represents a part of the state table of this circuit. What is the value of $J_A K_A - J_B K_B$ for each of the following stated present states – input?

13. **a. 0 X – 0 X** **b. 0 X – X 0** **c. 0 X – 1 X** **d. 0 X – X 1** **e. None**
14. **a. 1 X – 0 X** **b. 1 X – X 0** **c. 1 X – 1 X** **d. 1 X – X 1** **e. None**
15. **a. X 1 – 0 X** **b. X 1 – X 0** **c. X 1 – 1 X** **d. X 1 – X 1** **e. None**
16. **a. X 1 – 0 X** **b. X 1 – X 0** **c. X 1 – 1 X** **d. X 1 – X 1** **e. None**
17. **a. X 0 – 0 X** **b. X 0 – X 0** **c. X 0 – 1 X** **d. X 0 – X 1** **e. None**
18. **a. X 1 – 0 X** **b. X 1 – X 0** **c. X 1 – 1 X** **d. X 1 – X 1** **e. None**

19. **For this circuit, what is the simplified equation of J_A?**
    a. BX **b. $B\overline{X}$** **c. ABX** **d. $AB\overline{X}$** **e. None**

20. **For this circuit, what is the simplified equation of K_A?**
    a. $B + \overline{X}$ **b. $B + X$** **c. $AB + AX$** **d. $AB + B\overline{X}$** **e. None**

21. **For this circuit, what is the simplified equation of J_B?**
    a. $\overline{B}X$ **b. $B\overline{X}$** **c. X** **d. $\overline{X}$** **e. None**

22. **For this circuit, what is the simplified equation of K_B?**
    a. $\overline{B}X$ **b. $B\overline{X}$** **c. X** **d. $\overline{X}$** **e. None**

23. **For this circuit, what is the simplified equation of Y?**
    a. $A\overline{B}\,\overline{X}$ **b. AX** **c. $A\overline{B}$** **d. ABX** **e. None**

24. **How many inverters are used to build this sequential circuit?**
    a. 0 **b. 1** **c. 2** **d. 3**

C. **For the following state table, reduce the number of states, always start with the states in the upper rows, and in case of matching always keep the state in the upper rows.**

Current State	Next State		Output
	X=0	X=1	
A	A	B	1
B	C	E	0
C	F	G	1
D	C	I	0
E	I	G	1
F	H	I	1
G	C	B	0
H	F	G	1
I	C	E	0

25. **What is the removed state after the first reduction?**
a. F **b. G** **c. H** **d. I** **e. None**

26. **What is the removed state after the second reduction?**
a. F **b. G** **c. H** **d. I** **e. None**

27. **What is the removed state after the third reduction?**
a. F **b. G** **c. H** **d. I** **e. None**

28. **What is the removed state after the fourth reduction?**
a. F **b. G** **c. H** **d. I** **e. None**

29. **What is the number of flip flops needed to build the circuit before → after the reduction?**
a. 3→3 **b. 4→3** **c. 4→2** **d. 4→4** **e. None**

D. **Using one 4-bit adder and one full-adder to design a circuit that implements the function Y=25X+8, where X is 4-bit binary number. Note that doubling a binary number leads to left shifting this number and adding 0 to the left significant bit, i.e., if X= $X_3X_2X_1X_0$, 2X= $X_3X_2X_1X_0$ 0 (e.g., if X= 1011 then 2X=10110). Note C_H is the full-adder carry and C_P is the carry resulting from adding previous bits in the 4-bit adder.**

30. **What many bits is Y?**
a. 5 **b. 6** **c. 7** **d. 8** **e. None**

31. **What are the inputs of the full adder?**
a. X_0, X_3, 1 **b. X_1, X_2, 0** **c. X_0, X_1, 1** **d. X_2, X_3, 0** **e. None**

32. **What are the inputs of the least significant bit of the used 4-bit adders?**
a. X_0, X_3, 1 **b. X_0, X_1, C_H** **c. X_1, X_3, 0** **d. X_2, X_3, C_H** **e. None**

33. **What are the inputs of the second bit (from the right side) of the used 4-bit adders?**
a. X_0, X_3, C_P **b. X_0, X_1, X_3** **c. X_1, X_2, X_3** **d. X_1, X_2, C_P** **e. None**

34. **What are the inputs of the third bit (from the right side) of the used 4-bit adders?**
a. X_0, X_1, X_2 **b. X_0, X_3, 0** **c. X_1, X_2, C_P** **d. X_2, X_3, C_H** **e. None**

35. **What are the inputs of the most significant bit of the used 4-bit adders?**
a. X_3, 1, C_P **b. X_1, X_2, C_P** **c. X_3, 0, C_P** **d. X_0, X_1, C_P** **e. None**

36. **What is the value of Y3?**
a. X_0 **b. X_1** **c. X_2** **d. Result of the full adder** **e. None**

37. **What is the value of Y5?**
a. X_1 **b. X_2** **c. X_3** **d. Result of the full adder** **e. None**

E. **Having an n-bit register that performs the operations in this table:**

Register Operations
No change
Shift right
Shift left
Parallel load
Clear
Rotate right
Rotate left
Complement

38. **What is the size of the multiplexer needed to be used at each bit?**
a. 2x1 **b. 4x1** **c. 8x1**
d. 16x1 **e. None**

39. **What is the input at of the flip-flop middle stage i that performs the shift right operation?**
a. $Q_i(t)$ **b. $Q_{i+1}(t)$** **c. $Q_{i-1}(t)$**
d. Li **e. None**

40. **What is the input at of the flip-flop middle stage i that performs the rotate left operation?**
a. $Q_i(t)$ **b. $Q_{i+1}(t)$** **c. $Q_{i-1}(t)$** **d. Li** **e. None**

41. **What is the input at of the flip-flop of the most significant bit that performs the rotate right operation?**
a. $Q_0(t)$ **b. $Q_i(t)$** **c. Li** **d. $Q_{n-1}(t)$** **e. None**

42. **What is the input at of the flip-flop of the least significant bit that performs the clear operation?**
a. $Q_0(t)$ **b. $Q_i(t)$** **c. Li** **d. $Q_{n-1}(t)$** **e. None**

F. **Adding the two BCD numbers 0111 0111 and 0101 1000, where the first BCD code (from the left side) in each of the two numbers is represented by A1 and A2, the second is represented by B1 and B2, meaning that A1= 0111, A2= 0101 and B1=0111 and B2=1000:**

43. **What is the initial result of adding A1 and A2?**
a. 0110 **b. 1100** **0001** **d. 1101** **e. None**

44. **What is the initial result of adding B1 and B2?**
a. 1010 **b. 1011** **c. 1111** **d. 0111** **e. None**

45. **Which of the initial addition needs the correction step?**
a. Only the addition of A1 & A2. **b. Only the addition of B1 & B2.**
c. Both the addition of A1 & A2 and that of B1&B2. **d. None**

46. **What is the value needed to be added in the correction step (if needed)?**
a. 0111 **b. 0011** **c. 0110** **d. 1** **e. None**

47. **What is the final result of adding B1 and B2 (after the correction step if needed)?**
a. 0010 **b. 0011** **c. 0100** **d. 0101** **e. None**

48. **What is the first resulting BCD code from the left?**
a. 0001 **b. 0010** **c. 0011** **d. 0100** **e. None**

G. Using various codes, answer the following:

49. How is $(0101.1001)_{5421}$ represented in decimal?
a. 22.41 b. 22.9 c. 5.9 d. 5.6 e. None

50. How is $(0011.1001)_{BCD}$ represented in Excess-3?
a. 3.9 b. 0110.1100 c. 6.12 d. 0011.1100 e. None

51. What is the 9's Complement of $(0100.0110)_{BCD}$?
a. 1011.1001 b. 1011.1010 c. 0101.0011 d. 0101.0100 e. None

52. What is the code defined as an ordering of the binary number system such that each incremental value can only differ by one bit?
a. BCD b. Excess-3 c. Gray d. ASCII e. None

H. Using tabular method to simplify the following function as SoP: $F(A,B,C)=\sum m(1,2,4,5,7)+d(6)$, then answer the following:

53. How many groups are initially formed?
a. 1 b. 2 c. 3 d. 4 e. None

54. Which of the following numbers form the first group?
a. 1,2,4,5 b. 1,2,4 c. 1,2,4,6 d. 5,6,7 e. None

55. Which of the following numbers form the second group?
a. 4,5,6 b. 4,5 c. 4,6 d. 5,6 e. None

56. Which of the following combined terms is formed in the first iteration?
a. 1,2 b. 4,7 c. 5,6 d. 3,7 e. None

57. Which of the following combined terms is formed in the first iteration?
a. 1,4 b. 1,6 c. 2,6 d. 1,7 e. None

58. Which of the following combined terms is formed in the first iteration?
a. 2,7 b. 3,7 c. 1,4 d. 4,5 e. None

59. Which of the following combined terms is formed in the second iteration?
a. 4,5,6,7 b. 1,5,2,6 c. 1,2,4,5 d. 5,7,6,2 e. None

60. Using simple gates (AND, OR, NOT), which of the following is a term in the simplified function?
a. $\bar{A}C$ b. BC c. $B\bar{C}$ d. AB e. None

61. Using simple gates (AND, OR, NOT), how many inverters are needed to build the simplified function?
a. 0 b. 1 c. 2 d. 3 e. None

62. Without using any inverters, which of the following is a term in the simplified function?
a. BC b. $B+C$ c. $B \oplus C$ d. AB e. None

I. **Design a combinational circuit that builds the following with a four bits number ABCD and two outputs XY. If ABCD <5, the output(s) counts the number of ones, if ABCD >7, the output(s) counts the number of zeros. Inputs from 5 to 7 cannot occur.**

The following table represents a part of the truth table of this circuit. What is the value of the output(s) in case of the following inputs ABCD?

	Inputs								
	A	B	C	D					
63.	0	0	1	0	a. 00	b. 01	c. 10	d. 11	e. None
64.	0	0	1	1	a. 00	b. 01	c. 10	d. 11	e. None
65.	0	1	0	0	a. 00	b. 01	c. 10	d. 11	e. None
66.	0	1	1	0	a. 00	b. 01	c. 10	d. 11	e. None
67.	1	0	1	0	a. 00	b. 01	c. 10	d. 11	e. None
68.	1	1	0	1	a. 00	b. 01	c. 10	d. 11	e. None
69.	1	1	1	1	a. 00	b. 01	c. 10	d. 11	e. None

70. Which of the following is a term in the simplified function X as Product of Sum (PoS)?
a. $A+B+C$ **b.** $\overline{A}+\overline{C}+\overline{D}$ **c.** $\overline{A}+B+C$ **d.** $A+B+\overline{C}$ **e. None**

71. Which of the following is not a term in the simplified function X as Product of Sum (PoS)?
a. $A+C$ **b.** $\overline{B}+\overline{C}$ **c.** $\overline{B}+\overline{D}$ **d.** $A+\overline{B}$ **e. None**

72. How many inverters are needed to build X as Product of Sum (PoS)?
a. 1 **b. 2** **c. 3** **d. 4** **e. None**

73. How terms are there in the simplified function X as Product of Sum (PoS)?
a. 3 **b. 4** **c. 5** **d. 6** **e. None**

74. What is the optimal size of a decoder needed to build X?
a. 2x4 **b. 3x8** **c. 4x16** **d. 5x32** **e. None**

75. Which of the following is a term in the simplified function Y as Sum of Product (SoP)?
a. $ABCD$ **b.** $\overline{A}B\overline{C}$ **c.** $\overline{A}\,\overline{C}\,D$ **d.** $\overline{A}B\overline{D}$ **e. None**

76. Which of the following is a term in the simplified function Y as Sum of Product (SoP)?
a. $\overline{A}B$ **b.** $AB\overline{C}$ **c.** $\overline{A}D$ **d.** $A\overline{B}C$ **e. None**

77. How terms are there in the simplified function Y as Sum of Product (SoP)?
a. 4 **b. 5** **c. 6** **d. 7** **e. None**

78. Which of the following gate can be used to build Y in the simplest way?
a. Decoder **b. Multiplexer** **c. XOR** **d. XNOR** **e. None**

J. **Answer the following:**

79. Which of the following can used alone to build a 4x16 decoder?

a. Two 3x8 decoders **b. Two 3x8 decoders and a demultiplexer**

c. Four 2x4 decoders **d. Five 2x4 decoders** **e. None**

80. To build a circuit with four inputs and three different outputs using a decoder, you need:

a. One 4x16 decoder and one OR gate **b. One 4x16 decoder and three OR gates**

c. One 3x8 decoder and one OR gate **d. One 3x8 decoder and three OR gates** **e. None**

81. Having a number of four digits A,B,C,D and an output F. If (ABCD is odd) F=AB else F=CD. Beside the simple gates, what is the smallest multiplexer needed to build F?

a. 2x1 **b. 4x1** **c. 8x1** **d. 16x1** **e. None**

82. In general a $1x2^n$ demultiplexer is equivalent to $nx2^n$ decoder with enable, where the input of the demultiplexer is equivalent to which of the following in the decoder:

a. Inputs **b. Outputs** **c. Enable** **d. None**

83. The following function $F = \bar{A}\,\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$, represents a:

a. Decoder **b. Encoder** **c. Multiplexer** **d. Demultiplexer** **e. None**

84. To build a BCD to Excess-3 code converter, you need:

a. A decoder and an encoder **b. A multiplexer and a demultiplexer**

c. A decoder and a demultiplexer **d. A multiplexer and an encoder** **e. None**

K. **Having the following function: $F(A,B,C,D)=\sum_m(3,4,8,10)$**

85. What is the optimal multiplexer size used to build the above function?

a. 32x1 **b. 16x1** **c. 8x1** **d. 4x1** **e. None**

86. Using AB as selectors, what is the size of multiplexer used to build the above function?

a. 32x1 **b. 16x1** **c. 8x1** **d. 4x1** **e. None**

87. Using AB as selectors, what is the input to the 1^{st} input to the multiplexer?

a. CD **b. C+D** **c. 0** **d. 1** **e. None**

88. Using AB as selectors, what is the input to the 2^{nd} input to the multiplexer?

a. CD **b. C+D** **c. 0** **d. 1** **e. None**

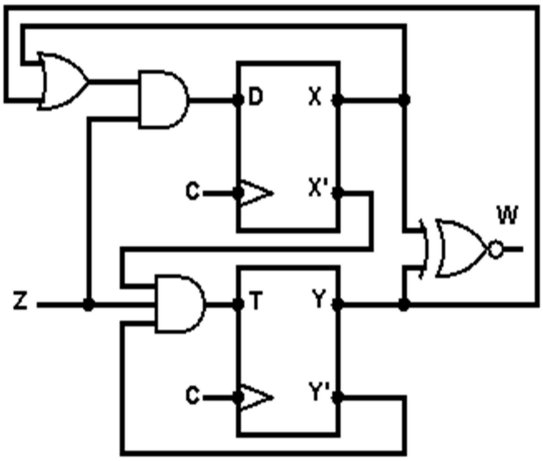
89. Using AB as selectors, what is the input to the 3^{rd} input to the multiplexer?

a. 1 **b. C+D** **c. 0** **d. $\overline{C \oplus D}$** **e. None**

90. Using AB as selectors, what is the input to the last input of the multiplexer?

a. CD **b. C+D** **c. 0** **d. 1** **e. None**

L. The shown sequential circuit has an input Z, two flip flops X and Y and an output W.



91. For a D flip–flop, what is the value of Q(t+1)?

a. 0 **b. 1** **c. Q(t)**

d. $\overline{Q(t)}$ **e. None**

92. For a T flip–flop, if T=1, what is the value of Q(t+1)?

a. 0 **b. 1** **c. Q(t)**

d. $\overline{Q(t)}$ **e. None**

93. For a T flip–flop, if T=0, what is the value of Q(t+1)?

a. 0 **b. 1** **c. Q(t)**

d. $\overline{Q(t)}$ **e. None**

94. For this circuit, what is the equation of T_Y?

a. X Y Z **b. $\overline{X}$ Y Z** **c. $\overline{X}\,\overline{Y}$ Z** **d. $\overline{X}\,\overline{Y}\,\overline{Z}$** **e. None**

95. For this circuit, what is the equation of W?

a. XY **b. X + Y** **c. $\overline{X \oplus Y}$** **d. X $\oplus$ Y** **e. None**

	Present State		Input
	X	Y	Z
96.	0	0	0
97.	0	1	0
98.	1	0	0
99.	1	1	0
100.	1	1	1

This table represents a part of the state table of this circuit. What are the flip-flops next state–output (XY–W) for each of the stated flip flops's present state and input (XYZ)?

96. a. 00–0 **b. 00–1** **c. 01–0** **d. 01–1** **e. None**

97. a. 00–0 **b. 00–1** **c. 01–0** **d. 01–1** **e. None**

98. a. 00–0 **b. 00–1** **c. 01–0** **d. 01–1** **e. None**

99. a. 00–0 **b. 00–1** **c. 01–0** **d. 01–1** **e. None**

100. a. 10–0 **b. 10–1** **c. 11–1** **d. 11–0** **e. None**

Good Luck
Prof. Imane Aly Saroit Ismail
Dr. Dina Tarek