Sheet 2 – Logic gates

Question 1:

c)

A	B	C	F	$\overline{F}$
0	0	0	1	**0**
0	0	1	1	**0**
0	1	0	1	**0**
0	1	1	0	**1**
1	0	0	0	**1**
1	0	1	1	**0**
1	1	0	1	**0**
1	1	1	0	**1**

List of Minterms of F: (the decimal no corresponding to 1's)

F(A,B,C) = m0,m1,m2,m5,m6.

List of Minterms of F':

F'(A,B,C) = ,m3,m4,m7.

List of Maxterms of F: (the decimal no corresponding to 0's)

F(A,B,C) =M3,M4,M7.

List of Maxterms of F':

F'(A,B,C)=M0,M1,M2,M5,M6.

Sum of Product sop F (1's -.-.-.-+-.-.-.-+-.-.-.- , (0->x',1->x)):

F(A,B,C)=A'B'C'+A'B'C+A'BC'+AB'C+ABC'

Product of Sum pos F(0's ((-+-).(-+-)),(1->x',0->x)):

F(A,B,C)=(A+B'+C').(A'+B+C).(A'+B'+C')

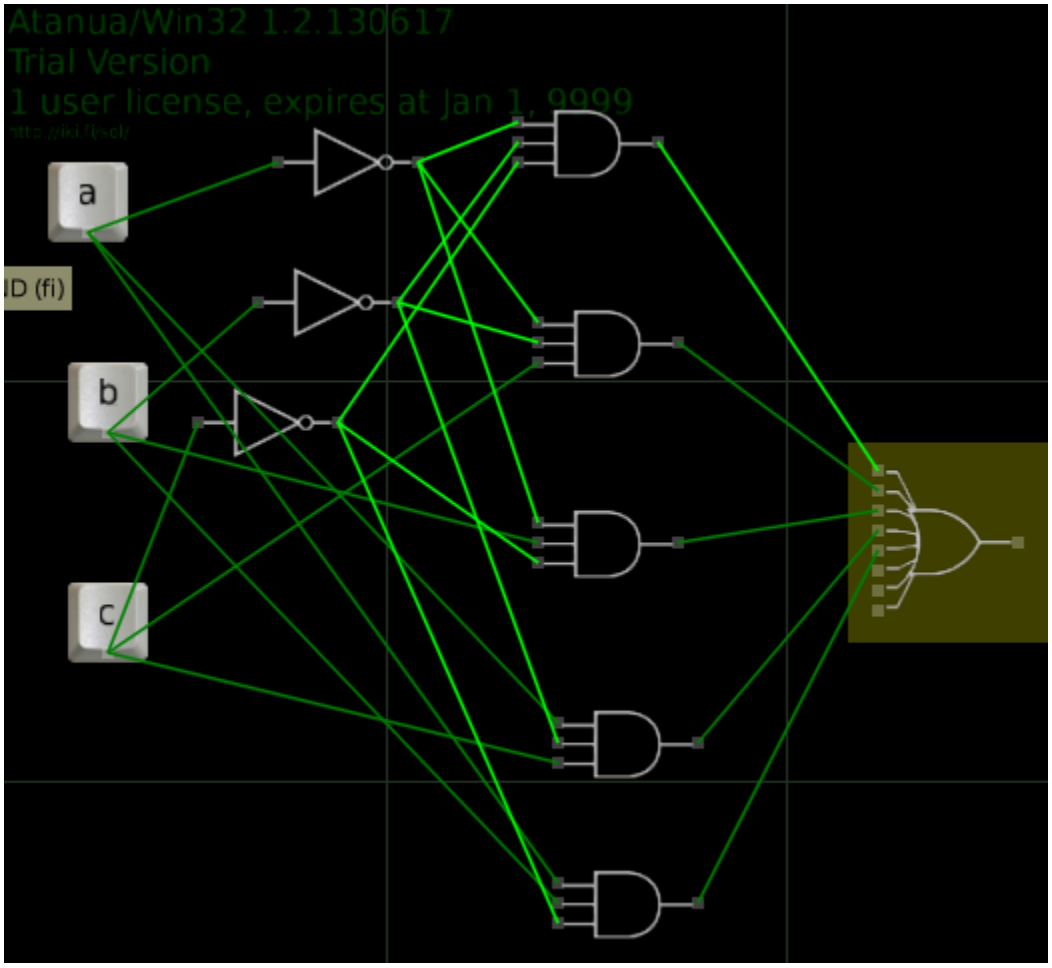
Sum of Product sop F' (1's -.-.-.-+-.-.-.-+-.-.-.- , (0->x',1->x)):

F'(A,B,C)=A'BC+AB'C'+ABC

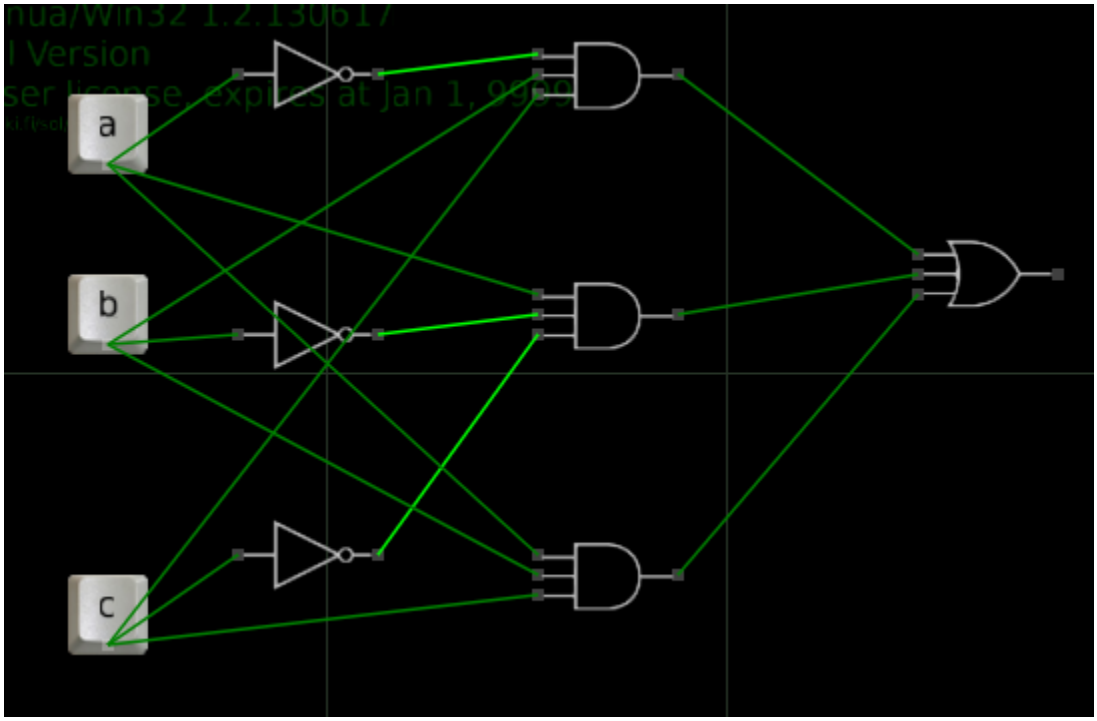
Product of Sum pos F’(0’s ((-+-).(-+-)),(1->x’,0->x)):

F’(A,B,C)=(A+B+C).(A+B+C’).(A+B’+C)+(A’+B+C’).(A’+B’+C)

Logic Diagram of F(sop):



Logic Diagram of F’(sop):



Question 2:

B:F(X,Y,Z)=XY+YZ+XY'Z

X	Y	Z	XY	YZ	Y'	XY'Z	F
0	0	0	0	0	1	0	0
0	0	1	0	0	1	0	0
0	1	0	0	0	0	0	0
0	1	1	0	1	0	0	1
1	0	0	0	0	1	0	0
1	0	1	0	0	1	1	1
1	1	0	1	0	0	0	1
1	1	1	1	1	0	0	1

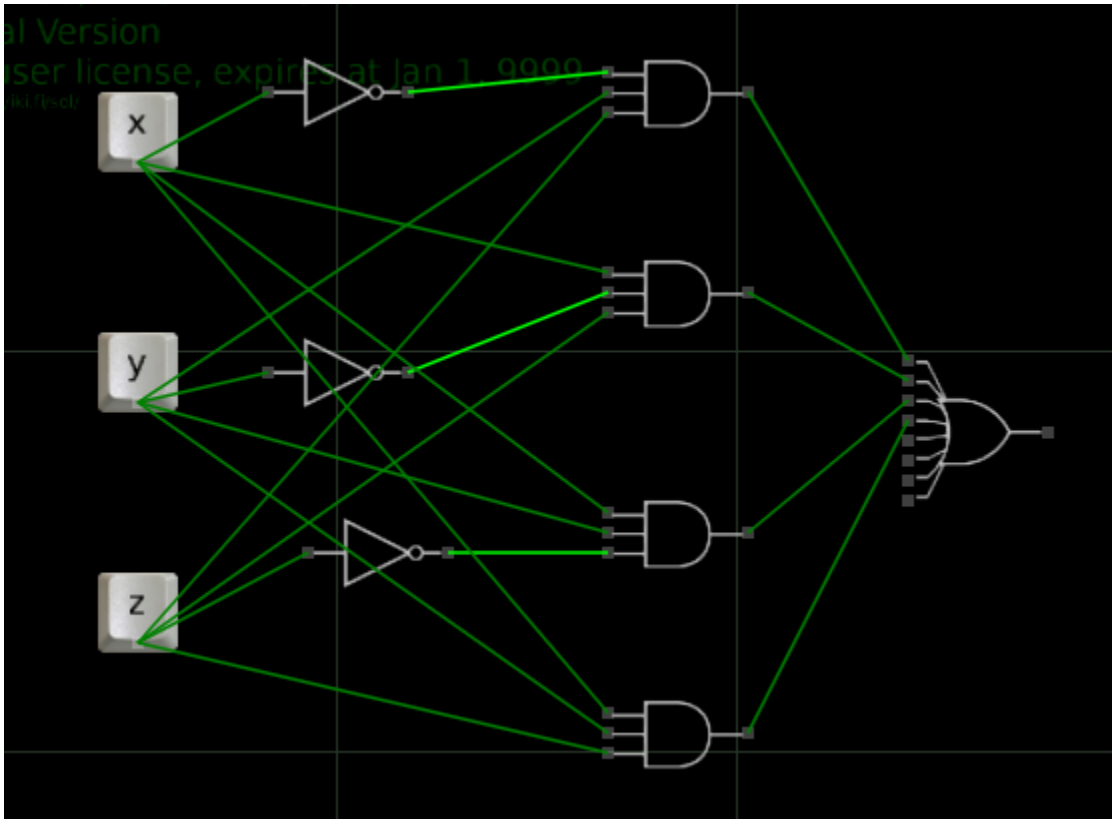
Minterms :m3,m5,m6,m7

SOP : X'.Y.Z+X.Y'.Z+X.Y.Z'+X.Y.Z

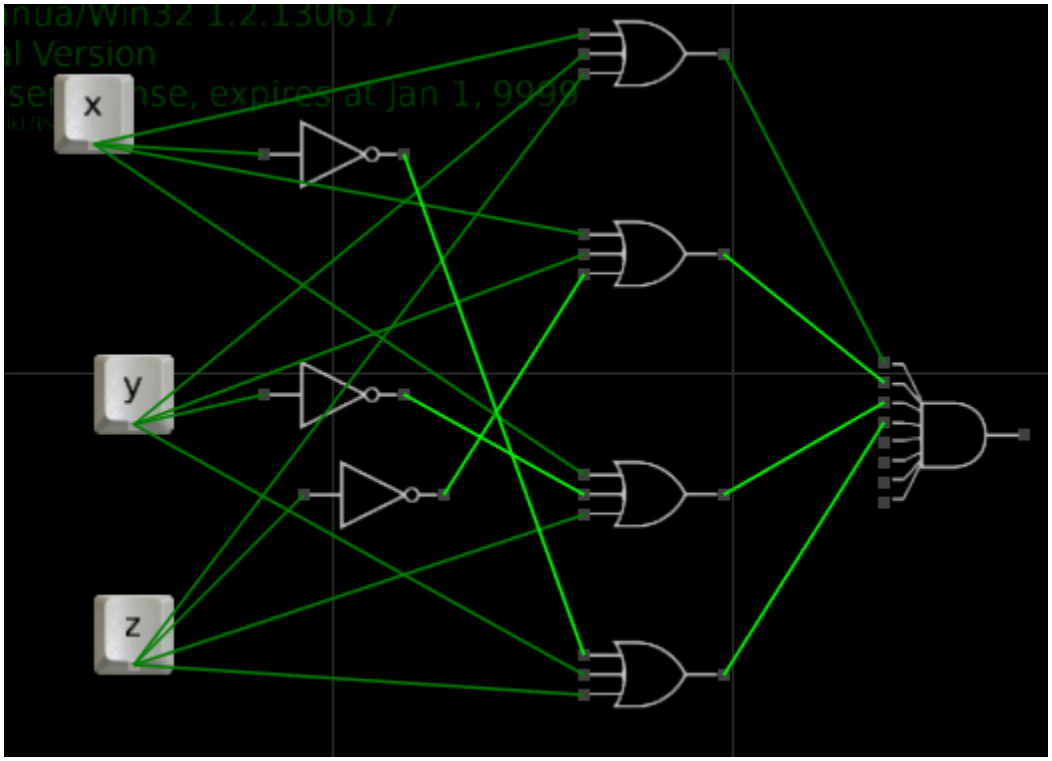
Maxterms : M0,M1,M2,M4

POS : (X+Y+Z).(X+Y+Z').(X+Y'+Z).(X'+Y+Z)

SOP



POS



Question 3:

g. F(X,Y,Z)=M(1,3,4,7)

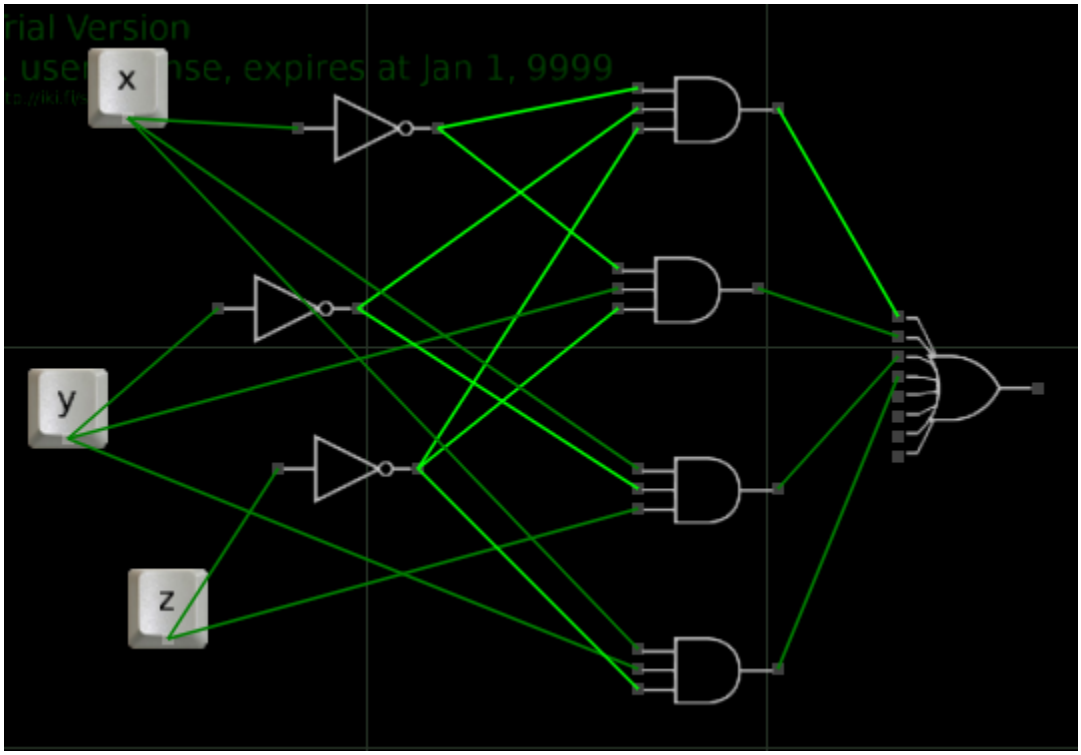
other form=m(0,2,5,6).

X	Y	Z	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

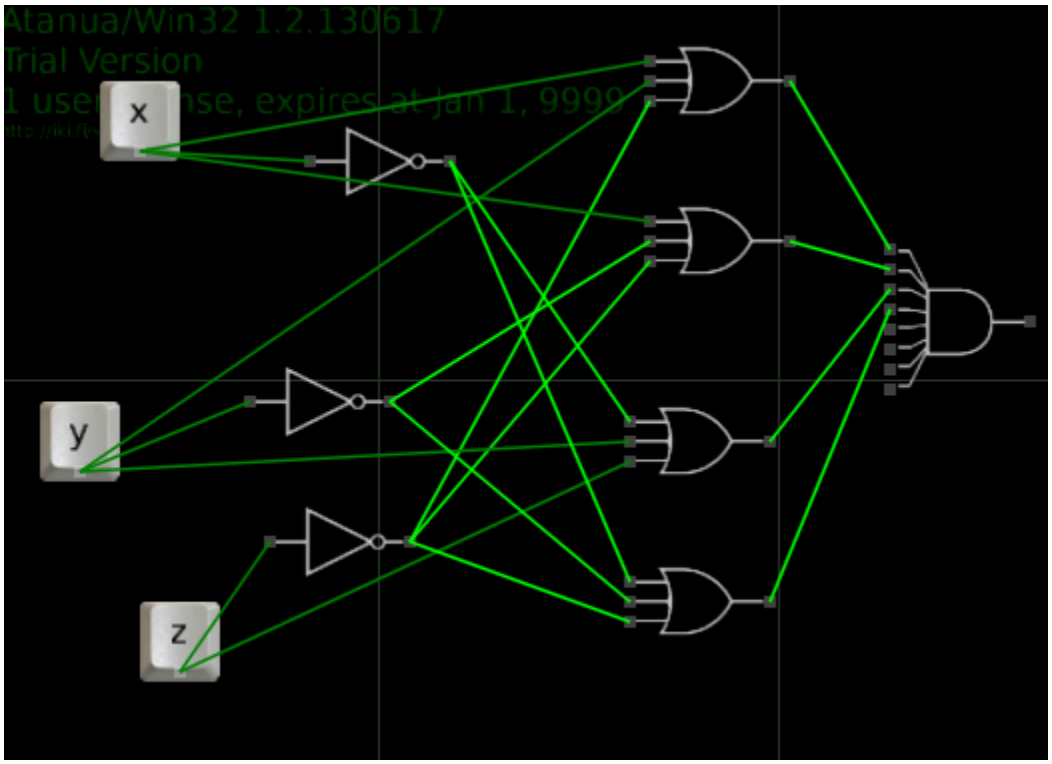
SOP= X’.Y’.Z’+X’.Y.Z’+X.Y’.Z+X.Y.Z’

POS= (X+Y+Z’).(X+Y’+Z’).(X’+Y+Z).(X’+Y’+Z’)

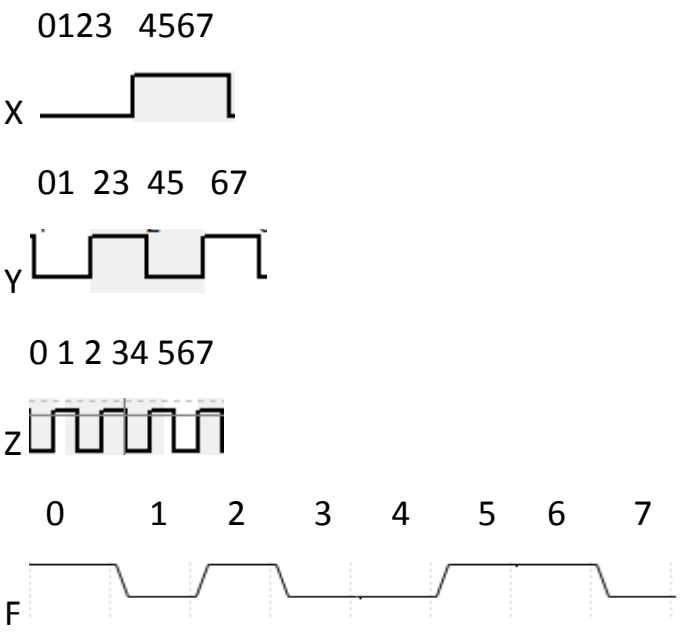
SOP



POS

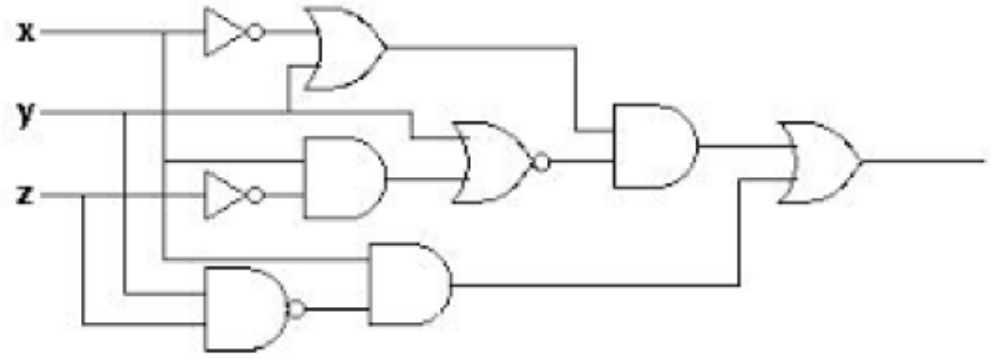


Input-output signal



Question 4

e.



F(X,Y,Z)=(X'+Y).((X.Z')+Y)'+X.(Y.Z)'

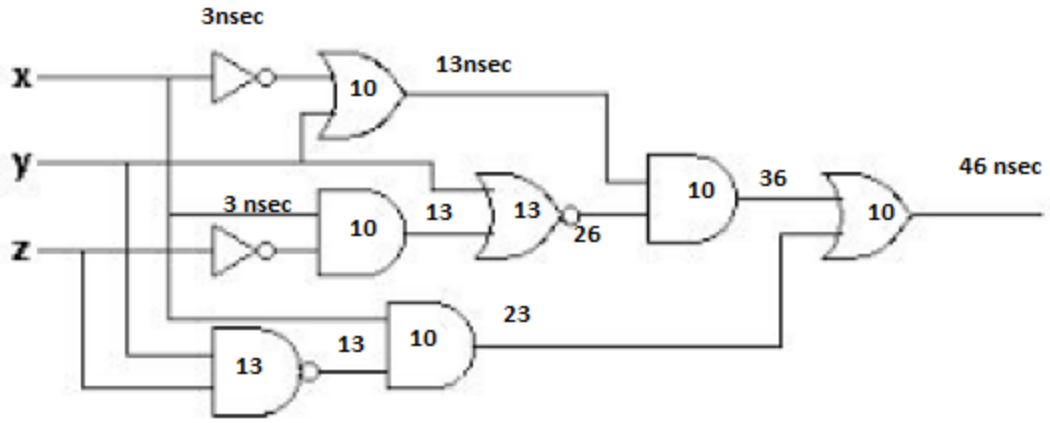
X	Y	Z	(X'+Y)	(X.Z')	(Y+(X.Z'))'	(X'+Y). (Y+(X.Z'))'	(Y.Z)'	(Y.Z)'.X	F
0	0	0	1	0	1	1	1	0	1
0	0	1	1	0	1	1	1	0	1
0	1	0	1	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0
1	0	0	0	1	0	0	1	1	1
1	0	1	0	0	1	0	1	1	1
1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	0	0	0	0	0

Minterms : m0,1,4,5,6

Maxterm: M2,3,7

SOP: (X'.Y'Z')+(X'.Y'.Z)+(X.Y'.Z')+(X.Y'.Z)+(X.Y.Z')

POS: (X+Y'+Z).(X+Y'+Z').(X'+Y'+Z')



Propagation delay = 46 nsec.

Question 5:

e. Four input NAND

TTL SSI 14 pin

2 pin for power

12 are remaining

Four input nand = 4 input and 1 output total=5 pin

12/5=2.4 take floor then 2.

Then we need 2 gates.