



LIMITER AMPLIFIER 179-230C
INSTRUCTION MANUAL

179-2310-C-4

Limiter Amplifier

179-230 C

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The limiter amplifier is especially designed as a "safe-limiter" with very high input overload margin to be used in places, where great care should be taken not to overload the subsequent equipment. Input reference level and recoverytime (dual) can be selected on the frontplate, and inside the unit pre-emphasis can be switched on/off, and the output level can be adjusted as well. The outputsignal can be monitored on the frontplate through a buffered control output in a way that shortcircuiting the output will not cause damage to the programme signal. Supply voltage to the limiter can be either symmetrical or unsummetrical with either positive or negative terminal as reference.

Temperature range	:	-10°C to +60°C amb.temp.
Supply voltage	:	22V to 32V DC or ±11V to ±16V DC
Maximum ripple voltage on supply	:	0,3V rms
Current consumption		
after heat-up at 25°C	:	appr. 65 mA (± 15 V supply)
during heat-up at 25°C	:	appr. 200 mA (± 15 V supply)
Input threshold level,		
in $2 \pm 0,2$ dB's step	:	from -10dBu to +10dBu
Output threshold level,		
internal adjustable	:	from 0dBu to +10dBu (Note 1)
Threshold level tolerance	:	±0,6 dB
Input overload margin	:	≥ 30dB above thresh level
Frequency response (fig. 1)	:	20 - 20 kHz ±0,5dB
Signal to noise ratio at		
threshold level	:	≥ 72dB weighted CCIR 468-1 (1976)
Distortion		
a) at threshold	:	≤ 0,2%
b) 0-20dB above thresh.level	:	≤ 0,3%
c) 20-30dB above thresh.lev.	:	≤ 0,5%
Input impedance (balanced floating)	:	22kOhms ±10%
Output impedance (balanced floating)	:	≤ 21 Ohms
Minimum load resistance	:	300 Ohms
Maximum output current	:	typ. 35mA rms

Input balance (CMRR) at 15 kHz	:	\geq 60dB
Output balance (CMRR) at 15 kHz	:	\geq 60dB
Control output, gain tolerance,		
$R_L \geq 10\text{kOhms}$:	$\pm 0,5\text{dB}$
Control output, output impedance	:	100 Ohms in series with
Pre-emphasis on threshold level		15uF
(internal switch)	:	50 us (fig. 2)
Control voltage slope	:	5dB/V (note 2)
Attack time	:	1,5 ms (note 3)
Recovery delay	:	50 ms $^{+60\%}_{-10\%}$
Recovery time T_1 Fig. 6	:	0,1-0,2-0,4-1-2-4 s/20dB $\pm 20\%$
Recovery time T_2 Fig. 7, 8 and 9	:	1-2-4-10-20-off s/20dB $\pm 20\%$
Mechanical outlines	:	see drawings fig. 5

Note 1:

Output reference level can be internally adjusted up to +21 dBu, however, technical specifications are only valid up to +10dBu.

Note 2:

The control voltage of two units may be linked together to obtain equal gainreduction in the two stereo channels.

Note 3:

The attack time is the period of time it takes the control voltage to reach 90% of its steady-state value, measured with 5kHz tone-bursts. Peaks shorter than 1,5 msec. will be limited by a full-wave smooth clipping circuit to a value approximately 3dB higher than output threshold level with steady sinusodial input-signal.

Fig. 3 and fig. 4.

Fig. 1. Relative frequency response.

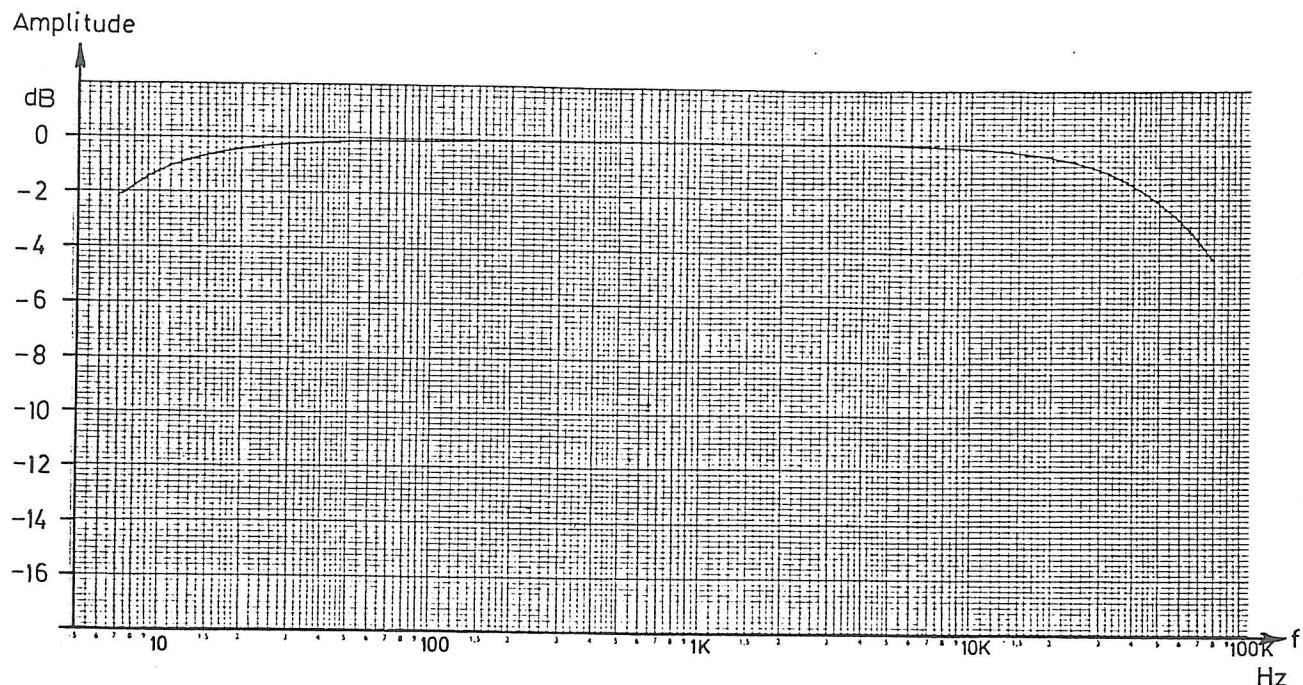
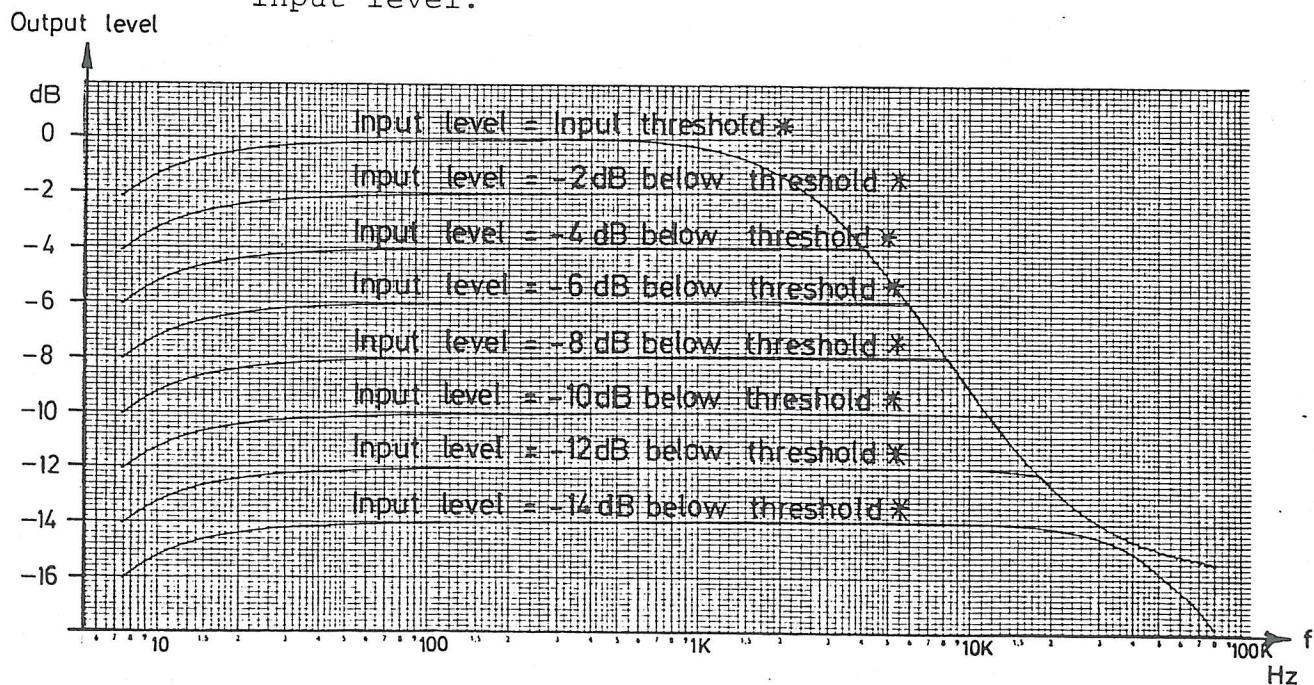


Fig. 2. Threshold level with pre-emphasis us. frequency and input level.



* refers to threshold level without pre-emphasis

Fig. 3 and 4. Output level and control voltage with 5 kHz tone-burst and input amplitude 10 dB above threshold level.

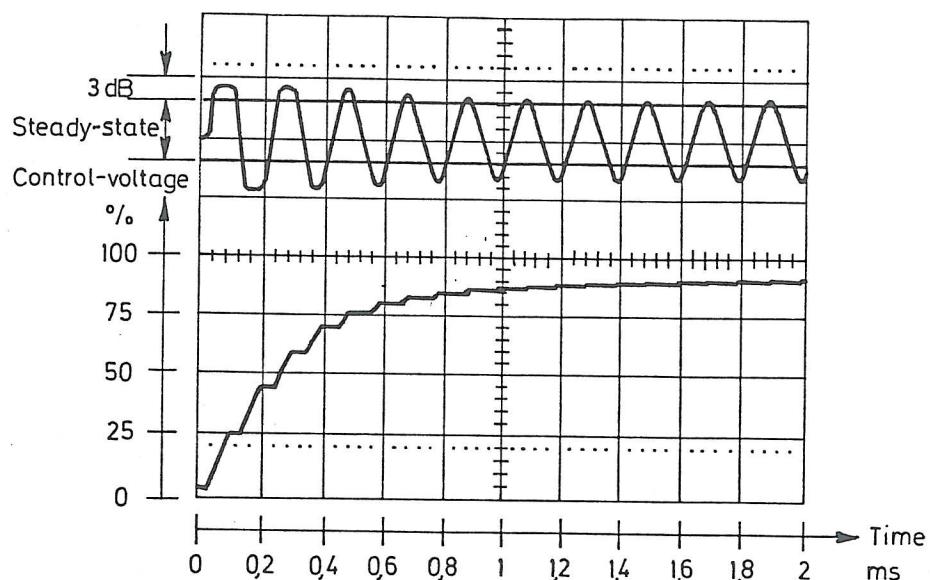


Fig. 5. Mechanical outlines and pin connections.

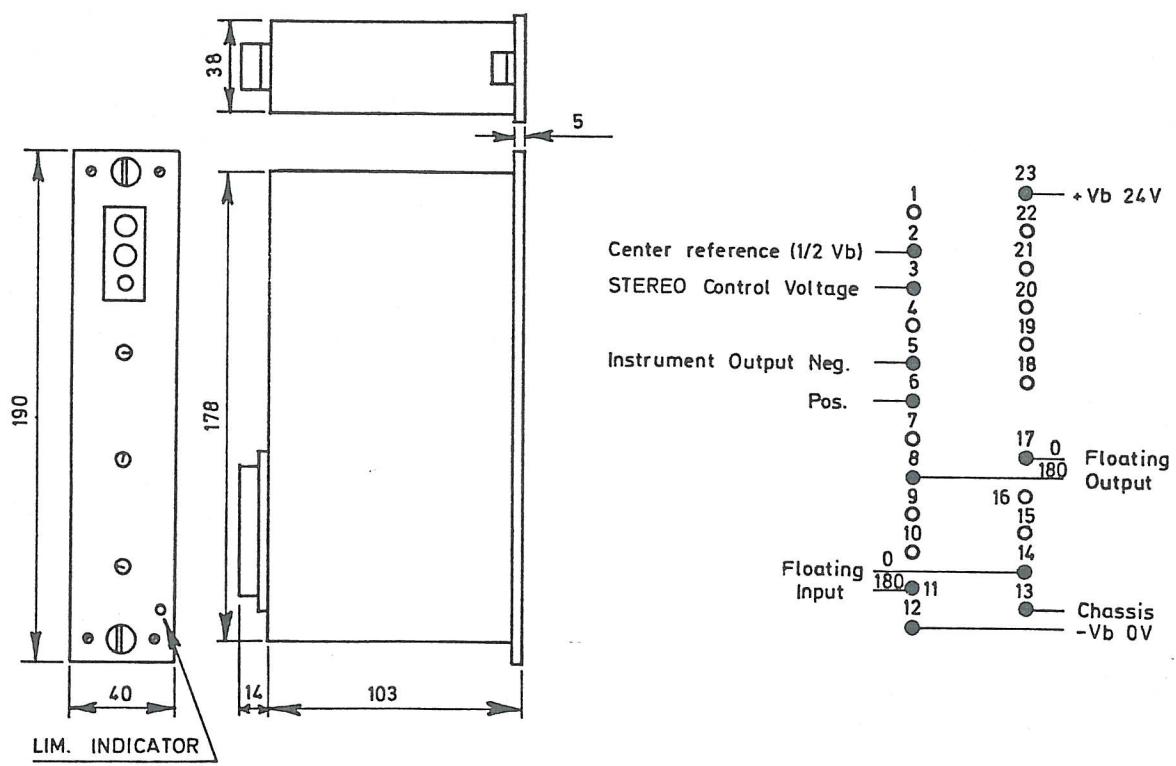


Fig. 6. Recovery us time and settings of T_1 .

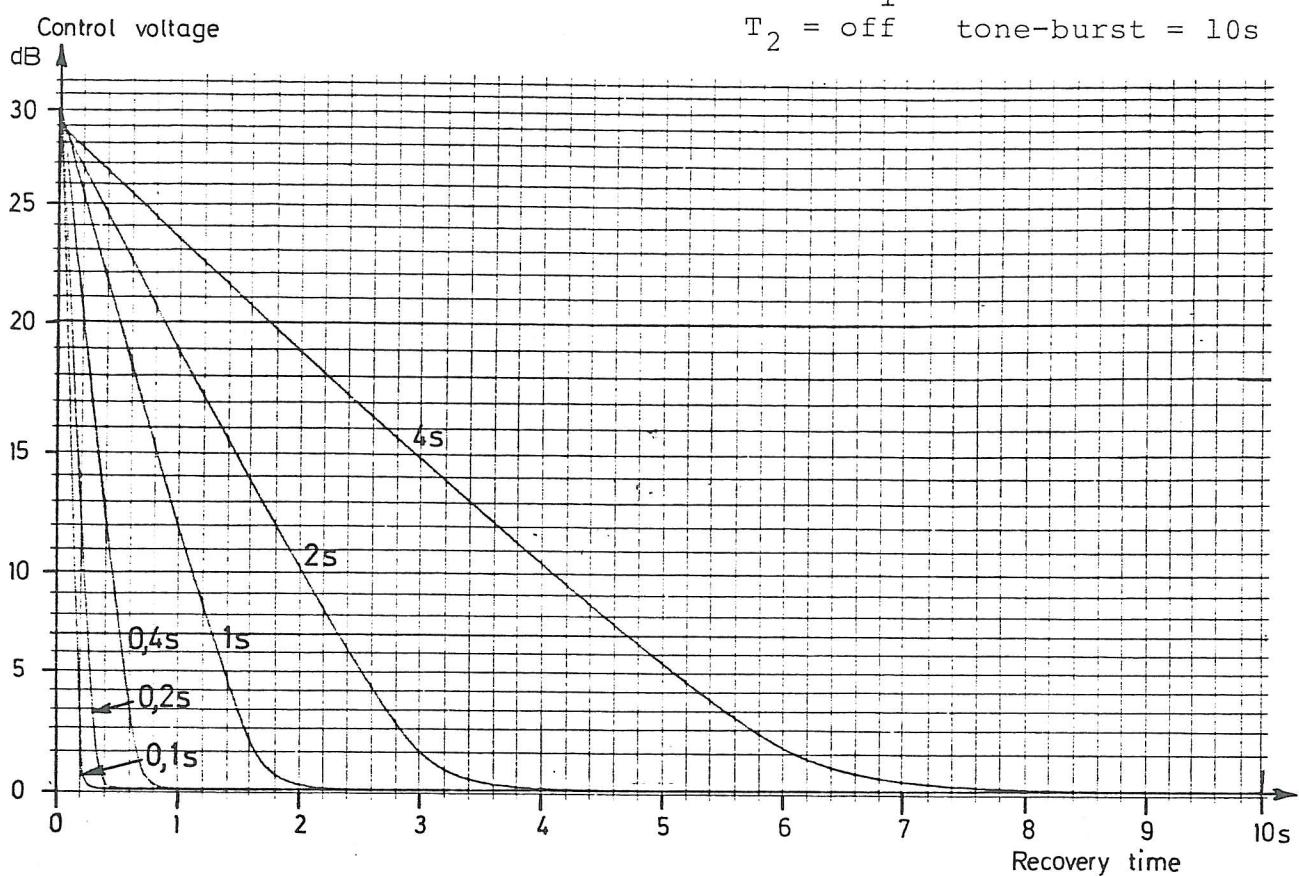


Fig. 7. Recovery us time and settings of T_2 .

$T_1 = 0.1\text{s}$ tone-burst = 10s

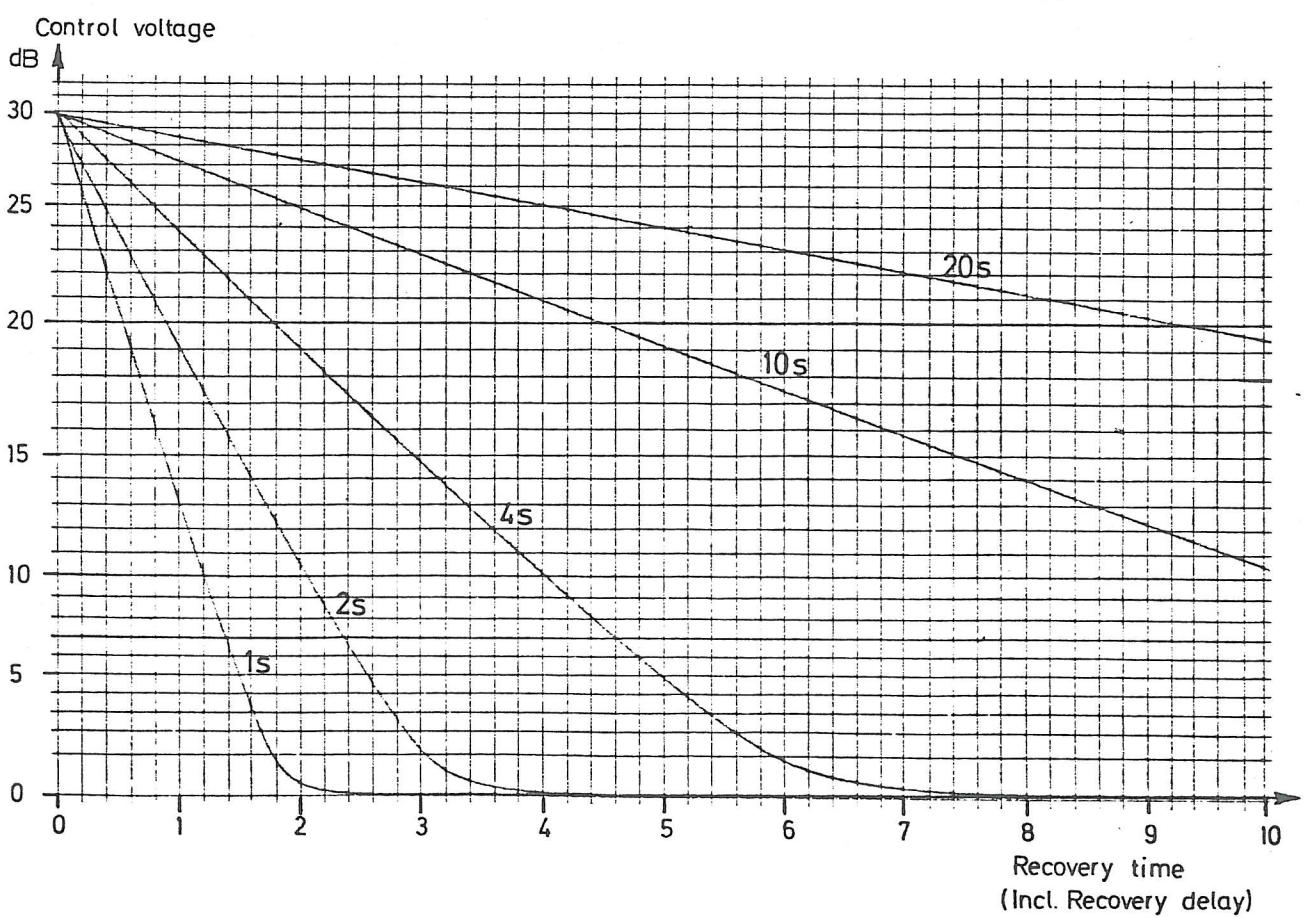


Fig. 8. Recovery us time and tone-burst length.

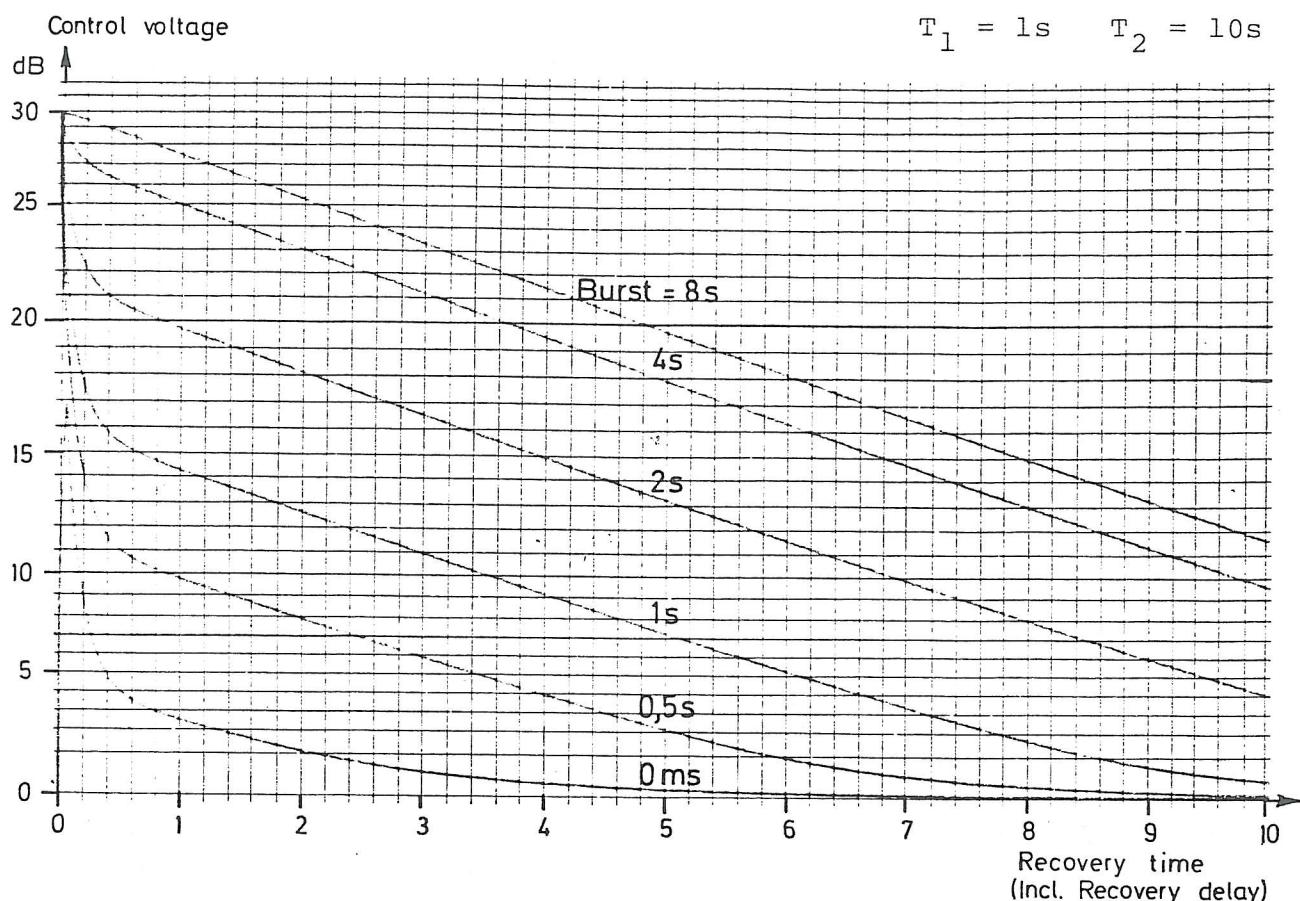
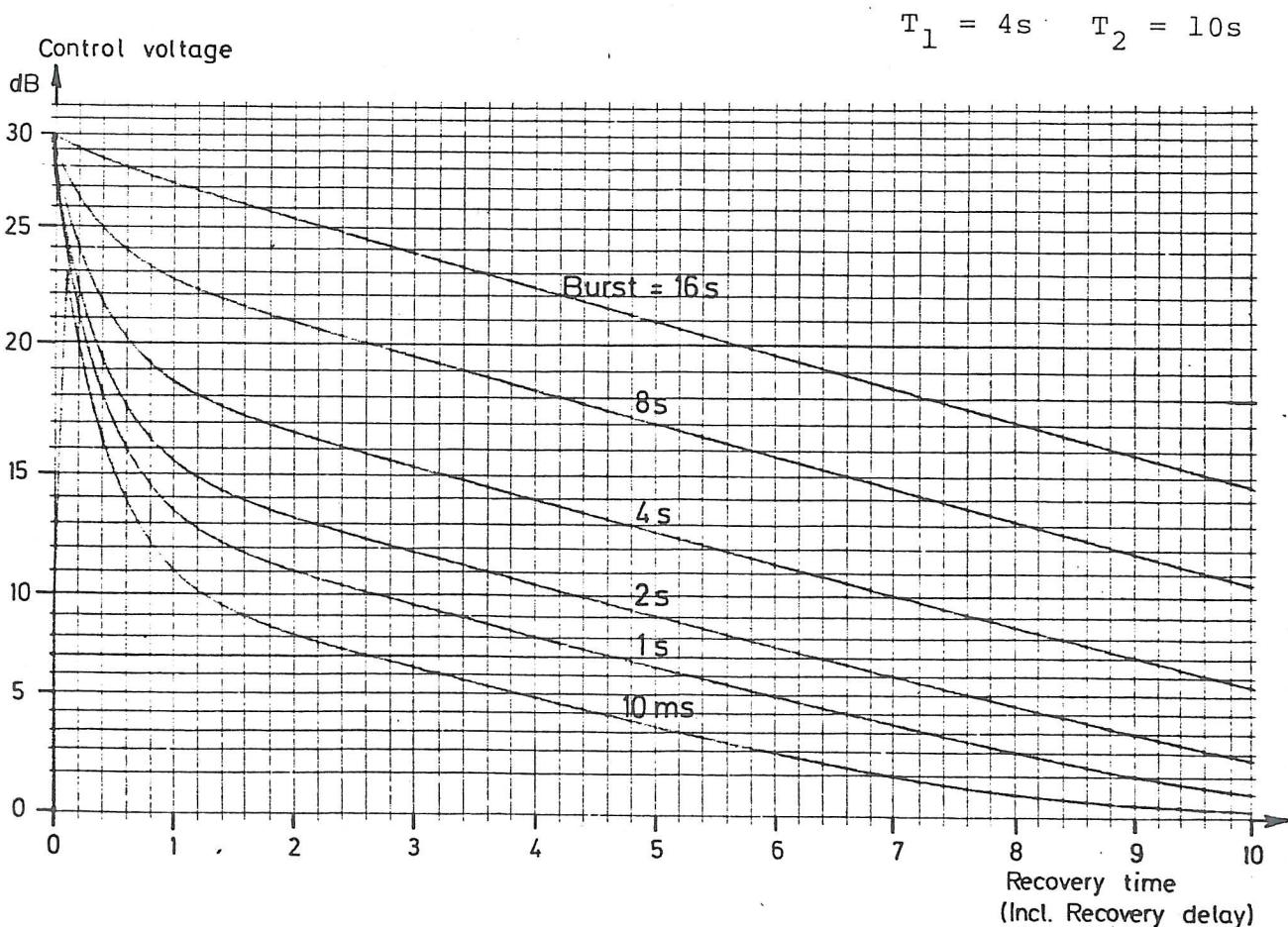


Fig. 9. Recovery us time and tone-burst length.



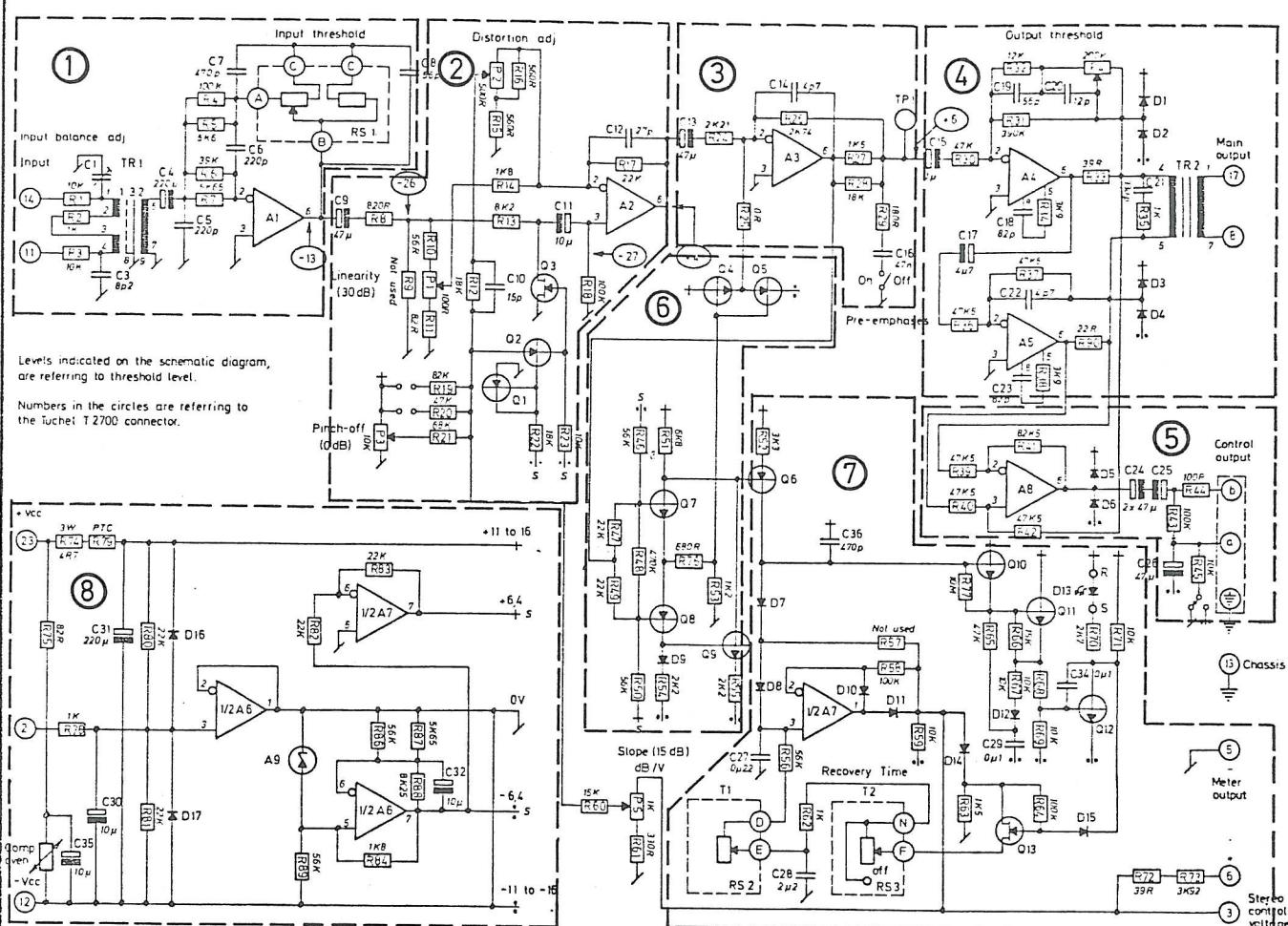


Fig. 10: Schematic diagram divided into subcircuits:

1 input circuit, 2 voltage controlled amplifier,
3 pre-emphasis amplifier, 4 main output stage,
5 control output stage, 6 rectifier, 7 timing and
recovery delay, 8 supply stage.

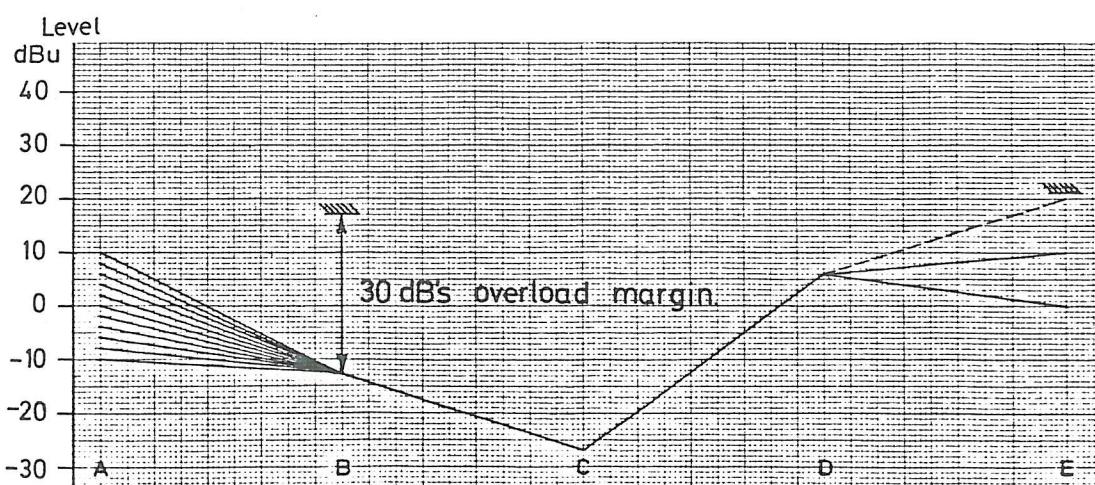


Fig. 11: Level diagram at threshold level (not valid with pre-emphasis)

1. Input Stage.

The input stage has variable gain and is designed with high input overload margin (30 dB). The stage is operating as an inverting 2' order low-pass filter, where the input transformer is placed in the "summing" point of the filter. Therefore only a very small voltage will occur across the transformer, and thereby the distortion is kept at a low value at high input levels and low frequencies. The variable capacitor C_1 adjusts the input balance of the transformer.

2. Voltage Controlled Amplifier.

The voltage controlled amplifier is using a bridge balance principle, when the source-drain resistance of a Field-Effect-Transistor is used a one of the balancing resistors. The gain can therefore be altered by changing the gate-source voltage of the FET. P_1 and P_3 adjust the operating point of the FET, and P_2 adjusts the harmonic distortion to minimum. Harmonic distortion adjustment is necessary due to the nonlinearity of the FET.

3. Pre-Emphasis Amplifier.

The pre-emphasis amplifier has two outputs. One output delivers signal to the rectifier/peak limiter circuit (6), and one output is feeding the output stages (4). The lastmentioned output is the feedback point of the amplifier, and the signal at this point therefore will be unaffected, when the pre-emphasis switch is closed, while the other outputsignal which is fed to the rectifier will be increased at higher frequencies and thereby making the threshold level frequency dependable. See fig. 2 in technical specifications.

4. Main Output Stage.

The main output stage is a symmetrical driven transformer coupled stage which gives the highest grade of output symmetry, output overload level and low current consumption. The output transformer is driven with a pre-distorted voltage swing which compensates the internal voltage drop across the copper resistance of the output transformer. This pre-distortion reduces the transformer output resistance and the distortion at low frequencies.

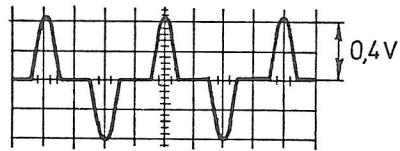
5. Control Output Stage.

The control output stage is a differential input amplifier stage which takes its inputsignal from output transformers primary signal for true indication of faults in the output amplifiers. A signal is furthermore taken from the output of A_5 to neutralize the pre-distorted primary voltage, so the control output voltage will be equivalent to the undistorted mainoutput voltage.

6. Rectifier.

The rectifier consists of two reversted biased transistors which are brought into its active region by the applied audio signal. When this threshold is reached, current starts to flow through the common emitter resistor and through resistor R_{51} . The voltage across R_{51} now will have the shape of a double rectified voltage. The transistor Q_6 will then start to change the timing capacitors in the timing circuit. See part 7.

Fig. 12:
Waveform of emitter voltage.



The common emitter resistor is designed as a voltage divider, where the lower voltage is fed to the bases of two transistors, whose emitters are in the feed-back loop of A_3 . If the base voltage exceeds approx. 0,3V, the transistors become active and will cause limiting of the peak amplitude of the output. Because the gain of this feedback loop is less than one, and the voltage/current function of the transistor has logarithmic relations, the clipping of the output voltage will be smooth.

7. Timing- and Recovery Delay Circuit.

The collector current of Q_6 changes the timing capacitors C_{27} and C_{28} , and the voltage across C_{27} is sensed by a FET-input operational amplifier, whose output is the control voltage. The discharge will be linear and dependable of the settings of controls T_1 and T_2 . The discharge voltage which causes the discharge current is the voltage drop over D_{14} , and the FET Q_{13} serves as a switch for incoupling of recovery delay. The transistor Q_{10} serves as a low input current buffer amplifier for changing the recovery delay timing capacitor C_{29} . Recovery delay time is determined by the resistance R_{66} which in conjunction with Q_{11} forms a constant current discharge circuit.

8. Supply Stage.

The input current to the unit flows through R_{74} and R_{79} which is a low resistance PTC resistor. In case of heavy current consumption, for instance due to a fault, inside the unit, the maximum current will be limited to the "hot current" of the PTC. R_{74-79} and C_{31} furthermore form a ripple filter for the supply line. The unit can be operated on either symmetrical or unsymmetrical supply voltage and has an internal voltage splitter which produces center reference voltage half of the external supply voltage (A_6 pin 1). A positive and a negative reference voltage is produced by A_7 and A_6 .

Normally the limiter amplifier will stay correctly adjusted, except when component has failed and has been replaced; then it may be necessary to make certain adjustments. The function of the trimpotentiometers and the variable capacitor is as follows:

- P₁ Linearity adjustment of the Field-Effect-Transistor
(control voltage linearity)
- P₂ Adjustment for minimum distortion of the FET
- P₃ Compensates for individual Pinch-off voltages of the FET
(input threshold level adjustm.)
- P₄ Adjusts the output threshold level
- P₅ Compensates for individual controlvoltage sensitivity of the FET
- C₁ Input balance adjustment

Do not attempt to make any adjustment, until the current consumption has fallen to a steady level (60-90mA) after 1 minute.

Correct sequence of adjustments is as follows:

a. Pinch-off adjustment of P₃

Conditions: Input threshold level 0dBu, Input level 0dBu, f=1kHz.

P₃ is adjusted, until the LED indicator on the frontplate is at the on/off threshold. The adjustment range can be altered by connecting or disconnecting R₁₉ and/or R₂₀.

b. Slope dB/V adjustment of P₅ and linearity adjustment of P₁

Conditions: As stated under position a.

A floating external DC-source (0-6V) is connected between terminal 3 and 5, terminal 3 positive. The DC voltage is set to 3,0V, and P₅ is adjusted, so that the output level is attenuated 15dB. Now the DC voltage is set to 6,0V, and P₁ is adjusted, so that the output level is attenuated 30 dB. Because of mutual dependence between P₅ and P₁, repeat the adjustments, until correct reading is obtained.

c. Distortion adjustment of P_2 .

Conditions: Input level +20dBu f=1kHz.

P_2 is adjusted to minimum distortion. Because of interaction between P_2 and the other adjustments repeat the adjustments under position a and b once more.

d. Output threshold adjustment P_4 .

Conditions: Input level +20dBu, f=1kHz.

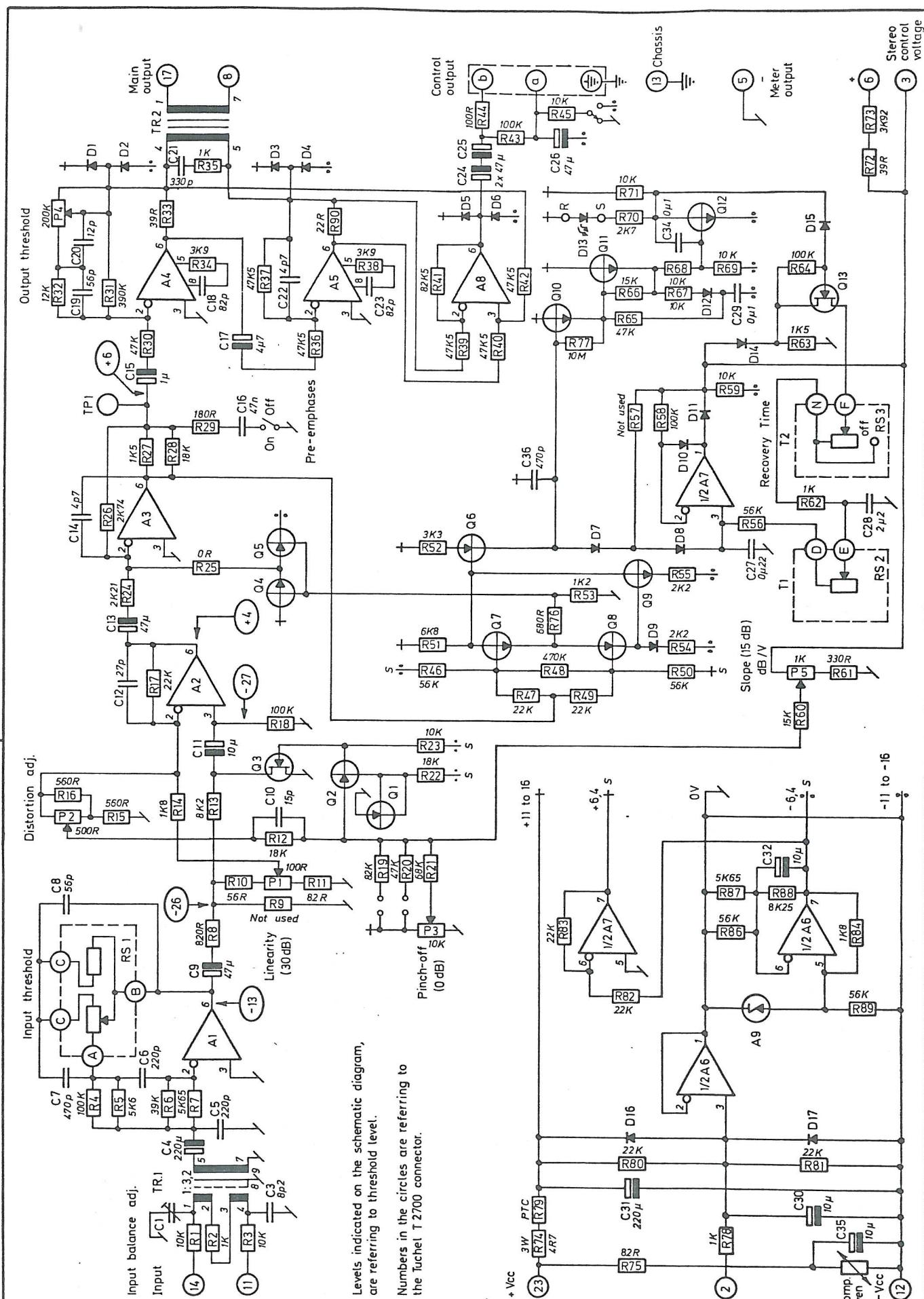
Adjust P_4 , until the wanted output threshold level is reached.

e. Input balance adjustment C_1 .

Conditions: Input threshold level 0dBu, input level +20dBu, f=15kHz.

Connect the two input terminals together, and apply the audiosignal between the two and negative supply line.

Adjust C_1 to minimum output signal.



Målestok	:
Konstruktør	:
Tegnet	: 21-9-78 JS
Godkendt	: KH.
Revideret	:

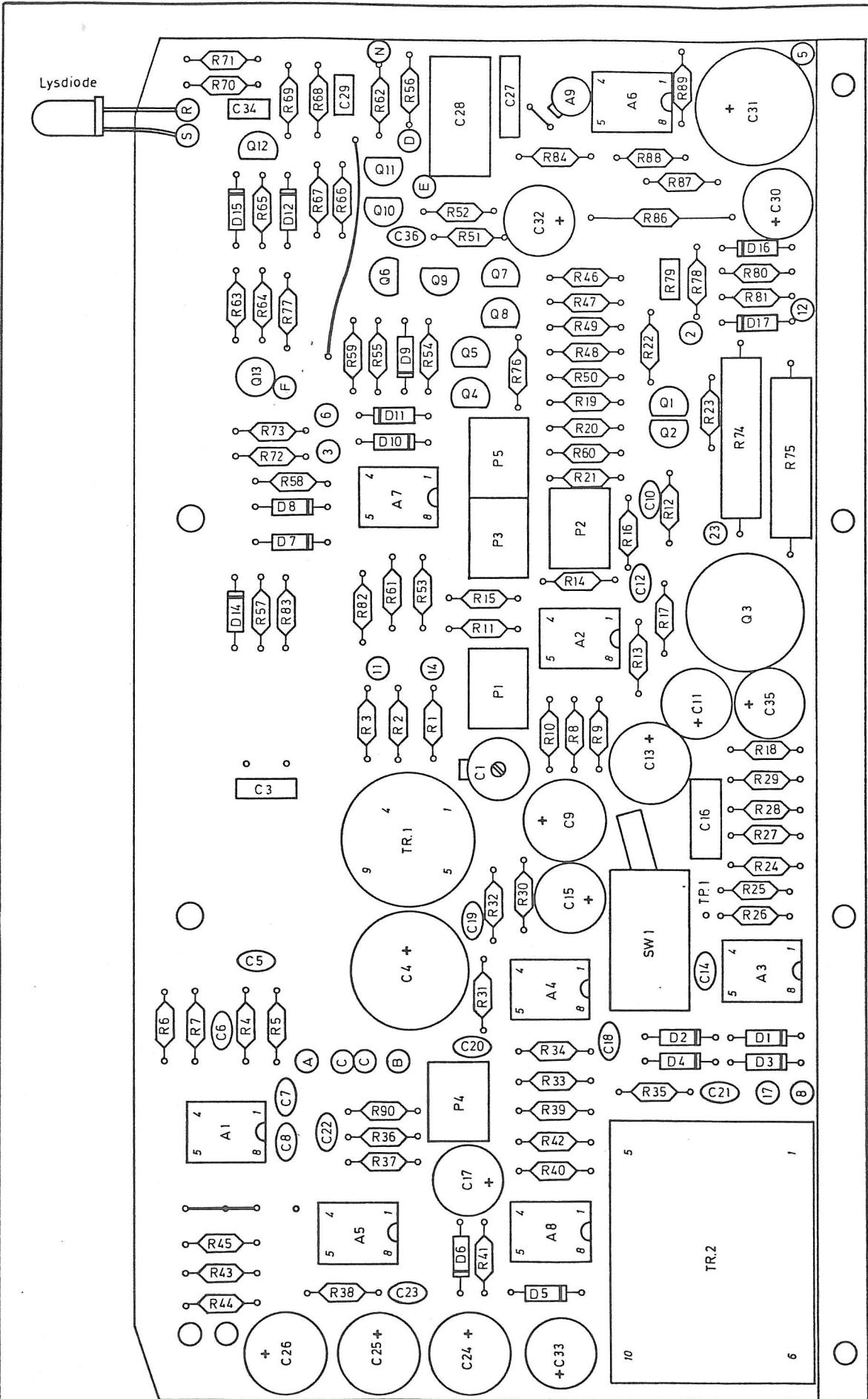
Limiter Amplifier Schematic Diagram

Numbers in the circles are referring to levels indicated on the schematic diagram, are referring to threshold level.

179 - 230 C

NTP
NTP ELEKTRONIK A/S

179 - 23A30 - C - 3



Målestok :	
Konstruktør:	
Tegnet : 22-9-78 JS	
Godkendt : KH.	
Revideret :	

Limiter Amplifier 179-230 C

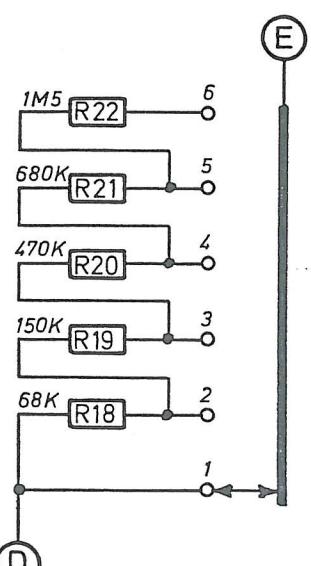
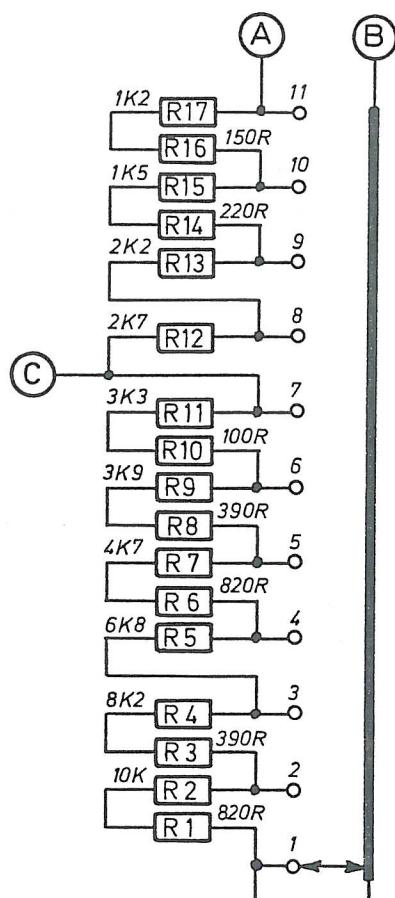
Component Lay-out



179-23A41-C-3

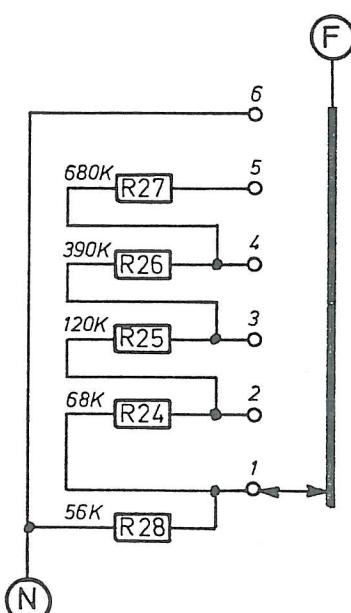
Ref. no.	Qty.	Description	Value / Size	Type no.	Manufacturer		
P90	1	Resistor	22R	1/8W	5%	SBB 0207	Beyschlag
R33,72	1	"	56R	"	"	"	"
R11	1	"	82R	"	"	"	"
R29	1	"	180R	"	"	"	"
R61	1	"	330R	"	"	"	"
R15,16	2	"	560R	"	"	"	"
R76	1	"	680R	"	"	"	"
R 8	1	"	820R	"	"	"	"
R 2,35,62, 78	4	"	1k	"	"	"	"
R53	1	"	1k2	"	"	"	"
R27,63	2	"	1k5	"	"	"	"
R14,84	2	"	1k8	"	"	"	"
R54,55	2	"	2k2	"	"	"	"
R70	1	"	2k7	"	"	"	"
R52	1	"	3k3	"	"	"	"
R34,38	2	"	3k9	"	"	"	"
R 5	1	"	5k6	"	"	"	"
R51	1	"	6k8	"	"	"	"
R13	1	"	8k2	"	"	"	"
R 1, 3,23, 45,59,67, 68,69,71	9	"	10k	"	"	"	"
R32	1	"	12k	"	"	"	"
R60,66	2	"	15k	"	"	"	"
R12,22,28	3	"	18k	"	"	"	"
R17,47,49, 80,81,82, 83	7	"	22k	"	"	"	"
R 6	1	"	39k	"	"	"	"
R20,30,65	3	"	47k	"	"	"	"
R46,50,56, 89,86	5	"	56k	"	"	"	"
R21	1	"	68k	"	"	"	"
R19	1	"	82k	"	"	"	"
R 4,18,43, 58,64	5	"	100k	"	"	"	"
R31	1	"	390k	"	"	"	"
R57,48	2	"	470k	"	"	"	"
R77	1	"	10M	"	"	"	"
R24	1	"	2k21	1/8W	1%	2322-151-52212	Philips
R26	1	"	2k74	"	"	"	"
R73	1	"	3k92	"	"	"	"
R 7,87	2	"	5k65	"	"	"	"
R88	1	"	8k25	"	"	"	"
R36,37,39, 40,42	5	"	47k5	"	"	"	"
R41	1	"	82k5	"	"	"	"
R74	1	"	4R7	3W		Type 211	Diplomatic
R75	1	"	82R	"		Type 211	"
R44	1	Resistor	100R			CRS	Philips
R25	1	Strap					
R79	1	PTC resistor				P9390-F51	Siemens

Ref. no.	Qty.	Description	Value / Size	Type no.	Manufacturer		
P 1	1	Potmeter, trim.	100R	3386P-1-101	Bourns		
P 2	1	" "	500R	3386P-1-501	"		
P 5	1	" "	1k	3386P-1-	"		
P 3	1	" "	10k	3386P-1-103	"		
P 4	1	" "	200k	3386P-1-204	"		
C14,22	2	Capacitor, ceramic	4P7	100V	2%	2222-632-57478	Philips
C 3	1	" "	8P2	500V	2%	2222-650-57828	"
C20	1	" "	12P	100V	2%	2222-632-58129	"
C10	1	" , styroflex	15p	160V	2,5%	B31310	"
C12	1	" "	27P	100V	2%	2222-632-70279	"
C 8,19	2	" "	56P	"	"	2222-632-70569	"
C18,23	2	" "	82P	"	"	2222-632-70829	"
C 5, 6	2	" "	220P	"	"	2222-632-70221	"
C21	1	" "	330P	"	"	2222-632-70331	"
C 7,36	2	" "	470P	"	"	2222-632-70471	"
C16	1	"	47n	250V	5%	B32561-D3473-J	Siemens
C34,29	2	"	100n	100V		FSK 2 min	Wima
C27	1	"	220n	100V		B32561-D1224-J	Siemens
C28	1	"	2u2	100V		B32562-D1225-J	"
C15,33	2	" , ellyt	1u	63V		EKO	EKO
C17	1	" "	4u7	63V		EKO	"
C11,30,32, 35	4	" "	10u	63V		EKO	"
C 9,13,24, 25,26	5	" "	47u	40V		EKO	"
C 4,31	2	" "	220u	40V		EKO	"
C 1	1	" , trim.	2-22pF			2222-808-11229	Philips
D 1-12,14, 15	14	Diode				1N4148	
D16,17	2	"				1N4002	
Q 4	1	Transistor				BF241	
Q 1,2,6,8	4	"				BC307B	
Q 7, 9-12	5	"				BC237B	
Q 5	1	"				BF450	
Q13	1	FET				ZN4302	
Q 3a	1	"				Si 216-N	
Q 3b	1	Component oven				5 STL-Z	
A 1, 8	2	Op-amp				LF 356	
A 2- 5	4	"				TDA 1034	
A 6	1	"				RC 4558	
A 7	1	"				LF 353	
A 9	1	Reg. regulator				ZN 458	
Tr 1	1	Transformer				310-203-002	Ferranti
Tr 2	1	"				LL 5001	Beyer
S1	1	Switch				06.17631.19	Lars Lundahl
TP 1	1	Soldering post				APL-65	Secme
	1	P.C. board				179-2340C	Assmann
	1	Mounting block				235-1016	NTP



RS 1.

RS 2.



telser

Målestok :

Konstruktør: H.E.N.

Tegnet : 13-10-78 JS

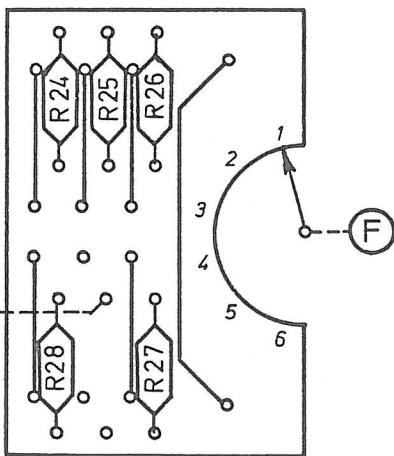
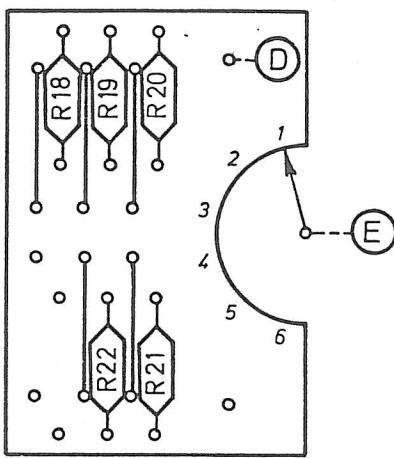
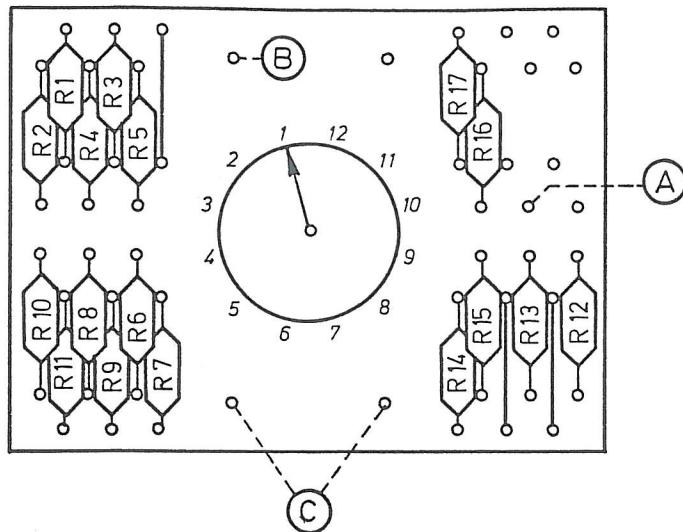
Godkendt : KH.

Revideret :

Switch Unit
Limiter Amplifier 179 - 230 C
Schematic diagram

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179 - 2332 - C - 4



Målestok : 2:1
Konstruktør: H.E.N.
Tegnet : 16-10-78 JS
Godkendt : KH.
Revideret :

Switch Unit
Limiter Amplifier 179-230C
Components Lay-out.

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179 - 2343 - C - 4

Ref. no.	Qty.	Description	Value / Size	Type no.	Manufacturer
R10	1	Resistor	100R	1/8W	5%
R16	1	"	150R	"	"
R14	1	"	220R	"	"
R 3, 8	2	"	390R	"	"
R 1, 6	2	"	820R	"	"
R17	1	"	1k2	"	"
R15	1	"	1k5	"	"
R13	1	"	2k2	"	"
R12	1	"	2k7	"	"
R11	1	"	3k3	"	"
R 9	1	"	3k9	"	"
R 7	1	"	4k7	"	"
R 5	1	"	6k8	"	"
R 4	1	"	8k2	"	"
R 2	1	"	10k	"	"
RS 1	1	Switch			
	1	Print	MX 1/1 x 11K T=12 182-900		



SWITCH UNIT
LIMITER AMPLIFIER 179-230C
ELECTRICAL PARTSLIST

Partlist

Page 1 of 3

No.: 179-2333-A-3

Ref. no.	Qty.	Description	Value / Size	Type no.	Manufacturer	
R18	1	Resistor	68k	1/8W	5%	Beyschlag
R19	1	"	150k	"	"	"
R20	1	"	470k	"	"	"
R21	1	"	680k	"	"	"
R22	1	"	1M5	"	"	"
RS 2	1 1/2	Switch Print		MX 1/1 x 6k T=12 182-900	EBE NTP	

Ref. no.	Qty.	Description	Value / Size	Type no.	Manufacturer
R28	1	Resistor	56k	1/8W	5%
R24	1	"	68k	"	"
R25	1	"	120k	"	"
R26	1	"	390k	"	"
R27	1	"	680k	"	"
RS 3	1	Switch		MX 1/1 x 6k T=12	EBE
	1/2	Print		182-900	NTP