DK-Audio A/S
Marielundvej 37D
DK-2730 Herlev
Denmark

PT 5230 Digital Video Generator

Service Manual

PT 5230 Digital Video Generator, Service Manual

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Contents

1 General Service Information

1.1 Use of the Service Instructions

Troubleshooting is best carried out on a functional level using block diagrams. Reference is made to Chapters/Paragraphs – “Block Diagram Description” for an overall description of the instrument. The block diagrams of each individual unit are described in the chapters to follow. Drawings to be found in full size in Section with Diagrams
Fault finding to component level will however, require the use of appropriate circuit diagrams.

1.2 Safety

The opening of covers or removal of parts, except those to which access can be gained by hand, is liable to expose live parts. Accessible terminals may also be live.

The instrument must be disconnected from all voltage sources before performing any adjustment, replacement, maintenance, or repair, which requires the instrument to be opened.

If adjustment, maintenance, or repair of the opened instrument is unavoidable, it must only be carried out by a skilled person who is aware of the hazards involved.

1.2.1 Electrostatics Sensitive Devises

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD).

Careless handling during repair can reduce life drastically.

When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance. Keep components and tools also at this potential.

1.3 Block Diagram Symbols Description

Various symbols and conventions are used in the block diagram and a short description of these is given below.

1.3.1 Functional Block Information

The bold text within the block gives the function provided by the block.

Test shows the major components in the block or stage.

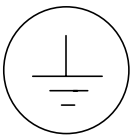
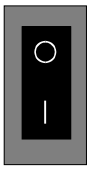
The number in the lower right hand corner of the block shows on which sheet of the appropriate circuit diagram the block may be found.

1.3.2 The Dotted Line

A dotted line around a functional block (or stage) means that the block is either an option or not used in all versions of the instrument

ATTENTION

1.4 Safety Symbols

Symbol	Colour:	Explanation:
	Red	High voltage terminal: a terminal at which a voltage, with respect to another terminal or parts exists or may be adjusted to 1000 V or more. (High voltage > 1000 V).
	Black/Yellow	Live part shock risk of electric shock.
	Black/Yellow	To preserve the instrument from damage the operator must refer to an explanation in the instruction manual.
	White/Black	Protective earth (grounding) terminal.
~	Black	Alternating current (placed on the indentification plate).
	White/Black	Off (supply – mains switch). On (supply – mains switch).

2 Instrument Block Diagram

2.1 General Information

The PT 5230 Digital Video Generator is a dual standard genlockable generator, which can be, equipped with a large number of individual signal and pattern generators to suite many different applications. It is especially designed to fit into digital and mixed digital/analog video installations and it provides signals for fault finding and checking of the entire digital chain.

Both Serial Digital Interface (SDI) and composite analog video generator modules are available as well as AES/EBU digital audio test signal generators. SDI generators have embedded digital audio included. A Time Clock Generator option can transform external LTC or VITC time information into date and time text in the pattern.

Characteristic for the PT 5230 is that generator outputs can be time shifted individually to solve the special timing problems which are found in mixed digital/analog video installations.

Please see the “PT 5230 Digital Video Generator – User’s Manual” for a detailed description of the instrument features.

The PT 5230 instrument block diagram is shown in Figure 2-1. The PT 5230 has a very flexible structure: a simple basic configuration can be easily extended by mounting individual options in the form of separate PCB modules. In the instrument block diagram (Fig. 2-1) the optional function blocks are surrounded by a dotted outer line. Only options known at the time of printing are included; future may bring more option modules.

2.2 Basic Instrument

The basic instrument, PT 5230 without any options, is the simplest possible version of the instrument. The instrument block diagram (Fig. 2-1) shows the names of the function blocks belonging to the basic instrument written inside full line boxes. The circuits of the basic instrument are located in one of 4 different units: the small number in the lower right corner of each block indicates which unit. The units are numbered as follows:

- Main Board : Unit 1
- SPG Board : Unit 2
- Front Panel Assy : Unit 3
- Power Supply Module : Unit 4

2.3 Sync Generator Block and Related Functions

2.3.1 Input Selector & Analog Genlock Monitor

The internal Sync Generator block can be synchronised to an external reference signal at “ANALOG GENLOCK” A or B input. The possible genlock signal types are:

- Composite sync
- Composite video
- Fsc or
- 5 MHz or 10 MHz continuous wave signals

The input selector is operated from the Master Controller. Four different modes are possible:

- Genlock to A

- Genlock to B
- Signal looped through between A and B
- Internal reference

An analog buffer makes a “GENLOCK MONITOR” output available.

Genlock to an external SDI signal is possible via the optional SDI Digital Genlock (PT 8606).

2.3.2 Sync Generator Block

The most important function of the Sync Generator block is to supply different digital synchronisation signals to the general synchronisation bus in the PT 5230. From this bus, each of the generators obtain a convenient set of synchronisation signals which simultaneously provides G and M television system related signals as well as characteristic frequencies for synthesis of the SDI signals.

All signals are derived form the internal OCXO frequency reference. The OCXO is ether free-running or locked to the “ANALOG GENLOCK” input as defined by the user.

2.4 Master Controller and Related Functions

2.4.1 Master Controller

As shown in the instrument block diagram (Fig. 2-1) the Master Controller controls many different functions such as:

- User interface handling via Keyboard and Display
- Remote Interface RS 232 or TTL
- Setting of:
- Input Selector
- Sync Generator
- and options
- Automatic identification of the mounted options
- Monitoring instrument temperature and control of the fan
- Monitoring the power supply voltages and the Level Detector status
- Transfer of date and time info from Time Clock Interface (PT 8637) to generators.

The Master Controller communicates with its surroundings via three different I^2C busses, a V24 bus, and several parallel ports.

2.4.2 Keyboard

The Keyboard is a separate PCB board located on the Front Panel assembly. It contains the front panel buttons and LEDs and their drivers. The Master Controller scans the buttons and controls the LEDs.

2.4.3 Display

The Display is an LCD matrix display with its own processor and drivers. The information displayed is received from the Master Controller.

2.4.4 Remote Interface (RS232 & TTL)

Two alternative remote interfaces can be selected by internal configuration:

- RS 232 or Parallel TTL

The blocks shown in fig. 2-1 contain only drivers; the Master Controller handles the communication directly.

2.4.5 Temperature Detector & Fan

The internal instrument temperature is measured by a sensor connected to the Master Controller.

Measurement of the internal temperature is used to control the Fan. If too-high temperatures are detected, a warning message appears in the display.

2.4.6 Level Detectors

The presence of signal of all generator outputs are monitored.

The Level Detector has two purposes:

- A direct error line is sent to a PT 5211 VariTime™ Changeover to indicate illegal signals
- Each generator status is monitored by the Master Controller, which then causes a warning to appear on the display if necessary

The Level Detector block actually represents many separate detectors, each located at a generator output; a detector follows its generator module. Multiple output generators have multiple detectors, one at each output.

2.4.7 Analog Black Burst Generator

The PT 52230 contains two independent Analog Black Burst Generators with controllable time shift adjustment.

2.4.8 Power Supply

A switched mode power supply module is used. It covers the full range of mains voltage without any configuration.

2.5 Options

Various optional units can easily be mounted in the PT 5230. Available options are shown in dotted boxes in the instrument block diagram (fig. 2.1).

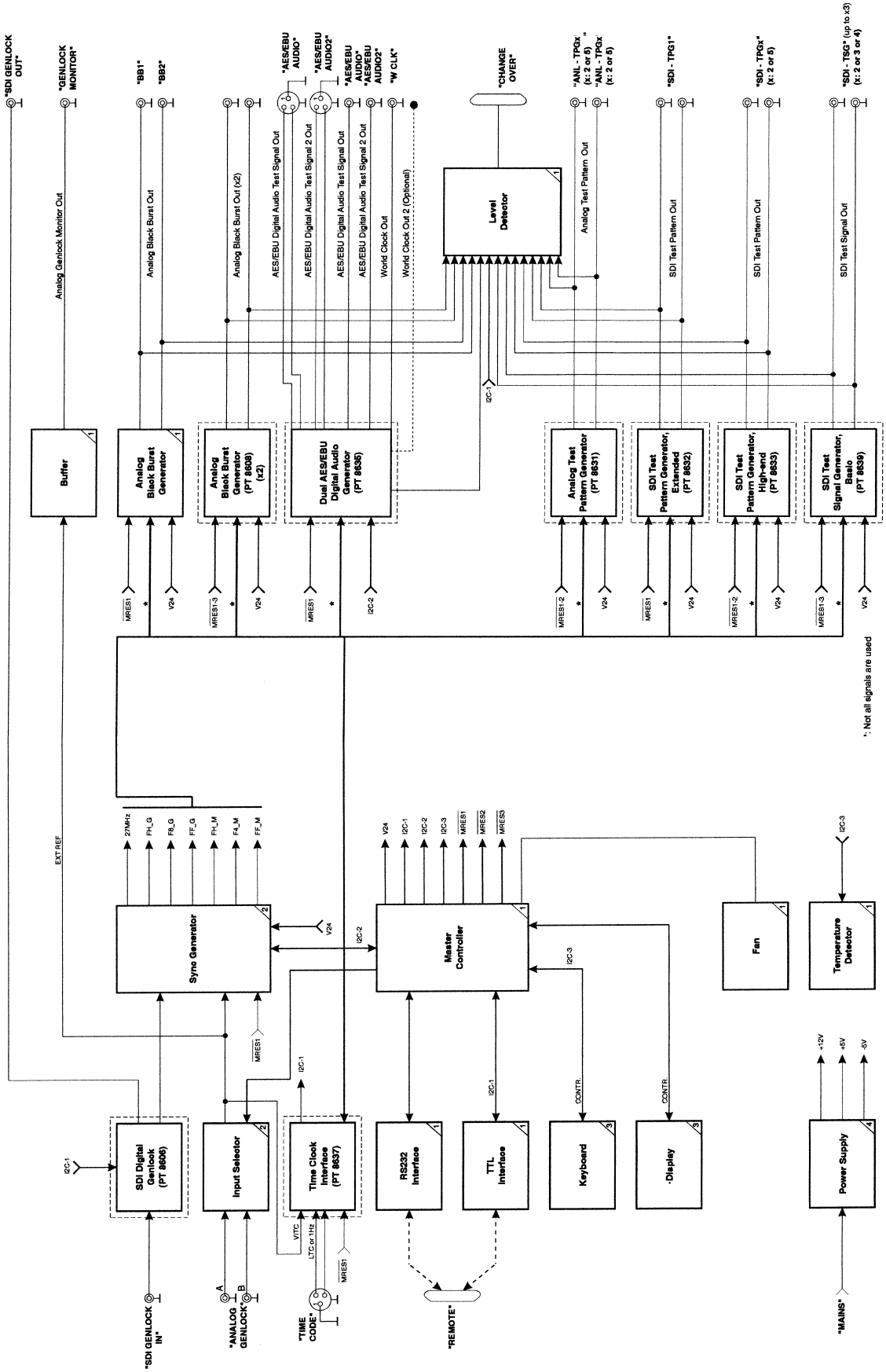
The options are typically connected to the shared synchronisation bus and to one of the communication busses.

Most of the options have their own microprocessor for local control of the operation of the option. This means that once the Master Controller has identified the option and communicated the desired settings (such as TV system, signal type, time delay, etc.) the option is able to perform its function without help from the Master Controller.

Options are automatically identified during power-up of the instrument and the content of display menus is context dependent.

The options available are described in separate chapters.

For a full size diagram, please refer to Section 2



3 Block Diagram Description - PT 5230

3.1 Master Controller

3.1.1 Overall Description

The Master Controller receives commands from the Keyboard unit and the Remote Interface (RS232 or TTL). It translates and communicates the commands to the various parts of the apparatus. The Master Controller also includes a data store for the apparatus' status parameters, which are necessary for a correct start - up.

The heart of the Master Controller is the µController (V401), which runs at about 30MHz. It uses an Address Latch (V402), a Program/Data PROM (V403), and a battery backed-up RAM (V404) together with Address Decoders (V409 and V410). The interface consist of parallel ports and serial busses (I^2C and V24).

3.1.2 Functional Description

The Keyboard is read via a local I^2C bus connected directly to the µController (FRONT-SCL and FRONT-SDA). The Serial Remote Control circuit (V445) also interfaces directly with RX, TX, CTS, RTS, DCD, and DSER. Gate (V441) in the DSR path prolongs the Reset Pulse to pin 17 necessary for the correct start-up of the µController.

The µcontroller's second internal serial bus (at RX_COM, TX_COM) serves as an interconnection between the Master Controller and the other µControllers in the apparatus.

At parallel ports (V405 and V407) are two I^2C busses (SCL1/SDA1 and SCL2/SDA2), which are also used as interconnections to other functional units. The TTL interface uses SCL1/SDA1.

Other output ports are used for Display (from V411, V412), Reset ($\overline{MRES}$) to other units (from V412), control of the SDI Digital Genlock, PT 8606, (from V413) and driving of the Watch-dog circuit, V423, (from V412).

Display contrast is controlled by V421, which also monitors the internal temperature of the apparatus in order to control the fan connected to transistor Q400.

V 415 and V416 are extra RAM for storing test parameters.

Disabling of Level Detectors
It is possible to disable Level Detectors by use the Code Field (PP1) on the Main Board (Unit 1).

Each Level Detector has its own signal (BB1_OK..BB9_OK) into the Code Field (PP1). When a signal is to be disabled connect the signal to +5V in PP1.

A detailed description can be found in Operating Manual.

3.2 Analog Black Burst Generator – Main Board

The input to the Black Burst Generator is a 27 MHz clock signal, a line and field reference for both PAL-G and NTSC, and a V24 serial bus form the Master Controller to select phase and system.

The μProcessor (V201, V203, V204 and V212) receives data via the V24 bus and outputs course horizontal phase and line type to the H-Counter (V206). Fine horizontal phase, burst phase, and system are outputs to the Phase Latch (V205).

The μProcessor is controlled by a line interrupt pulse and a field pulse. The μProcessor controls 2 Black Burst Generators.

The course horizontal phase from the μProcessor goes to the H-Counter/Decoder (V206) which is preset to the course horizontal phase at the horizontal timing reference.

The H-Counter is decoded together with line type information from the μProcessor, and it also addresses the signal PROMs.

The video data is stored in 2 EPROMs (V207 and V208) which are addressed by the H-Counter/Decoder and the Phase Latch.

The outputs from the PROMs are multiplexed to a 27 MHz 10-bit data stream. The data is sent to D/A Converter (213, V214 , V215, and V217) through an Anti-aliasing Filter to the Output Amplifier (V216).

3.3 Input Selector – Unit 2

The Input Selector (V2) can be configured from front plate or remote to either a loop-through input or a dual standard input.

When dual standard is selected you can select either “ANALOG GENLOCK” input A or input B form the front plate or remote.

3.4 Sync Generator – Unit 2

The signal from the Main Board goes to Reference Select (V5) and the 10/5 MHz Divider & Filter (V1, V3, and V4). The 10/5 MHz Divider (V3) is used if a reference frequency is selected.

Reference Select (V5) selects either video or frequency reference. The signal then goes to a DC-Restore circuit (V6, V13, and V15) through an Anti Aliasing Filter to the video A/D Converter (V10).

The output from the video A/D Converter goes to Ext_Logic (V12) and to a Dual Port RAM (V301).

The Ext_Logic (V12) finds field and line; this information goes to the μProcessor (V303, V304, V305, V312, and V313). The μProcessor also looks at the video information in the Dual Port RAM (V301) and use this information to decide when to lock, onto the external source.

The output pulses are all divided down from the 27 MHz OCXO (A1).

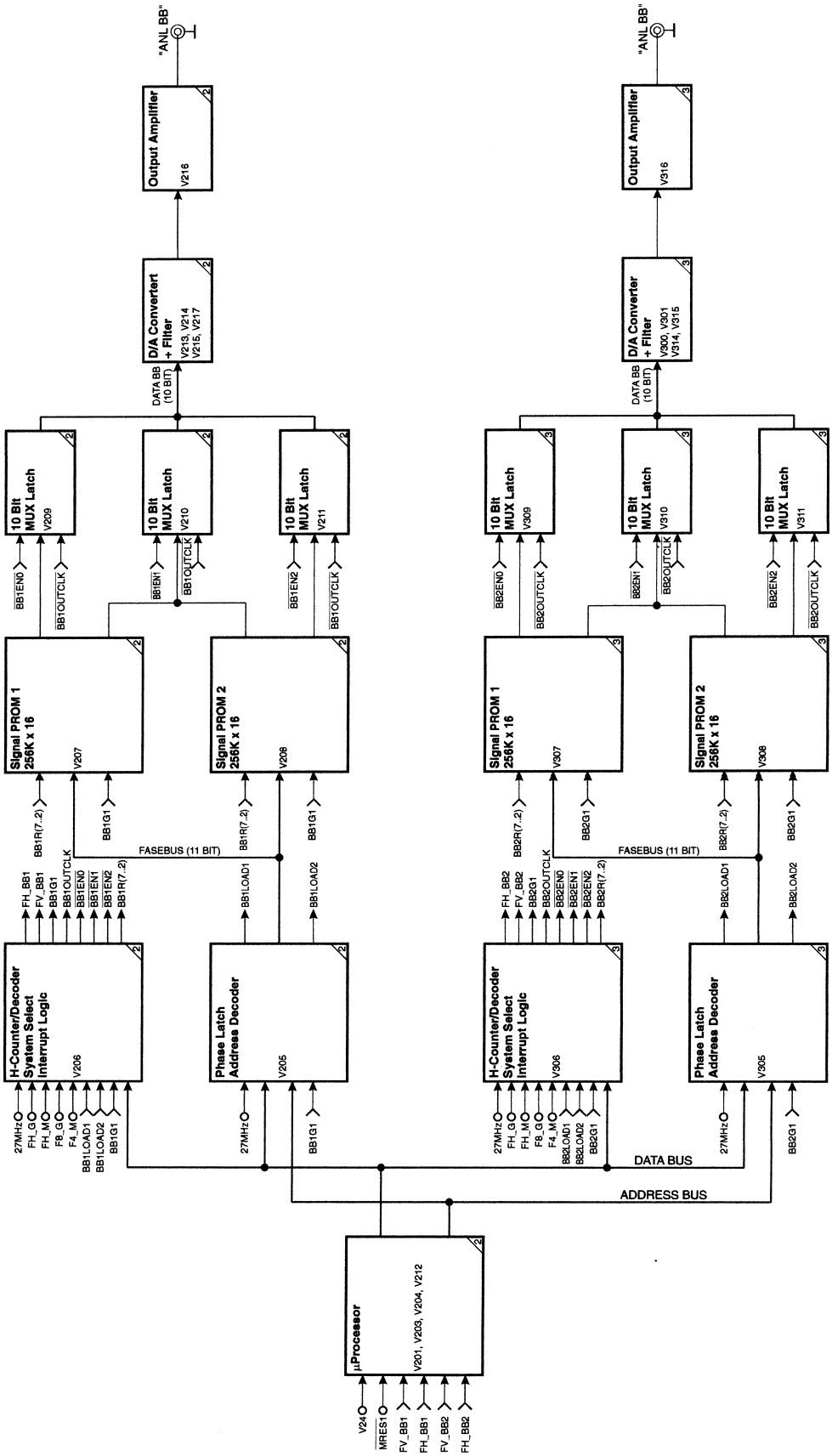
There are 2 sets of outputs pulses:

- One for PAL-G
- One for NTSC

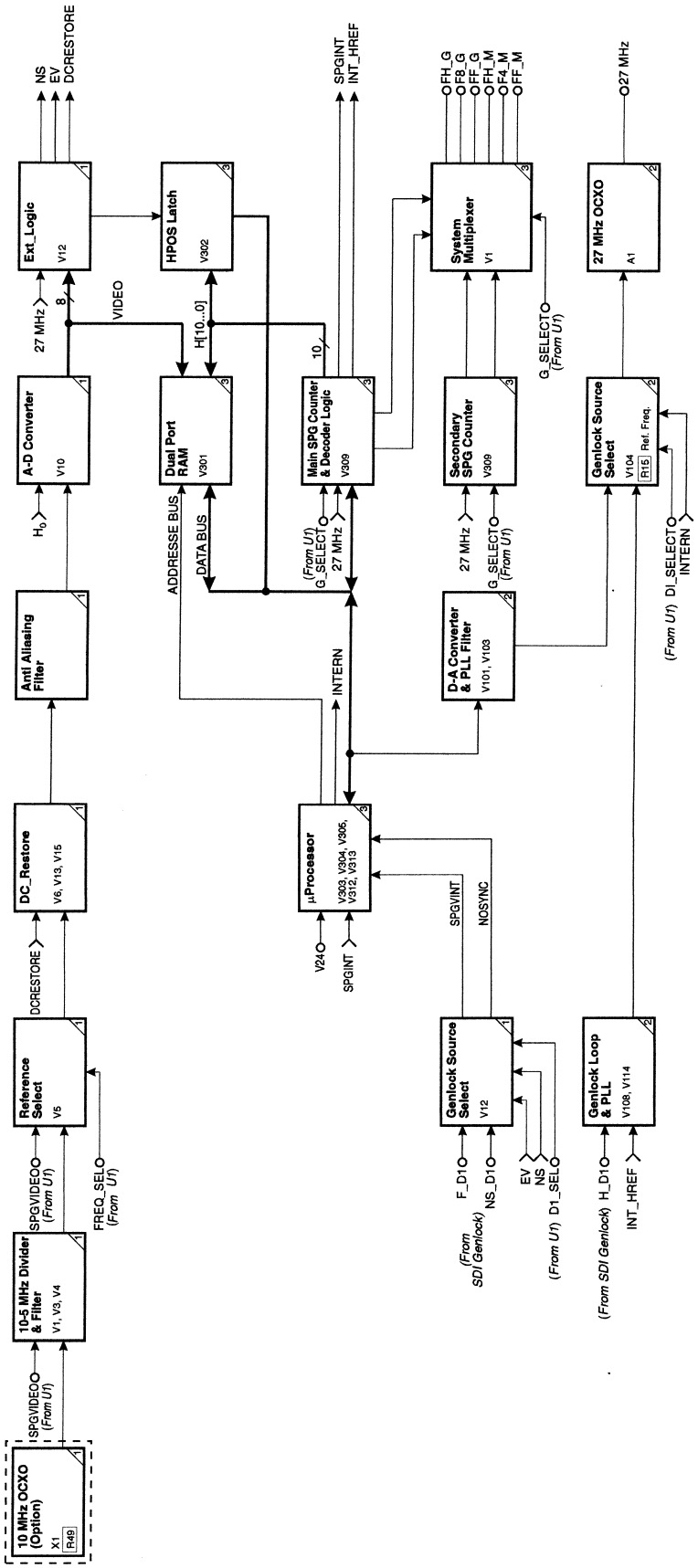
When locked to an external reference, the μProcessor controls the OCXO via a D/A Converter (V101) and PPL Filter (V103).

Optionally it is a possibility to genlock to a D1 digital video input “SDI GENLOCK IN” via SDI Digital Genlock (PT 8606).

For a full size Block Diagram, please refer to Section 2



For a full size Block Diagram, please refer to Section 2



4 Performance Check – PT 5230

Test Equipment:

Video level meter:	e.g. VM 700
Waveform Monitor:/	
Vectorscope, SC-H	e.g. PM 5662
Oscilloscope	e.g. PM 3094
Counter:	e.g. HP 53132

(accuracy better than 0.1 ppm)

4.1 Main Board – Unit 1

4.1.1 Analog Black Burst

This performance check should be performed at **all** analog black burst outputs at the instrument.

PAL G System:

- Using menu select:
- ANALOG-BLACK / BB1 / SYSTEM / PAL w/PAL ID
- Using Video Level Meter, check that the sync amplitude is 300 mV ± 6 mV
- Using Waveform monitor/Vectorscope, check that the burst amplitude is 300 mV ± 6 mV
- If necessary, adjust the burst amplitude at C203 on channel 1, 3, 5, and 7 or at C303 on channel 2, 4, 6, and 8

- Using Wave monitor/Vectorscope, check that the SC-H phase is $0^o \pm 5^o$
- Using oscilloscope, check that the DC voltage on the blanking level is 0 mV ± 20mV
- Using Waveform Monitor/Vectorscope, check that there is a white pulse on line 7

NTSC System:

- Using menu select:
- ANALOG-BLACK / BB1 / SYSTEM / NTSC
- Using Video Level Meter, check that the sync amplitude is 286 mV ± 6 mV
- Using Waveform monitor/Vectorscope, check that the burst amplitude is 286 mV ± 6 mV
- Using Wave monitor/Vectorscope, check that the SC-H phase is $0^o \pm 5^o$
- Using oscilloscope, check that the DC voltage on the blanking level is 0 mV ± 20 mV
- Using Waveform Monitor/Vectorscope, check that the signal contains set-up

Timing check

The following description applies to instruments in which all timings are set to zero, at the black burst out as well as on genlock timings. When this is not practical – for example, if you are checking an instrument which has been adjusted for a certain application – you will have to compensate for the instrument setting.

PAL G System:

- Using menu select:
  GENLOCK / A-B PAL Burst
- Genlock the PT 5210 to a PAL G video signal at “ANALOG GENLOCK A” input
- Connect the “ANALOG GENLOCK B” input from the PT 5230 to the B input of Waveform monitor/Vectorscope
- Connect the “ANL BB” output to the A input of the Waveform monitor/Vectorscope
- Connect the “GENLOCK MONITOR” output from the PT 5230 to the external sync input of the Waveform monitor/Vectorscope
- Check that the line syncs have the same timing (±2 nsec)
- Check that the filed syncs have the same timing (±0 line)
- Check that the bursts have the same phase (±2°)

NTSC System:

- Using menu select:
  GENLOCK / A-B NTSC Burst
- Genlock the PT 5210 to a NTSC video signal at “ANALOG GENLOCK A” input
- Connect the “ANALOG GENLOCK B” input from the PT 5230 to the B input of Waveform monitor/Vectorscope
- Connect the “ANL BB” output to the A input of the Waveform monitor/Vectorscope
- Connect the “GENLOCK MONITOR” output from the PT 5210 to the external sync input of the Waveform monitor/Vectorscope
- Check that the line syncs have the same timing (±2 nsec)
- Check that the filed syncs have the same timing (±0 line)
- Check that the bursts have the same phase (±2°)

4.1.2 Changeover Control

- Leave every output unterminated
- Switch the instrument off and on
- Then press the ▲ button
- The display should read:
  PT 5230 ERROR/WARNING STATUS
  NO ACTIVE WARNINGS
- Terminate the analog black burst (“ANL BB”) output one by one with 3 x 75 ohm termination in parallel (25 Ω)
- The following message should appear in the display:
- *GENLOCK: A*
  E[001]: LEVEL ERROR AT BBX
  for each output when it is terminated with 25 Ω

4.2 Sync Generator – Unit 2

PAL G genlock

- Using menu select:
  GENLOCK / SYSTEM /PAL Burst
- Connect PAL G signal to the “ANALOG GENLOCK” input
- Check that the PT 5230 remains locked when you vary the input signal amplitude by ±3 dB
- Check that the PT 5230 remains locked, even with 1 Vpp hum in the input signal
- Check that the PT 5230 remains locked, even with 30 dB noise in the input signal

NTSC genlock

- Using menu select:
  GENLOCK / SYSTEM /NTSC Burst
- Connect NTSC signal to the “ANALOG GENLOCK” input
- Check that the PT 5230 remains locked when you vary the input signal amplitude by ±3 dB
- Check that the PT 5230 remains locked, even with 1 Vpp hum in the input signal
- Check that the PT 5230 remains locked, even with 30 dB noise in the input signal

Frequency lock 10 MHz

- Using menu select:
  GENLOCK / SYSTEM /10 MHz
- Connect a 10 MHz 1 Vpp signal to the “ANALOG GENLOCK” input
- Check that the PT 5230 remains locked when you vary the input signal amplitude by ±3 dB

Frequency lock 5 MHz

- Using menu select:
  GENLOCK / SYSTEM / 5 MHz
- Connect a 5 MHz 1 Vpp signal to the “ANALOG GENLOCK” input
- Check that the PT 5230 remains locked when you vary the input signal amplitude by ±3 dB

Frequency lock 4.43 MHz

- Using menu select:
  GENLOCK / SYSTEM /10 MHz
- Connect a 4.43 MHz 1 Vpp signal to the “ANALOG GENLOCK” input
- Check that the PT 5230 remains locked when you vary the input signal amplitude by ±3 dB

Frequency lock 3.58 MHz

- Using menu select:
  GENLOCK / SYSTEM /3.58 MHz
- Connect a 3.58 MHz 1 Vpp signal to the “ANALOG GENLOCK” input
- Check that the PT 5230 remains locked when you vary the input signal amplitude by ±3 dB

Internal frequency reference

- Make sure that the instrument is warmed up (1 hour)
- Select internal reference
  GENLOCK / Internal
- Connect a counter to TP08
- The frequency should be 27 MHz ± 1 ppm
- If necessary, adjust R15

5 Service Hints

5.1 Maintenance

5.1.1 Cabinet

The cabinet can be cleaned with a mild detergent and water. If necessary, a fine scouring detergent may be used.

5.2 Repairs

Our recommended of repair of the instrument, PT 5230 and PT 86XX, is to replace the faulty unit with a new one, i.e. keep normal repair on a PCB board level.

We recommend this method because:
1. SMD components are used
2. The units are factory software adjusted

Thanks to the individual software adjustment of the PCB units, they can be replaced freely with new units in service situations.

Note:
The Main board (Unit 1) and Sync Generator Board (Unit 2), however, are factory adjusted in pairs to obtain maximum timing accuracy between Genlock Input and Outputs.

List of error and warning messages can be found in Appendix A.

If the instrument has to be sent to PTV for repair/or alignment, the following points should be noted:

1. Attach a label to the instrument stating the address of the sender and describing the fault(s) and complaint(s) as clearly as possible.

2. Use the original shipping carton and padding materials (if still available) or pack the instrument, wrapped in a plastic bag, in a rigid box with filling materials in order to avoid transport damage.

3. The box should be marked with the complete type- and serial number (KU.Number) and the remark “Return-shipment for repair”.

6 Chapter reserved for future use

7 SDI Digital Genlock – PT 8606

7.1 General Information

SDI genlock unit consists of:

- A cable Equaliser
- An Output Buffer
- A Serial-to-Parallel Converter
- An H / V Pulse Detector.

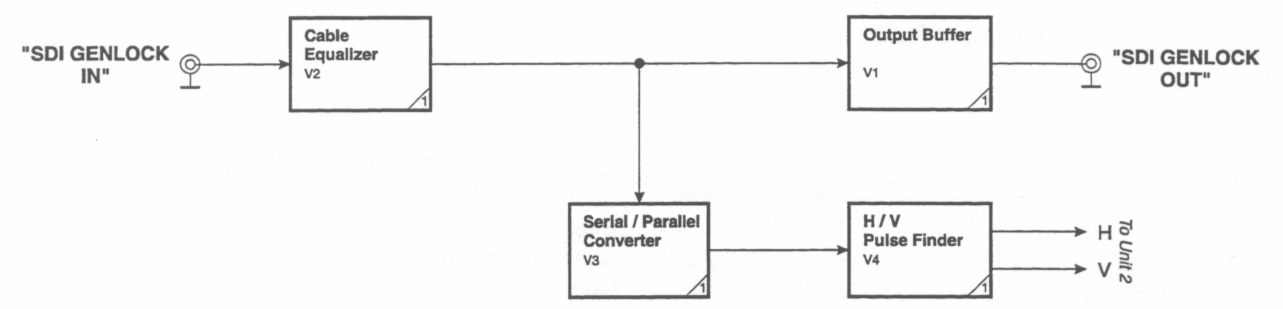


Fig. 10-1 Block Diagram - PT 8606

7.2 Test and Adjustments

7.2.1 Performance Check

- Using menu select:
  GENLOCK / INPUT / SYSTEM / 625/50
- Connect an SDI 625/50 signal to the "SDI GENLOCK IN" input
- Check that the signal comes out at the output (active loop trough)
- Using menu select:
  SDI-TSGx / SYSTEM /625/50 or SDI-TPGx / SYSTEM / 625/50
- Check that the output of the PT 5230 is in phase with the incoming signal

- Using menu select:
  GENLOCK / INPUT / SYSTEM / 525/59.94
- Connect an SDI 525/59.94 signal to the "SDI GENLOCK IN" input
- Check that the signal comes out at the output (active loop through)
- Using menu select:
  SDI-TSGx / SYSTEM /525/59.94 or SDI-TPGx / SYSTEM / 525/59.94
- Check that the output of the PT 5230 is in phase with the incoming signal

7.2.2 Adjustment

- Connect an SDI signal to the "SDI GENLOCK IN" input
- Monitor the voltage at TP 1
- Tune R6 first so that the PPL loses lock at the low end (lowest loop voltage)
- Then slowly increase the voltage to determine the error-free low limit of the capture range
- Use a suitable CRC or EDH measurement method to determine error-free operation
- Record the loop voltage at the point, then adjust R6 so that the voltage is 250 mV above

8 Analog Test Signal Generator – PT 8631

8.1 General Information

PT 8631 is a signal board video generator. From a clock, line and frame pulse, it generates a complete composite signal, which can be time shifted.

It consists of:
- A μController
- A 13.5 MHz *Numerically Controlled Oscillator* (NCO)
- A Video Generator
- A Composite Modulator
- DAC with Lowpass (anti-aliasing) Filter
- An Output amplifier

The output is monitored by a Level Detector that sets off an alarm if the output amplitude is too low or too high.

The μController circuit consists of:
- A μController (V50)
- A program PROM
- An Address-Latch
- An E^2-PROM containing calibration data

The signal selected can be time adjusted ±4 fields (PAL) or ±2 field (NTSC) with a resolution of $1/(27x10^6x256)$ second, equals approx. 0.14ns. The Sc-H phase of the resulting signal can be adjusted. Up to 3 lines with 16 characters can be written in the generated pattern. The text placement has several options, i.e. fixed in lower left-hand corner or free placed on the screen. For Philips or FuBK pattern text can be placed default in the black areas of the pattern.

The μController interfaces with the Master Controller on Main Board via a two-wire serial bus and reset wire. The video part of the generator is controlled by a clock signal and, for each system (PAL and NTSC), a line pulse (PAL: FH_G, NTSC: FH_M) and a colour framing pulse. Colour framing for PAL/NTSC is 2500/1050 lines between each pulse (PAL: F8_G; NTSC: F4_M).

When the power is switched on, the Master Controller detects presence of an Analog Test Signal Generator. When detected, the generator receives information on:
- Which system to generate
- Pattern
- Text
- Timing

When this information is received, NCO and Subcarrier oscillator are initialised, according to the system selected. Text - data are stored in Dual Port RAM (V56). Finally, a 10-bit word is written to H-OFFSET PORT. This word is the sample offset between incoming and generated line pulses. Line and field offsets are generated by the μController, see below.

8.2 Block Diagram Description

8.2.1 NCO

The incoming clock is doubled to 54 MHz; this clock feeds the NCO. After RESET the NCO is loaded with data that will generate a 13.5 MHz sine wave. The phase of this 13,5 MHz sine is programmable and is used to generate timing offsets of less than a clock period for the resulting video signal. Output from the NCO circuit (V46) is a 10-bit sine wave. This is converted to an analog voltage by V47 and V58. After bandpass filtering, (L1 and C4/C5, (this sine wave is converted to a 13,5 MHz square wave by V48-B. V49 is a clock buffer that drives the rest of the generator.

8.2.2 H-Counter

This is a 10-bit counter running at 13,5 MHz. It is loaded with a 10-bit number which enables it to be offset from the incoming line pulse (SYS_H). The H-counter is used to address the Video Line Generator and Text Generator.

8.2.3 Line Type Register and Video Line Generator

A video pattern is made up of a number of lines. The address for these lines is written to Line Type Register. A new number is written by the µController each line if it is necessary, i.e. if a line different from the previous line is needed. Line type is 1 0-bits wide. First upper part is written to 8 MSB-DATA (V55), then 8 LSBs are written together with 2 MSBs to V61. Output from µController is synchronised to video line in V62. Each line consists of segments; each segment is 32 samples. The Line Type Register and the upper five bits from H-Counter address the Segment Address PROM (V64). Output from this PROM address segment data PROMs (V65, V66, V67, and V68) producing a 32-bit word representing 12-bit Y (luminance) samples, 10-bit U samples and 10-bit V samples.

8.2.4 Status Port

Additional information is needed for each line:

- Two bits are used to generate half-lines and lines without burst (PAL only)
- One bit is used to indicate which system to generate (PAL-G or NTSC)
- Three bits are used to indicate if text should be added to the pattern
- One bit is used to indicate Field 1 or Field 2
- One bit is used to indicate Line 1 (of 2500 in PAL-G, of 1050 in NTSC) and to reset the colour framing

8.2.5 Text Generator

In lines with text added to the pattern, one or more of the text bits in STATUS PORT are set high. This starts a text line counter (4 bits) in V54 and addresses a text row in Dual Port RAM (V56). From H-Counter seven bits address the horizontal text row. The output from the RAM is a character. This character is used to address a PROM (V68) where the waveshape is stored. Three bits from the H-Counter, four bits from the text line counter and one bit indicating Field 2, make up the actual text amplitude at the PROM output.

8.2.6 Test Inserter

The 32 bits from the Video Line Generator and the eight bits from text PROM are fed into the Text Inserter (V70 & V71). Seven of these eight text bits are added to the luminance signal, and when TXT7 is high, Y, U, and V are blanked.

8.2.7 Subcarrier

The subcarrier frequency is generated in Subcarrier Oscillator (V9). This is a 32-bit NCO with a 12-bit sinus and 12-bit cosine output. After RESET a 32-bit value indicating subcarrier frequency and a 11-bit value indicating Sc-H phase are written to V9.

Writing the 32-bit value is a four step process. First, the eight MSBs of the 16 low bits are written to 8 MSB-DATA (V55), and then eight LSBs of the 16 low bits are written, together with the bits from V55, to V9 in an address given by A_0 to A_2. The same process is repeated for the 16 high bits. The same process is again repeated for the 11 Sc-H phase bits. These values are only changed if the system or Sc-H phase are changed. This is done from the front plate or remote interface.

The Subcarrier Modulator (V8) multiplies U and the cosine from V9 and multiplies V with the sinus from V9; both values are then added to the resulting chrominance signal. Also Y from the Text Inserter is added to the chrominance signal.

8.2.8 D/A Converter

The D/A Converter receives 12 bits, representing the complete composite video signal, come from the Subcarrier Modulator (V8). These bits are converted into an analog current by V10, this current is then converted to a voltage by V11. The resulting amplitude can be adjusted from the μController via V17.

8.2.9 Lowpass Filter

The Lowpass Filter, or Anti - aliasing Filter, is a conventional LC-filter with a delay equaliser. It has a pass band at 5.8 MHz. After lowpass filtering, the signal is fed to the Output Amplifier, which also performs the necessary Sinx/x correction.

The blanking level can be adjusted from the μController via V17.

8.2.10 Level Detector

At the output BNC (after the output resistor) the signal is fed to a Buffer (V13-A). The chroma part is removed (L23/C77) and the resulting luminance signal is amplified by the Inverting Amplifier (V13-B). The correct signal level is detected from the sync part.

If the signal is OK, the multivibrator (V3-A) is triggered through V14-A, holding XA1 pin 5 'SYNC OK' high. If the SYNC is too low V3-A is not triggered and output goes low. If the SYNC for some reason is too high, the multivibrator (V3-A) is cleared through V14-B and then XA1-pin 5 goes low.

8.3 Test and Adjustments

Test Equipment

Video Level Meter:	e.g. VM 700
Waveform Monitor/Vectorscope, Sc-H:	e.g. PM 5661/70
Oscilloscope:	e.g. PM 3094
Network Analyser:	e.g. HP3577A

8.3.1 Performance Check

Check NCO part:

- Connect an oscilloscope probe to TP94.
- Check that the amplitude of the 13.5 MHz sine wave is approximately 1.2 V_{PP}
  It has a DC-offset of 2.5V

- **Check video level and blanking level:**
- Select system PAL (625/50) ANALOG-TPGx SYSTEM / PAL
  and EBU C.bar
  ANALOG-TPGx/PATTERN/EBU C.Bar
- Connect the "ANL TPGx" connector to an oscilloscope
- Measure blanking level: it must be 0 V ±20 mV
- Connect the "ANL TPGx" connector to a video level meter
- Select colour bar signal
  ANL-TPGx / PATTERN / EBU C. Bar
- Measure white bar level: it must be 700 mV ±7 mV

Lowpass Filter check:

- Select system PAL (625/50)
  ANL-TPGx / SYSTEM / PAL
- Connect the "ANL TPG" connector to network analyser input
- Select multiburst signal
  ANL-TPGx / PATTERN / CCIR18
- Check, that frequencies 0.5, 1, 2, 4, and 4.8 MHz are within 1 % and 5.8MHz is within 2% of reference level

Timing check:

The following description applies to instruments in which all timings are set to zero, at the black burst output as well as on genlock timings. When this is not practical - for example, if you are checking an instrument which has been adjusted for a certain application - you will have to compensate for the instrument setting.

PAL G System:

- Using menu select: GENLOCK / A-B PAL Burst
- Genlock the PT 5230 to a PAL G video signal at "ANALOG GENLOCK A" input
- Connect the "ANALOG GENLOCK B" input from the PT 5230 to the B input of Waveform monitor/ Vectorscope
- Connect the "ANL TPGx" output to the A input of the Waveform monitor/Vectorscope
- Connect the "GENLOCK MONITOR" output from the PT 5230 to the external sync input of the Waveform monitor/Vectorscope
- Check that the line syncs have the same timing (± 2nsec)
- Check that the field syncs have the same timing (± 0line)
- Check that the bursts have the same phase (± 2°)

NTSC System:

- Using menu select:
  GENLOCK / A-B NTSC Burst
- Genlock the PT 5230 to a NTSC video signal at "ANALOG GENLOCK A" input
- Connect the "ANALOG GENLOCK B" input from the PT 5230 to the B input of Waveform monitor/ Vectorscope
- Connect the "ANL TPGx" output to the A input of the Waveform monitor/Vectorscope
- Connect the "GENLOCK MONITOR" output from the PT 5230 to the external sync input of the Waveform monitor/Vectorscope
- Check that the line syncs have the same timing (±2 nsec)
- Check that the field syncs have the same timing (±0 line)
- Check that the bursts have the same phase ($\pm 2^0$)
-

8.3.2 Adjustments

All adjustments at this unit are factory adjustments.

9 SDI Test Pattern Generators, PT 8632 & 8633

9.1 General Information

PT 8632 and PT 8633 are single board digital video generators. They differ mainly in the available pattern possibilities. Even though they have separate diagrams and printed circuits boards, the circuits are almost identically. Therefore this description covers both options.

From a clock, line and frame- pulse they generate a complete serial digital video signal, which can be time shifted.

Sound with different levels and frequencies can be embedded in the signal.

Error Data Handling (EDH) codes can be calculated and inserted into the signal.

A text generator can generate and insert up to 3 lines with 16 characters in the pattern. Text is inserted in the lower right-hand corner of the screen. In Philips and FuBK patterns two rows of text are available. Date and clock can be inserted in the signal when Time Clock Interface, PT 8637, is mounted (all patterns).

The units have two equal SDI outputs each. The outputs are monitored by a Level Detector that sets off an alarm if the signal for some reason disappears.

The selected signal can be time adjusted ±1 field (totally 625 lines or 525 lines) with a resolution of 1/27 µsec ≅ 37 nsec.

9.2 Block Diagram Description

9.2.1 SDI Test Signal Controller

This unit is controlled by a µController. The µController interfaces with the Master Controller on the Main Board via a two-wire serial bus and a reset wire.

The µController circuit consists of:

- a µController (V50)
- a program PROM
- an Address Latch
- an EEPROM containing calibration data.

The video part of the generator is controlled by a clock signal and, for each system (625 line and 525 line), a line pulse (625 line: FH_G; 525 line: FH_M) and a colour framing pulse. Colour framing for 625 line/525 line systems is 2500/1050 lines between each pulse (625 line: F8_G; 525 line: F4_M).

When power is switched on, the Master Controller detects presence of the SDI Test Signal Generator. When detected, the unit receives information on:

- which system to generate
- pattern
- text
- sound status

(frequency and amplitude)
- EDH on/off
- timing
- sound group number (PT 8633 only)

When this information is received, text data are stored in Dual Port RAM (V59), sound data (if needed) are stored in RAM circuits (V56 & V57). When writing to the RAM, the PS-bit (V50, pin 6) is high, otherwise is low. Finally, an 11-bit word is written to the H-OFFSET PORT. This word is the sample offset between incoming and generated line pulses. The line and field offsets are generated by the μController, see below.

9.2.2 Video Generator

A video pattern is made up of a number of lines. The sequence of lines is calculated by the μController from timing information and the VINT and HINT interrupts. The address to these lines is written to the Line Type Register. A new number is written by the μController for each line if it is necessary, i.e. if a line different from the previous line is needed. The line type is 16 bits wide: the first upper part is written to the 8 MSB-DATA (V66), and then 8 LSBs are written to V65. The output from the μController is synchronised to the video line in 16 bit register (V67 and V68).

Each line consists of 32 segments; each segment is 32 samples. A horizontal counter (H-Counter) in V63 counts each line up to 1727 (625 line) or 1715 (525 line). Outputs are H0 to H10. Line type register and upper 5 bits from H-Counter addresses the segment address PROM (V69). Output from this PROM addresses segment Data PROMs (PT 8632: V79, V80, and V81; PT 8633: V87, V88, and V89), producing a 20-bit word representing 10-bit Y (luminance) samples and multiplexed 10-bit U and V samples.

9.2.3 Status Port

Additional information is needed for each line:
- two bits (S0 and S1) are used to start the Text Generator
- one bit (SYSSEL) is used to indicate which system to generate (625/50 or 525/59.95)
- two bits (SOUND and 3OR4) are used to handle the sound generator
- one bit (F2) is used to indicate Field 1 or Field 2.
- one bit is used to disable the EDH-insertion.

9.2.4 Text Generator

In lines with text added to the pattern, one or both of the text bits in STATUS PORT are set high. This start a text line counter (four bits) in V63 and addresses a text row in the Dual Port RAM (V59). From the H-Counter seven bits address the horizontal text row. The output from the RAM is a character. This character is used to address a PROM (V64) where the waveshape is stored. Three bits from the H-Counter, four bits from the Text Line Counter and one bit indicating Field 2, make up the actual text amplitude at the PROM output.

9.2.5 Sound Generator

Sound data are stored in RAM and addressed by the Sound Address Counter in V63. When a new level or sound function is selected, new sound data for the new selection are stored in RAM (V56/V57) by the μController.

When 3OR4 (V73, pin 12) is low, three sound samples for each of the four channels are inserted. When 3OR4 is high, four samples are inserted. When no sound is to be inserted, SOUND-bit (V73 pin 13) is low. In PT 8633 two bits (GR0 and GR1) from V54 selects the audio group.

9.2.6 Data Multiplexer / Sound Inserter

V75 has four functions:

- it blanks luminance and chroma- data when text is to be inserted;
- it adds text to the luminance data;
- it multiplexes luminance and chroma- data;
- it inserts sound into the 10-bit data stream.

When TXT7 is high, luminance and chroma- data are blanked. Text (7 lower bits from the text PROM) is always added to luminance data. After the Text Adder luminance and chroma- data are multiplexed together. Sound is then inserted in this data stream. According to the 5 Sound Status Bits framing codes, group identification (group code), sound data or checksum is inserted.

The checksum is calculated for every line with sound insertions.

9.2.7 EDH Inserter

At the output of V75, (pin 21 to 9 [PI9..PI0]) a correct 10-bit SDI parallel signal is present. These ten bits are clocked into the EDH Inserter (V82). This circuit calculates and inserts EDH codes in to the data stream. Insertion takes place when EDH bit (V73, pin 15) is low. When the EDH bit is high, data are clocked through without modification.

9.2.8 Parallel-to-Serial Converter

The ten bits are serialised in V76. Output from this circuit feeds the Output Amplifier (V77). This amplifier contains two amplifiers which drive two output BNC - connectors. Signals at these connectors are identical but independent of each other.

9.2.9 Level Detector

The Level Detector is connected, via two transformers (TR1 and TR2), directly to the output BNCs.

Signals from the TR1 Transformer are rectified by D201 and V201A, then lowpass-filtered and amplified by V201B. This provides a almost DC-voltage at TP201/TP205 of -1.3V when the signal is correct (output open or terminated). This voltage keeps TP202 and XA1-pin 5 high. If signal at the BNC - connector vanishes, e.g. if the amplifier is not working, the DC - voltage increases to 0V. Then V203B takes TP202 and XA1-pin 5 low, indicating an error. TR2, V211, V213, and XA1-pin 6 has a similar function.

9.2.10 Test Pins

These two pins could be used to indicate whether or not V76 locks or has a chance to lock properly onto incoming data stream.

TP5:
At this pin is a 27MHz clock signal which is regenerated from incoming video data. This clock is 0.8V centred around 2.5V and indicates whether or not the serialised (V76) is able onto lock to incoming data.

TP6:
This pin is low when the data words (00.xHex and FF.x_{Hex}) are received; otherwise it is high. In patterns without sound or EDH codes, there will be two low pulses in each line. These pulses indicate EAV and SAV.

9.3 Test and Adjustments

Test Equipment:

Digital Video Analyser	:
Digital Video Component Analyser	: e.g. R&S VCA
Picture Monitor w. SDI input	:

9.3.1 Performance Check

To perform a performance check, you need an instrument that is able to measure following parameters:

- TRS - errors
- jitter
- serial video amplitude
- video level (digital information)
- sound detection (preferable an instrument that can convert the sound information to analog sound)
- The instrument must also be able to calculate EDH-codes.

In system 625/50 check as follows:

- The generator should be internally locked

Using the menu select:
GENLOCK / Internal.

- Using the menu select:

SDI-TPGx / SYSTEM / 625/50

- Connect the “SDI-TPGx” output to the measuring device.
- Select a black signal without sound:

SDI-TPGx / PATTERN / Black
SDI-TPGx / EMB.AUDIO-LEVEL / Silence
and EDH-codes
SDI-TPGx / EDH / Off

- Look for TRS-errors: there should not be any.
- Measure jitter: it must be <0.15 UI. Measure over 4 frames without lowpass-filtering.
- Measure level of serial video: it must be 800mV ±80mV.
- Select the 75% colour bar signal.

SDI-TPGx / PATTERN / EBU C.Bar.

Check the white level: it must be 235.00d.
Using the waveform display, check for waveform errors.

- Step through the available patterns.

Using the waveform display, check for waveform errors.

- Select colour bar signal.

Switch 3 text lines On.

- Using the digital pattern monitor, check that 3 lines of the text are displayed.

Check also, that the text displayed are the same as shown in display.

- Select Philips pattern.

Modify pattern by adding motion
SDI-TPGx / PATTERN/ Philips 4x3 / Modify / Motion ON
Check that the 2T needle in lower text field is scrolling from right to left (Text must be OFF).

- Add sound (silence) to the signal.

SDI-TPGx / EMB.AUDIO-LEVEL / Silence
Make sure sound samples have been added to the SDI-signal.
By converting to analog voltage, you get a good indication of whether there are any bit errors in the signal.

- Check for reserved code errors. Values 00.xHex and FF.xHex must not appear in the data stream except in TRS-words.
- Add EDH-codes to the signal

SDI-TPGx / EDH / On
Check to make sure that the codes are in the
signal and, if possible, whether they have been generated correctly.

- Check level detectors. Connect PP1 of the generator. Watch the display, a message

LEVEL ERROR AT SDI-TPGx
should appear.

In system 525/59.94 check as follows:

- Select system 525/59.94

SDI-TPGx / SYSTEM / 525/59.94

- Look for TRS-errors: there should not be any.
- Select the SMPTE-colour bar signal

SDI-TPGx / PATTERN / SMPTE

- Check the white level: it must be 180.25_d. (line 25).

Output
Connect the other “SDI-TPGx” output to the measuring device, and check the level of the data signal: it should be 800mV ±80mV.

Timing check
The purpose of this check is to verify the output timing to be within ±1 sample period (~37nsec.) when the display shows:
V: +0 H: +000 T: +00000.0.

This check requires the SDI Digital Genlock option, PT 8606, and another SDI Test Pattern Generator. An instrument that can measure the timing difference between two SDI-signals is also necessary.

- Connect a SDI digital signal to “SDI GENLOCK IN” input.
- Using menu select:

GENLOCK / SDI PAL Burst

- Compare the output from SDI Digital Genlock option at “SDI GENLOCK OUT” to the output from SDI Test Pattern Generator at “SDI-TPGx”, the timing should be the same as the reference generator.

9.3.2 Adjustments

There are no adjustments in this unit.

10 AES/EBU Audio Generator - PT 8635

10.1 General Information

The purpose of the audio generator is to generate digital audio as defined in the AES3-1992 standard.
The generator board contains two independent audio generators with the same performances.

The generator consists mainly of five parts:

1) Phase Locked Loop (PLL)
2) PROMs with audio data
3) Video audio timing control
4) Output drivers for the XLR and BNC connectors and the Word Clock outputs.
5) Level detectors for the six outputs.

10.2 Block Diagram Description

10.2.1 Phase Locked Loop

The purpose of the PLL is to convert the 27MHz reference clock to 6.144MHz, which is the clock for the Audio Generator. The 27MHz ref. clock is divided by 2250 into 12kHz, which is the reference to the phase comparator in V2. The VCO frequency of 6.144MHz is divided by 512, into 12kHz, which is the input to the Phase Comparator.

The output from the Phase Comparator is fed to the Lowpass Filter (V3), which controls the VCO (V4). The two dividers are implemented in the PLD (V9).

The VCO control voltage can be measured at TP1, and the 6.144MHz clock can be measured at TP2. When the PLL is locked, the 27MLOCK signal is logic “1” and D3 is on.

10.2.2 PROMs with Audio Data

The PROMs (V6 / V7) contains the audio data, which will be converted into serial data in the PLD (V9) and then sent to the XLR Output Drivers
(V25 / V26), the BNC Output Drivers
(V27,V28 / V27,V29) and the Word Clock Output Drivers (V30 / V31).
The audio signals and levels are selected by setting the I^2C-ports (V10 / V12)

10.2.3 Video-audio Timing Control

This function is implemented in the PLD (V9). The timing is selected by setting the I^2C-port V11/V13. The timing only relates to the audio sample timing (audio sample = 20.83µs), not the audio block timing (audio block = 4ms). When the video-audio timing is correct, the VIDLOCK signals are logic “1” and D5/D4 are on.

The Audio Generator timing is fixed to the PT 5230 synchronisation bus as timing reference. Since the analog video generator outputs can be freely time shifted relative to the very same reference please note: the timing between digital audio and analog video outputs will be at the nominal value only when the analog video timing is set to zero.

The audio-video timing for PAL is described in EBU Recommendation R83-1996, and the audio-video timing for NTSC is described in SPMTE Recommended Practice S17.401 (1994).

10.2.4 Output Drivers for XLR and BNC Connectors

The drivers for the XLR connectors consist of a RS422 driver in V25 / V26 followed by a pulse transformer to obtain a balanced output. The output impedance is 110Ω.

The drivers for the BNC connectors consist of a RS422 driver in V27 followed by a video amplifier in V28 / V29 to obtain an output impedance of 75Ω.

The drivers for the Word Clock BNC connectors consist of a HCMOS buffer (V30 / V31) followed by resistors to obtain an output impedance of 75Ω.

10.2.5 Output Level Detectors

The detectors (see sheet 3) consist of a window comparator followed by a one-shot. The reference levels for the comparators are set individually for the XLR, BNC and the Word Clock outputs.
The six detector outputs are connected to the AND-gate in V21, and to the I^2C-ports V11 and V13. This enables the master processor to monitor the six level detectors.
The level detectors can be disabled by mounting jumpers in PP4.

10.3 Test and Adjustment

Test Equipment:

Oscilloscope	e.g. PM3094
Digital Audio Monitor	e.g. TEK764
Multimeter	e.g. HP34401
Counter	e.g. HP53132 *)

*) accuracy better than 0.1 ppm

10.3.1 Performance Check

Note: The PT8635 AES/EBU Audio Generator consists of two audio generators with the same performances. The performance check described here is the same for both generators.

Connect the AES/EBU Audio connector to the oscilloscope.
Select an AES/EBU audio signal (for example “Stereo 1kHz”) in the menu: AES-EBU / AES-EBUx / SIGNAL / Stereo 1 kHz.

Check the following:

Amplitude on AES/EBU BNC connectors:
0.9 - 1.1 Vpp (75Ω).
Rise/fall time:
30 - 44 nsec (10%-90%).
DC level:
0 ± 0.05 V.

Amplitude on AES/EBU XLR connectors:
2.5 - 3.5 Vpp (110Ω).
Rise/fall time:
10 - 30 nsec (10%-90%).
DC level:
0 ± 0.05 V.

Amplitude on Word Clock BNC connectors:
High level:≥2.3 V (75Ω).
High level: ≥ 4.5 V (unterminated).
Low level: <0.1 V (75Ω).
Rise/fall time:
20 - 50 nsec (10%-90%).
Frequency:
48 kHz.

Connect the AES/EBU Audio connector to the Digital Audio Monitor. Select an AES/EBU audio signal (for example “Stereo 1kHz”) in the menu:
AES-EBU / AES-EBUx / SIGNAL / Stereo 1 kHz.

Check the following:

Audio levels:
Silence, -20, -18, -16, -15, -12, -9, 0 dBFS
(on channel 1 and 2).
Use following menu to select audio levels:
AES-EBU / AES-EBUx / LEVEL

Audio signals:
Stereo 800 Hz, Stereo 1 kHz, Stereo EBU 1kHz, Stereo BBC 1 kHz, Mono EBU 1 kHz, Mono BBC 1 kHz, and Dual 1kHz/400 Hz.
Check that the Block CRC is valid.
Check that the channel status bit shifts between stereo, monaural and 2-channel when you select the audio signals.

The analog audio signals are output to the headphone connector on the front of the Digital Audio Monitor.

Use following menu to select audio signals:
AES-EBU / AES-EBUx / SIGNAL.

Audio/video timing:
PAL phase, NTSC phases 1 to 5.

When the analog video and digital audio are in phase, the LED D4 on the AES/EBU audio board is ON.

Use following menu to select audio timing:
AES-EBU / AES-EBUx / TIMING.

Word clock (48 kHz ref):
Check that a 48 kHz, 50% duty cycle signal is output when “Word-clock” is selected in the menu AES-EBU / AES-EBUx / SIGNAL.

Phase Locked Loop (27 MHz / 6.144 MHz):
Check that the LED D3 on the AES/EBU Audio Generator board is ON.
Check the voltage at TP1: 0 ± 3 VDC
Check the frequency at TP2: 6.144 MHz ± 7 Hz **)

***) The frequency obtained depends on the accuracy of the 27 MHz ref clock or the accuracy of the genlock signal.*

Output Level Detectors
Terminate the XLR output with
>75Ω: OK
<30Ω: Display: Level error at AES XLR #x

Terminate the BNC output with
>56Ω: OK
<30Ω: Display: Level error at AES BNC #x

Terminate the Word Clock BNC output with 0Ω:
Display: Level error at AES WORD #x

10.3.2 Adjustments

There are no adjustments.

11 Time Clock Interface - PT 8637

11.1 General Information

The purpose of the Time Clock Interface is to read VITC time code, LTC time code and 1 Hz pulses and output the read time on different test patterns including the Philips and FuBK test pattern.

A positive or negative time offset between the read time and the output time can be selected by the user.

The option consists mainly of six parts:

- 1) VITC reader and decoder
- 2) LTC reader and decoder
- 3) 1 Hz reader
- 4) Real Time Clock (RTC)
- 5) EEPROM
- 6) LTC/1 Hz detector

A microcontroller controls the readers and the RTC and communicates with the master processor on the main board via an I²C-bus interface (V3).

11.2 Block Diagram Description

11.2.1 VITC reader and decoder

The VITC code resides in two non-adjacent lines in the vertical interval between two picture fields. A code line consists of a binary signal of 90 bits. There are 9 words of 8 bits each: the last word is a *Cyclic Redundancy Check* (CRC) code. Two synchronization bits leading each word account for the remaining bits.

The video signal is fed to the Input Clamp and Slicer, which extracts the binary data from the video line. A Filter (L2, C34, C35, C37, C39, R35, R38, and R39) attenuates the burst so that it will not exceed the detector threshold (determined by R47, R48).

The microprocessor receives line synchronization signal FH (which is pulse stretched with C6, R16) from which is produces a WINDOW pulse which enables the Start/Stop circuit (PLD V9) and begins the search for VITC data.

In a window, the first pulse on the line will trigger the Start/Stop circuit, and the Clock Divider will start dividing a clock derived from the Crystal Oscillator (14.5MHz). The divided clock will shift the data into the 8+2 bit Shift Register and into the CRC circuit. Of each ten bits, eight bits are stored in a FIFO Register (V10, V11) and the two bits (the synchronization bits) are compared to '10'. The result is clocked by the '90-bit Counter' into the CRC Latch. If the compare fails, the CRC Latch is inhibited.

If the CRC checker has received the correct 90 bits of data during a line, the CRC Latch will tell the microprocessor to stop producing more windows to search in. The microprocessor then reads the VITC data from the FIFO Register.

11.2.2 LTC reader and decoder

The LTC-signal itself is an 80-bit serial binary code that repeats once each frame: 25 Hz on PAL and 29.97 Hz on NTSC. 32 bits are reserved for time information, 32 bits are reserved as user bits and the last 16 bits are a sync pattern used to locate the start of the time code information in the serial stream.
The LTC-signal is fed to the LTC/1Hz input circuit, which converts the balanced LTC-signal into an unbalanced signal LTCIN (TP1). The bi-phased coded LTC-signal is then fed into the LTC-decoder which splits the signal into two signals: LTCDATA and LTCINT. These two signals are then fed into the T0 and T1 pin on the microprocessor via the Signal Selector in the PLD (V9). The microprocessor then reads the LTCDATA on falling edges of the LTCINT-signal, and then locates the sync pattern and decodes the time code information in each frame.

13.2.3 1 Hz reader

The 1 Hz signal is fed to the LTC/1Hz input circuit and via the Signal Selector into the T1 pin on the microprocessor. The microprocessor is then interrupted on every 1 Hz pulse.

13.2.4 Real Time Clock

The RTC (V7) contains a clock circuit, a watch-crystal and a battery as backup, when power is switched off.
When a valid time code (VITC or LTC) is received, the clock circuit is updated with the received time information, but date information is unchanged. The date is only updated when the time passes from 23.59.59 to 00.00.00 or if it is changed by the user.

13.2.5 EEPROM

The EEPROM (V1) contains information about the option: type number, serial number etc.

13.2.6 LTC / 1 Hz detector

The detector monitors the signals from the
LTC / 1 Hz input circuit (TP1). The LTC-detector has a time-out of appr. 3 msec and the 1 Hz-detector has a timeout of appr. 0.5 sec. The two detector signals are fed into the micro controller (V4), via the PLD (V9).

11.3 Test and Adjustment

Test Equipment:

LTC generator	e.g. Horita VG-50 *)
VITC generator	e.g. Horita TG-50 *)
Video generator	e.g. PT5230 or PT5210
1 Hz pulse generator	e.g. Fluke PM5715

*) one version in PAL and one version in NTSC if both video systems are to be checked.

11.3.1 Performance Check

VITC:
Connect the PT5230 ANALOG GENLOCK input to a video signal containing a VITC time code.
The genlock of the PT5230 must be set to either PAL Burst or NTSC Burst at input A-B.
Terminate the video signal with 75 ohms.
The Time Clock Interface must be set to “VITC on genlock” in the CONFIG / DATE-TIME / REFERENCE menu.

The UNLOCKED LED on the front panel must be off.

The DATE / TIME status display should show:
DATE: xx-xx-xx TIME: xx:xx:xx
REF: VITC on genlock STATUS:VITC(zzz)

zzz = PAL or NTSC

Check that TIME:xx:xx:xx shown is from the VITC time code.

Check that the VITC signal is received correctly with no termination and double termination of the genlock signal.

Disconnect the genlock signal.
The UNLOCKED LED on the front panel must be on.

The DATE / TIME status display should show:
DATE: xx-xx-xx TIME: xx:xx:xx
REF: VITC on genlock
STATUS:NO VITC

Check that TIME:xx:xx:xx shown is counting up correctly.

LTC:
Connect the PT5230 TIME CODE XLR-input to a LTC time code signal.
The Time Clock Interface must be set to “LTC-input” in the CONFIG / DATE-TIME / REFERENCE menu.

The DATE / TIME status display should show:
DATE: xx-xx-xx TIME: xx:xx:xx
REF: LTC-input STATUS:LTC(zzz)

zzz = PAL or NTSC

Check that TIME:xx:xx:xx shown is from the LTC time code.

Disconnect the LTC signal.

The DATE / TIME status display should show:
DATE: xx-xx-xx TIME: xx:xx:xx
REF: LTC-input STATUS:NO SIGNAL

Check that TIME:xx:xx:xx shown is counting up correctly.

1 Hz:
Connect the PT5230 TIME CODE XLR-input to a 1 Hz input signal.
The Time Clock Interface must be set to “1 Hz Reference” in the CONFIG / DATE-TIME / REFERENCE menu.

The DATE / TIME status display should show:
DATE: xx-xx-xx TIME: xx:xx:xx
REF: 1 Hz Reference STATUS: 1 Hz

Check that TIME:xx:xx:xx shown is counting up correctly each one second.

Disconnect the 1 Hz signal.

The DATE / TIME status display should show:
DATE: xx-xx-xx TIME: xx:xx:xx
REF: 1 Hz Reference STATUS:NO SIGNAL

Check that TIME:xx:xx:xx shown is counting up correctly.

11.3.2 Adjustments

There are no adjustments at this option.

12 SDI Black & Colour Bar Generator – PT 8639

12.1 General Information

PT 8639 is a single-board digital video generator. From a clock, line and frame -pulse it generates a complete serial digital video signal. Compared to the PT 8632 and PT 8333 the PT 8639 offers the Basic test signals, which are needed for routine check and alignment. Sound (digital silence) can be embedded in the signal. Error Data *Handling* (EDH) codes can be calculated and inserted in the signal.

The unit has two equal SDI outputs. The outputs are monitored by level detectors that sets off an alarm if the signal for some reason disappears.

The signal selected can be time adjusted ±1 field (a total of 625 lines or 525 lines) with a resolution of 1/27 μsec.

12.2 Block Diagram Description

12.2.1 SDI - Black Controller

This unit is controlled by a μController. This μController interfaces with the Master Controller on the Main Board via a two-wire serial bus and a reset wire.

The video part of the generator is controlled by a clock signal and, for each system (625-line and 525-line), a line pulse (625-line: FH_G; 525-line: FH_M) and a colour framing pulse. Colour framing for: 625-line/525-line systems is 2500/1050 lines between each pulse (625-line: F8_G; 525-line: F4_M).

When the power is switched on, the Master Controller detects the presence of one or more SDI Black & Colour Bar Generators. When detected, the unit(s) receive information on:

- What to generate
- Pattern
- Sound
- EDH-codes
- Timing

When this information is received, sound data and colour bars for the system chosen are stored in RAM (V56 & V57). When writing to the RAM, the PS-bit (V50, pin 40) is high, otherwise is low. Finally, an 11-bit word is written to the H-OFFSET PORT. This word is the sample offset between incoming and generated line pulses. The line and field offsets are generated by the μController, see below.

12.2.2 Video Generation

From System Select in V54 and the H-Counter in V63 a field/8 or field/4 (VINT) and a line interrupt (HINT) go to the μController. From these interrupts, two bits are generated; SO (V73, pin18) and S1 (V73, pin19). These two bits, together with the H-Counter, combines to a correct black line. S0 and S1 determine the fourth word in SAV and EAV sequences. Two bits, S2 (V73, pin 17) and S3 (V73, pin 16), are used to select one of four possible lines to generate, "0 0" = black line; "0 1", and "1 0" will generate one of the three colour bar lines stored in RAM. The RAM-address for the colour bar comes from the H-Counter in V63.

12.2.3 Sound Generator

Sound is also inserted in the signal in V63. When SOUND-bit (V73, pin 13) is high, sound-framing words are generated in the Sound Framing Generator. Sound data are inserted in the Data Multiplexer, which also calculates and inserts a checksum for sound data on each line. Sound data are stored in RAM and addressed by the Sound Address Counter in V63.
When FIELD-1 (V73, pin 12) is low, three sound samples for each of the four channels are inserted. When FIELD-1 is high, four samples are inserted.

12.2.4 EDH – Inserter

At the output of V63 (pin 21 to 9 [DO9..DO0]) a correct 10-bit SDI-parallel signal is present. These ten bits are clocked into the EDH - Inserter (V65). This circuit calculates and inserts EDH - codes into the data stream. Insertion takes place when the EDH-bit (V73, pin 15) is low. When the EDH-bit is high, data are clocked through without modification.

12.2.5 Parallel-to-Serial Converter

The ten bits are serialised in V59. Output from this circuit feeds the Output Amplifier (V60). This amplifier contains two amplifiers which drive two output BNC-connectors. Signals at these connectors are identical but independent of each other.

12.2.6 Level Detectors

The level detectors are connected, via two transformers (TR1 and TR2), directly to the output BNCs.

Signals from the TR1 transformer are rectified by D201 and V201 A, is then lowpass-filtered and amplified by V201B. This provides an almost DC-voltage at TP201/TP205 of -1.3V when the signal is correct (output open or terminated). This voltage keeps TP202 and XA1, pin 5 high. If signal at the BNC-connector vanishes, e.g. if the amplifier is not working, the DC-voltage increases to 0V. Then V203B takes TP202 and XA1, pin 5 low, indicating an error. TR2, V211, V213, and XA1-pin 6 has similar function.

12.2.7 Test Pins

These two pins could be used to indicate whether or not V59 locks or has a chance to lock, properly onto the incoming data stream.

TP5:
At this pin is a 27 MHz clock signal which is regenerated from incoming video data. This clock is 0.8V centred around 2.5 V and indicates whether or not the Serialiser (V59) is able to lock onto incoming data.

TP6:
This pin is low when data words $00.x_{Hex}$ and FF_{Hex} are received; otherwise it is high. In patterns without sound or EDH codes, there will be two low pulses in each line. These pulses indicate EAV and SAV.

12.3 Test and Adjustments

Test Equipment:
Digital Video Analyser:
Digital Video Component:Analyser: e.g. R&S VCA

12.3.1 Performance Check

To perform a performance check, you need an instrument that is able to measure following parameters:

- TRS - errors
- jitter
- serial video amplitude
- video level (digital information)
- sound detection (preferable an instrument that can convert the sound information to analog sound)
- The instrument must also be able to calculate EDH-codes

In system 625/50 check as follows:

- The generator should be internally locked

Using the menu select:
GENLOCK / Internal

- Using the menu select:

SDI-TSGx/ SYSTEM / 625/50

- Connect the "SDI BLK" output to the measuring device
- Select a black signal without sound:

SDI-TSGx/ PATTERN / Black
SDI-TSGx/ EMB.AUDIO/Silence
and EDH-codes
SDI-TSGx/EDH/ Off

- Look for TRS-errors: there should not be any
- Measure jitter: it must be <0.15 UI. Measure over 4 frames without lowpass-filtering
- Measure level of serial video: it must be 800 mV ±80 mV
- Select the 75 % colour bar signal

SDI-TSGx/ PATTERN/EBU C.Bar
Check the white level: it must be 235.00d
Using the waveform display, check for waveform errors

- Select the 100 % colour bar signal.

SDI-TSGx/ PATTERN
100% C.Bar
Check the white level: it must be 235.00d
Using the waveform display, check for waveform errors

- Add sound (silence) to the signal

SDI-TSGx/ EMB.AUDIO/
Silence
Make sure sound samples have been added to the SDI-signal

By converting to analog voltage, you get a good indication of whether there are any bit errors in the signal

- Check for reserved code errors. Values $00.x_{Hex}$ and $FF.x_{Hex}$ must not appear in the data stream except in TRS-words
- Add EDH-codes to the signal

SDI-TSGx / EDH / On

Check to make sure that the codes are in the signal and, if possible, whether they have been generated correctly

- Check level detectors

Connect PP1 of the generator. Notice which connector the generator is connected to (TSG2, TSG3, TSG4)

Watch the display, a message

LEVEL ERROR AT TSGx

should appear

In system 525/59.94 check as follows:

- Select system 525/59.94
  SDI-TSGx/ SYSTEM / 525/59.94
- Look for TRS-errors: there should not be any
- Select the SMPTE-colour bar signal
  SDI-TSGx / PATTERN / SMPTE
  Check the white level: it must be 180.25_d (line 25)

Output

- Connect the other "SDI TSGx" output to the measuring device, and check the level of the data signal: it should be 800 mV ±80 mV

Timing check

- The purpose of this check is to verify the output timing to be within ±1 sample period (~37nsec) when the display shows:
  V: -0 H: -000 T: -00000.0.

This check requires the SDI Digital Genlock option, PT8606, and another SDI Black & Colour Bar Generator. An instrument that can measure the timing difference between two SDI-signals is also necessary.

-
- Connect a SDI digital signal to "SDI GENLOCK IN" input
- Using the menu select:
- GENLOCK / SDI PAL Burst
- Compare the output from SDI Digital Genlock option at "SDI GENLOCK OUT" to the output from SDI Black & Colour Bar Generator at "SDI BILK", the timing should be the same as the reference generator

12.3.2 Adjustments

There are no adjustments at this unit.

13 PT5210 options which can be mounted

The following units can be installed in the PT5230 and recognised by the menu system of the instrument.

These options are:
- PT 8604 Multiple Black Burst output
- PT8608 Analog Black Burst

There are a few restrictions in the use of these options:

The standard text on the rearplate does not reflect the proper text. Labels to be applied to the rear of the cabinet.
Some of the menu items may have different texts compared to the standard PT 5230 texts

Please contact the factory for more information.

14 Multiple Parallel Black Burst – PT 8604

14.1 General Information

This option is a Black Burst Buffer.

It consists of a common Input Buffer with a Gain Regulation (R9). After the Input Buffer, the signal goes to 6 Output Buffers.

The level at each output is monitored by the Level Detector.

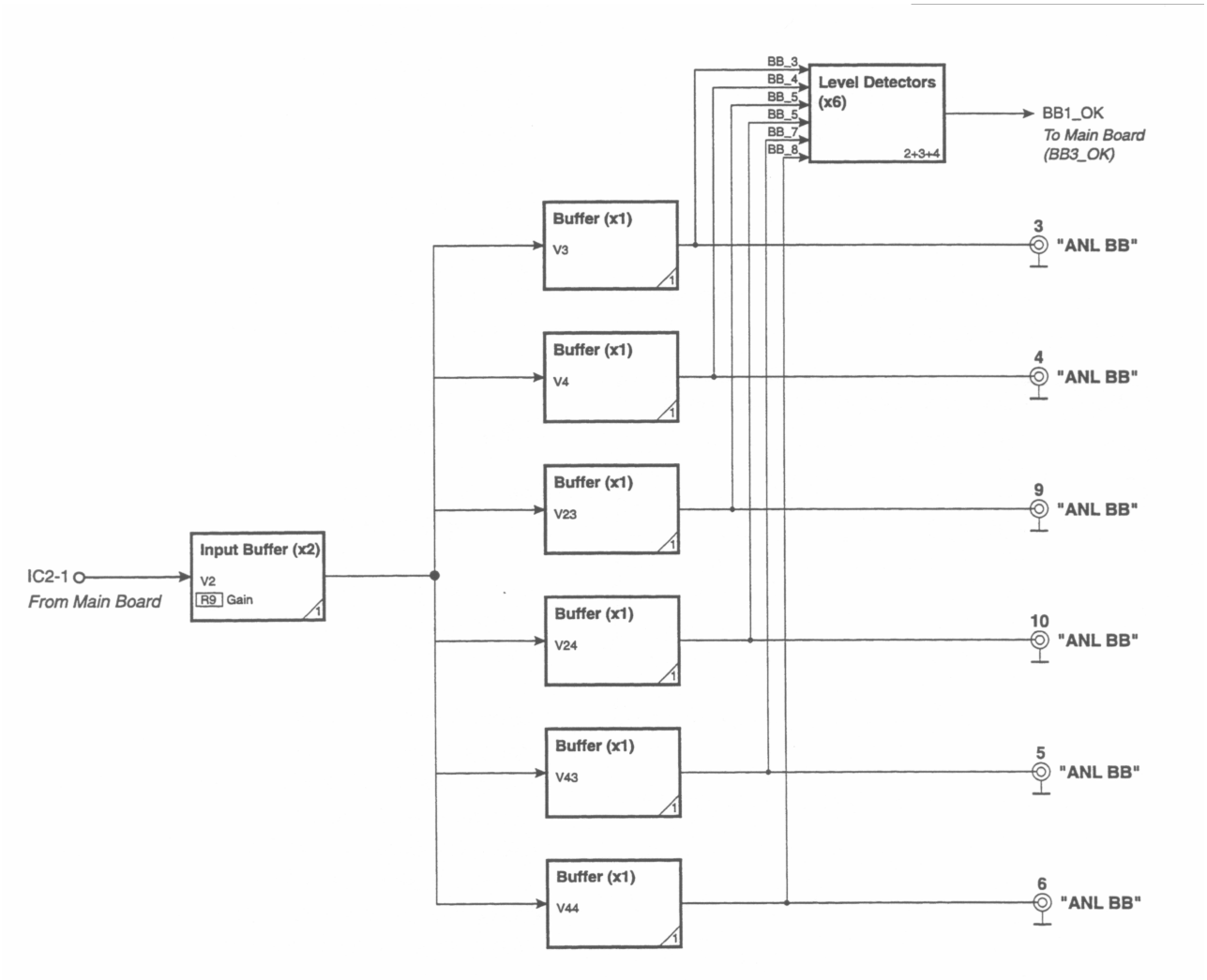
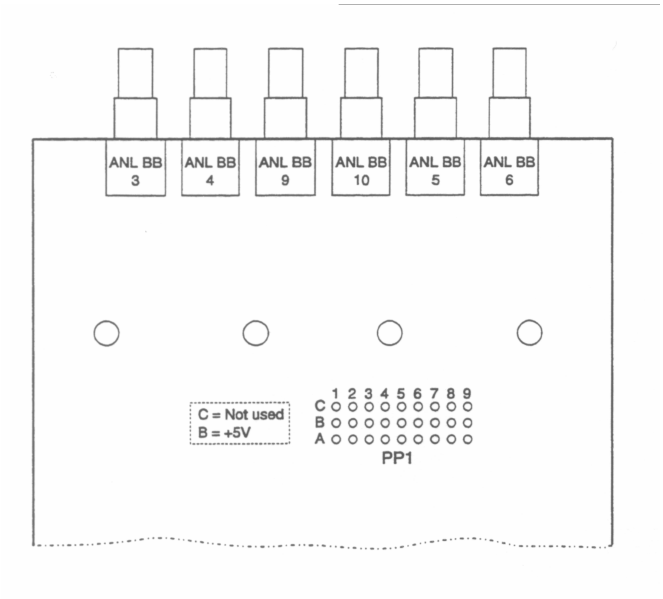


Fig. 16-1 Block Diagram – PT 8604

14.1.1 Disabling of Level Detectors

It is possible to disable Level Detectors by solder the Code Field (PP1). Please refer to figure below for location of PP1.



To disable a Level Detector, solder the level signal in column A to column B *(+5V)*.

Row	Level error signal from rear panel connectors:
1	ANL BB 3
2	ANL BB 4
3	ANL BB 9
4	ANL BB 10
5	ANL BB 5
6	ANL BIB 6
7	Not used
8	Not used
9	Not used

Example:
To disable level error from "ANL BB 6", solder A4 to B4.

14.2 Test and Adjustments

Test Instruments:

Video Level Meter:	VM 700
Waveform monitor/Vectorscope, Sc-H:	e.g. PM 5661/70
Oscilloscope:	e.g. PM 3094

14.2.1 Level Detectors Control

- Leave every output unterminated
- Switch the instrument off and on
- Then press the ▲ button
- The display should read:
  PT S230 ERROR/WARNING STATUS
  NO ACTIVE WARNINGS
- Terminate the analog black burst ("ANL BB") output one by one with 3 x 75Ω termination in parallel (25Ω)
- The following message should appear in the display:
  GENLOCK: A
  E(001): LEVEL ERROR AT BB2MUL
  for each output when it is terminated with *25 Ω.*

14.2.2 Performance Checks

Note: This performance check should be done at all 6 outputs.

- Use menu to select:
  ANALOG-BLACK / BB2 SYSTEM
  PAL w/PAL ID

  - Using Waveform Monitor Vectorscope, check that the burst amplitude is 300 mV ±6 mV
  - Using Waveform Monitor / Vectorscope, check that the Sc-H phase is 0^{o} $\pm 5^{o}$
  - Using Oscilloscope, check that the DC voltage on the blanking level is 0 mV ±20 mV
  - Using Waveform Monitor / Vectorscope, check that there is a white pulse on line 7

14.2.3 Adjustments

1. Gain

- Use menu to select: ANALOG-BLACK / BB2 / SYSTEM PAL w/PAL ID
- Using Video Level Meter, check that the sync amplitude is 300 mV ±6 mV. If necessary, adjust sync amplitude at R9

15 Analog Black Burst Generator – PT 8608

15.1 Block Diagram Description

The input to the Black Burst Generator is a 27 MHz clock signal, a line and field reference for both PAL-G and NTSC, and a V24 serial bus from the Master Controller to select phase and system.

The μProcessor (V201, V203, V204, and V212) receives data via the V24 bus and outputs course horizontal phase and line type to the H-Counter (V206). Fine horizontal phase, burst phase, and system are outputs to the Phase Latch (V205).

The μProcessor is controlled by a line interrupt pulse and a field pulse. The μProcessor controls two Black Burst Generators.

The course horizontal phase from the μProcessor goes to the H-Counter/Decoder (V206), which is preset to the course horizontal phase at the horizontal timing reference.

The H-Counter is decoded together with line type information from the μProcessor; and it also addresses the signal PROMs.

The video data is stored in 2 EPROMs (V207 and V208), which are addressed by the H-Counter/ Decoder and the Phase Latch.

The outputs from the PROMs are multiplexed to a 27 MHz 10-bit data stream. The data is sent to a D/A Converter (V213, V214, V215, and V217) through an Anti-aliasing Filter to the Output Amplifier (V216).

15.2 Test and Adjustments

15.2.1 Performance Check

Test Equipment:

Video level meter:	e.g. VM 700
Waveform monitor/Vectorscope, Sc-H:	e.g. PM 5662
Oscilloscope:	e.g. PM 3094

This performance check should be performed at **all** analog black burst outputs at the instrument.

PAL G System:

- Using menu select:
  ANALOG-BLACK / BBX / SYSTEM PAL w/PAL ID
- Using Video Level Meter, check that the sync amplitude is 300 mV ±6 mV
- Using Waveform monitor/Vectorscope, check that the burst amplitude is 300 mV ±6 mV
- If necessary, adjust the burst amplitude at C203 on channel 1, 3, 5, and 7 or at C303 on channel 2, 4, 6, and 8
- Using Waveform monitor/Vectorscope, check that the Sc-H phase is $0^{o} \pm 5^{o}$
- Using Oscilloscope, check that the DC voltage on the blanking level is 0 mV ±20 mV

- Using Waveform monitor/Vectorscope, check that there is a white pulse on line 7

NTSC System:
- Using menu select:
  ANALOG-BLACK / BBX / SYSTEM / NTSC
- Using Video Level Meter, check that the sync amplitude is 286 mV ±6 mV
- Using Waveform monitor/Vectorscope, check that the burst amplitude is 286 mV ±6 mV
- Using Waveform monitor/Vectorscope, check that the Sc-H phase is $0^{o} \pm 5^{o}$
- Using Oscilloscope, check that the DC voltage on the blanking level is 0 mV ±20 mV
- Using Waveform monitor/Vectorscope, check that the signal contains set-up

Timing check:
The following description applies to instruments in which all timings are set to zero, at the black burst output as well as on genlock timings. When this is not practical - for example, if you are checking an instrument which has been adjusted for a certain application - you will have to compensate for the instrument setting.

PAL G System:
- Using menu select:
  GENLOCK / A-B PAL Burst
- Genlock the PT 5210 to a PAL G video signal at "ANALOG GENLOCK A" input
- Connect the "ANALOG GENLOCK B" input from the PT 5210 to the B input of Waveform monitor/ Vectorscope
- Connect the "ANL BB" output to the A input of the Waveform monitor/Vectorscope
- Connect the "GENLOCK MONITOR" output from the PT 5210 to the external sync input of the Waveform monitor/Vectorscope
- Check that the line syncs have the same timing ±2 nsec
- Check that the field syncs have the same timing (± 0 line)
- Check that the bursts have the same phase ($\pm 2^{o}$)

NTSC System:
- Using menu select:
  GENLOCK / A-B NTSC Burst
- Genlock the PT 5210 to a NTSC video signal at "ANALOG GENLOCK A" input
- Connect the "ANALOG GENLOCK B" input from the PT 5210 to the B input of Waveform monitor/Vectorscope
- Connect the "ANL BB" output to the A input of the Waveform monitor/Vectorscope
- Connect the "GENLOCK MONITOR" output from the PT 5210 to the external sync input of the Waveform monitor/Vectorscope
- Check that the line syncs have the same timing (± 2 nsec)
- Check that the field syncs have the same timing (± 0 line)
- Check that the bursts have the same phase ($\pm 2^{o}$)

15.2.2 Adjustments

There are no adjustments at this unit.

16 Chapter reserved for future use

17 Diagram and component placements

Please refer to Section 2 of this Service Manual

END OF DOCUMENT