Logic Design Viva Question Bank

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Title of the Practical: Verify the truth table of logic gates AND, OR, NOT, NAND and NOR gates/ Design Basic Gates Using NAND/NOR gates.

Q.1 What is DIGITAL GATE?

A1:-Digital gates are basically electronic components which are used for switching and manipulating binary data

Q.2 What do u mean by universal gate?

A2:-The universal gates are those gate from which we can make any gate by using them. The universal gates are- NAND & NOR

Q.3 What is truth table?

A3:-Truth table is a table from which we can get o/p of different gates

Q4. Make truth table of NAND gate?

A4:-

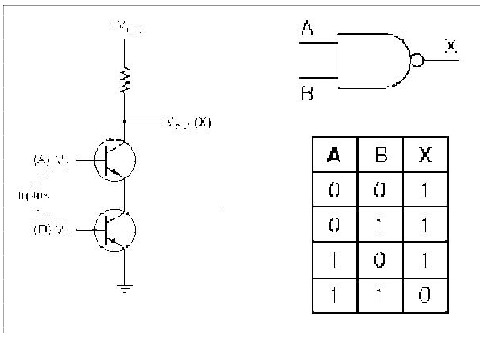
A	B	o/p
0	0	1
0	1	1
1	0	1
1	1	0

Q.5 What is different between Ex-or & Ex-nor gate?

A5:-the basic difference between this two gate is that Ex-or gate gives o/p when both the i/p is different & Ex-nor gate give o/p when both i/p same.

Q.6 Draw the NAND gate?

A6:-



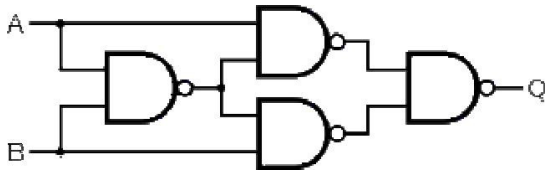
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Q.7 Draw the Ex-or gate?

A7:-

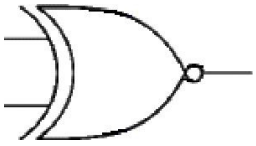
Q.8 Draw the EX-OR gate by using the NAND gate?

A8:-



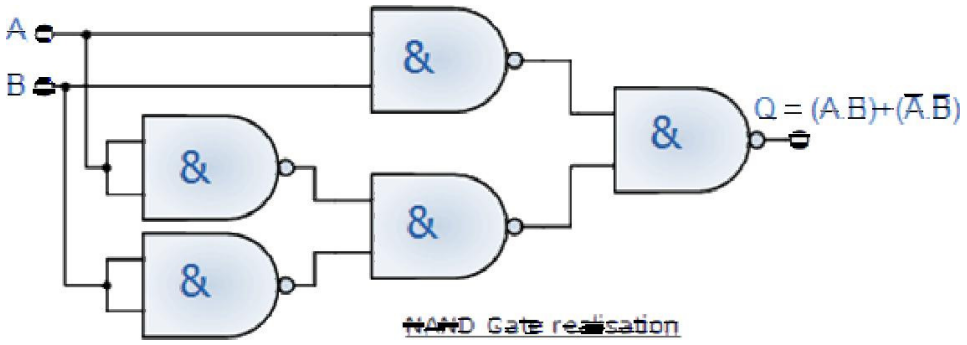
Q.9 Draw the EX-NOR gate?

A9:-



Q.10 Draw the EX-NOR by using the NAND gate?

A10:-



Q.11 What is the Universal gates?

A11– the universal gates are the gate by help of which we can make other all gates.

Q.12:- Types of universal gate?

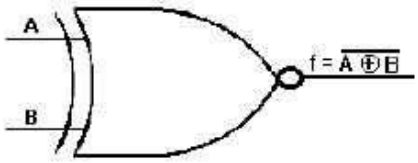
A12: - There are two universal gates:-

1. NAND
2. NOR

Q.13:- Make the symbol of NOR gate?

A13: -

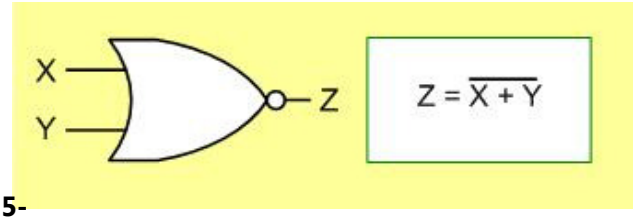
Q.14:- Draw the EX- NOR gate and also write truth table?



A	B	f
0	0	1
0	1	0
1	0	0
1	1	1

Q.15:- Draw the NOR gate?

A15-



Q.16:- What is the truth table of NOR gate?

A16:

X	Y	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Q. 17. What is a multiplexer?

A 17

A multiplexer is a combinational circuit which selects one of many input signals and directs to

the only output.

Q. 18. What is a demultiplexer?

A 18

Conversely, a demultiplexer (or demux) is a device taking a single input signal and selecting one of many data-output-lines, which is connected to the single input. A multiplexer is often used with a complementary demultiplexer on the receiving end.

Title of the Practical: - Design of half adder.

Q.1 What is use of half adder?

A1:-It is used for adding 2 bit data

Q.2 In Half adder how many inputs are used?

A2: - Two

Q.3 In o/p of Half adder what we gate?

A3: - SUM, CARRY

Q.4 In Half adder SUM=?

A4: - SUM= A (+) B.

Q.5 In half adder Carry=?

A5: - AB

Q.6 How many AND gate required to make a Half adder?

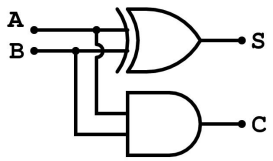
A6: - 1 one

Q.7 In Half adder how many types of gates are required?

A7: - two types NAND & Ex-or

Q.8 Draw the half adder diagram?

A8:-



Q.9 What is difference between the half and full adder?

A9: - in half adder only 2bits can be use but in full adder we can use 3

bit data. **Q.10 What is difference between half adder and half**

subs tractor?

A10:- The only difference is in carry & borrows expression.

Title of the Practical: - Design of full adder.

Q.1 What is use of Full adder?

A1:-Full adder is used for adding three bit data.

Q.2 In full adder how many inputs are used?

A2:-three

Q.3 In o/p of full adder what we gate?

A3:-SUM & Carry

Q.4 In full adder SUM=?

A4: - SUM= A (+) B (+) C.

Q.5 in full adder Carry=?

A5:-Carry=AB+BC+AC

Q.6 How many half adders required to make a full adder?

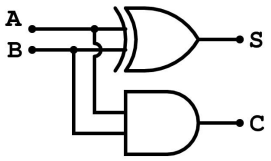
A6: - 2 Half Adder

Q.7 In full adder how many types of gates are required?

A7:-three types 1. And, 2.Ex-or, 3.or

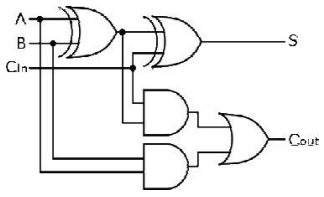
Q.8 Draw the half adder diagram?

A8:-



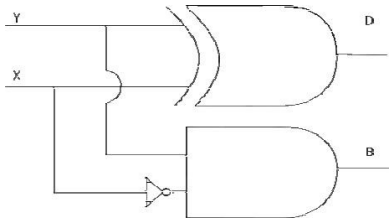
Q.9 Draw the full adder diagram?

A9:-



Q.10 Draw the half subtractor diagram?

A10:-



Title of the Practical: - Design half subs tractor.

Q.1 What is use of half Subs tractor?

A1: - It is used for subs tract 2 bit data.

Q.2 In Half Subs tractor how many inputs are used?

A2: - two

Q.3 In o/p of Half Subs tractor what we gate?

A3:-Difference & Borrow

Q.4 In Half Subs tractor Difference=?

A4: - Difference=A (+) B. Borrow=A'B?

Q.5 How many AND gate required to make a Half Subs tractor?

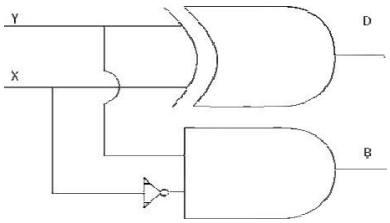
A5:- one

Q.6 In Half Subs tractor how many types of gates are required?

A6:- two ANAD & Ex-or

Q.7 Draw the half subtractor diagram?

A7:-



Q.8 What is difference between full & half substractor?

A8: - in half substractor we can subtract only 2 bit data but in full substractor we can subtract 3 bit data. **Q.9 What is difference between half adder and half substractor?**

A9: - The only difference is in carry & borrows expression. **Q10 If input of half substractor is 11 then output is?**

A10: - Difference= 0, borrow=0.

Title of the Practical:- Design of full substractor.

Q.1 What is use of Full Substractor?

A1: - Full substractor is used for differentiate three bit data. **Q.2 In Full**

Subs tractor how many inputs are used?

A2: - three

Q.3 In output of Full Subs tractor what we gate?

A3: - Difference & borrow

Q.4 In Full Subs tractor Difference=?

A.4 Difference=A (+) B (+) C. Borrow=A'B+A'C+BC?

Q.5 How many NAND gate required to make a Full Substractor?

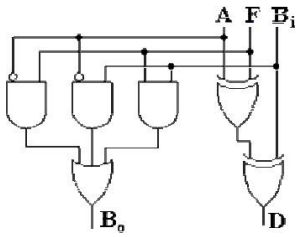
A5: - nine

Q.6 In Full Subs tractor how many Half Subs tractor are required?

A6:-two

Q.7 Draw the full substractor diagram?

A7:-

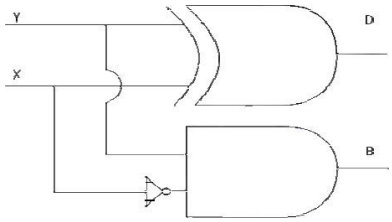


Q.8 How many half substractor are required to construct a full adder?

A8: - Two half substractor are required to construct a full adder.

Q.9 Draw the half substractor diagram?

A9:-



Q10. What is difference between full & half substractor?

A10: - In half substractor we can subtract only 2 bit data but in full substractor we can subtract 3 bit data.

Title of the Practical: - Verify the operation of magnitude comparator (7485 IC)

Q1. What is magnitude comparator?

A1 a digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. Comparators are used in a central processing units (CPU) and microcontrollers. Examples of digital comparator include the CMOS 4063 and 4585 and the TTL 7485 and 74682-'89.The analog equivalent of digital comparator is the voltage comparator. Many microcontrollers have analog comparators on some of their inputs that can be read or trigger an interrupt.

Q2. What is most significant bit?

A2 In computing, the most significant bit (msb, also called the high-order bit) is the bit position in a binary number having the greatest value. The msb is sometimes referred to as the left-most bit on big-endian architectures, due to the convention in positional notation of writing more significant digits further to the left.

Q3. Explain operation of AND gate?

A3 the AND gate is a digital logic gate that implements logical conjunction - it behaves according to the truth table to the right. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results. In another sense, the function of AND effectively finds the minimum between two binary digits, just as the OR function finds the maximum.

Q4. Explain truth table of a comparator?

A4 the operation of a single bit digital comparator can be expressed as a truth table:

Inputs		Outputs		
A	B	A < B	A = B	A > B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Q5. What is equality?

A5 The binary numbers A and B will be equal if all the pairs of significant digits of both numbers are equal, i.e.,

$A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$ and $A_0 = B_0$

Q6. What is inequality?

A6 In order to manually determine the greater of two binary numbers, we inspect the relative magnitudes of pairs of significant digits, starting from the most significant bit, gradually proceeding towards lower significant bits until an inequality is found. When an inequality is found, if the corresponding bit of A is 1 and that of B is 0 then we conclude that A>B.

Q7. Explain magnitude comparator7485 IC

A7 the 74F85 is a 4-bit magnitude comparator that can be expanded t almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0–A3) and (B0–B3) where A3 and B3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal Operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme. The expansion inputs IA>B, and IA=B and IA<B are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the lease significant word are connected to the corresponding IA>B, IA=B and IA<B inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation, the expansion inputs of the least significant word should be tied as follows: IA>B = Low, IA=B = High and IA<B = Low.

Q8. What is 8-input Magnitude Comparator?

A8 - Magnitude Comparator. This Magnitude Comparator can be used perform comparisons of two 8-bit binary or BCD words. The output provides both a P equals Q function or P greater than Q function. A Magnitude Comparator would be considered standard logic or glue logic when a discrete IC is used. However, because of the internal complexity, a Magnitude Comparator would also be considered an MSI Function [Medium Scale Integration].

Q9. What is IC?

A9 - In electronics, an integrated circuit (also known as IC, chip, or microchip) is a miniaturized electronic circuit (consisting mainly of semiconductor devices, as well as passive components) that has been manufactured in the surface of a thin substrate of semiconductor material. Integrated circuits are used in almost all electronic equipment in use today and have revolutionized the world of electronics. Computers, cellular phones, and other digital appliances are now inextricable parts of the structure of modern societies,

made possible by the low cost of production of integrated circuits.

Q10. Tell about advancement in integrated circuits?

A10 - Among the most advanced integrated circuits are the microprocessors or "cores", which control everything from computers and cellular phones to digital microwave ovens. Digital memory chips and ASICs are examples of other families of integrated circuits that are important to the modern information society. While the cost of designing and developing a complex integrated circuit is quite high, when spread across typically millions of production units the individual IC cost is minimized. The performance of ICs is high because the small size allows short traces which in turn allows low power logic (such as CMOS) to be used at fast switching speeds.

Title of the Practical: - Study of flip-flop.

Q.1 what is flip-flop?

A1: - Flip-flop is a 1 bit storing element.

Q.2 how many types of flip-flop are used?

A2: - 4 types of flip –flop, S-R, J-K, D, T

Q.3 what is disadvantage of SR flip-flop?

A3:- When both the input is one then it gives invalid

output. **Q.4 what is disadvantage of JK flip-flop?**

A4: - race around condition.

Q.5 to remove race around condition what we use?

A5: - master slave Flip-flop.

Q.6 what is race around condition?

A6: - when pulse width is more then signal width then for signal change of pulse width many no of times signal changes its state that is called race around condition.

Q7 what are the characteristic equation for T flip-

flop?

A7 Q = TQ'+ QT'

Q8 which Gates are used in SR flip flops to a JK flip-flop?

A8 Nand Gates

Q.9 D flip-flop is used for?

A9: - providing delay.

Q.10 what is full form of T flip-flop?

A10: - toggle flip-flop

Title of the Practical: - Design 3/4 bit Counter & Ripple 3/4 bit Counter & verify truth table.

Q1 What is counter?

A1 In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

Q2 Give types of counter?

A2 there are two types of counters(1) Up counters, which increase (increment) in value (2) Down counters, which decrease (decrement) in value .

Q3 What are the implements of counter?

A3 In electronics, counters can be implemented quite easily using register-type circuits such as the flip-flop, and a wide variety of designs exist, e.g.:(1)Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops (2)Synchronous counter – all state bits change under control of a single clock (3)Decade counter – counts through ten states per stage (4)Up–down counter – counts both up and down, under command of a control input (5)Ring counter – formed by a shift register with feedback connection in a ring (6)Johnson counter – a twisted ring counter (7)Cascaded counter

Q4 Explain Asynchronous (ripple) counter?

A4 an asynchronous (ripple) counter is a single K-type flip-flop, with its J (data) input fed from its own inverted output. This circuit can store one bit, and hence can count from zero to one before it overflows (starts over from 0). This counter will increment once for every clock cycle and takes two clock cycles to overflow, so every cycle it will alternate between a transition from 0 to 1 and a transition from 1 to 0. Notice that this creates a new clock with a 50% duty cycle at exactly half the frequency of the input clock. If this output is then used as the clock signal for a similarly arranged D flip-flop (remembering to invert the output to the input), you will get another 1 bit counter that counts half as fast. Putting them together yields a two bit counter.

Q5 Explain Johnson counter?

A5 A Johnson counter (or switch tail ring counter, twisted-ring counter, walking-ring counter, or Moebius
counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. A pattern of bits equal in length to twice the length of the

shift register thus circulates indefinitely. These counters find specialist applications, including those similar to the decade counter, digital to analog conversion, etc. it can be established by D flip flop and JK flip flop.

Q6 Explain Decade counter?

A6 A decade counter is one that counts in decimal digits, rather than binary. A decade counter may have each digit binary encoded (that is, it may count in binary-coded decimal, as the 7490 integrated circuit did) or other binary encodings (such as the bi-quinary encoding of the 7490 integrated circuit).

Alternatively, it may have a "fully decoded" or one-hot output code in which each output goes high in turn; the 4017 is such a circuit. The latter type of circuit finds applications in multiplexers and demultiplexer, or wherever a scanning type of behavior is useful. Similar counters with different numbers of outputs are also common.

Q7 What is synchronous counters?

A7 In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The circuit below is a 3-bit synchronous counter. The J and K inputs of FF0 are connected to HIGH. FF1 has its J and K inputs connected to the output of FF0, and the J and K inputs of FF2 are connected to the output of an AND gate that is fed by the outputs of FF0 and FF1.

Q8 Give truth table of two bit counter?

A8 Putting they together yield a two bit counter:

Cycle Q1 Q0 (Q1:Q0)dec

0	0	0	0
1	0	1	1
2	1	0	2
3	1	1	3
4	0	0	0

Q9 Give types of ring counters?

A9- There are two types of ring counters: (1)A straight ring counter or Over beck counter connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. For example, in a 4-register one-hot counter, with initial register values of 1000, the repeating pattern is: 1000, 0100, 0010, 0001, 1000... . Note that one of the registers must be pre-loaded with a 1 (or 0) in order to operate properly. (2)A twisted ring counter (also called Johnson counter or Moebius counter) connects the complement of the output of the last shift register to its input and circulates a stream of ones followed by zeros around the ring. For example, in a 4-register counter, with initial register values of 0000, the repeating pattern is: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, and 0000.

Q10 What is one hot counter?

A10 - In digital circuits, one-hot refers to a group of bits among which the legal combinations of values are only those with a single high (1) bit and all the others low (0). For example, the output of a decoder is usually a one-hot code, and sometimes the state of a state machine is represented by a one-hot code. A similar implementation in which all bits are '1' except one '0' is sometimes called one-cold

Title of the Practical: Design a counter for given event's counting

Q.1 what is counter?

Ans: - a **counter** is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

Q.2 what is the types of counter?

A1: In practice, there are two types of counters:

1. Up counters, which increase (increment) in value
2. Down counters, which decrease (decrement) in value

Q.3 what is the basic type of counter made by flip-flop or resistor?

A2: - Asynchronous (ripple) counter – changing state bits are used as clocks to subsequent state flip-flops

Synchronous counter – all state bits change under control of a single clock

Decade counter – counts through ten states per stage

Up–down counter – counts both up and down, under command of a control input

Ring counter – formed by a shift register with feedback connection in a ring

Johnson counter – a *twisted* ring counter

Cascaded counter

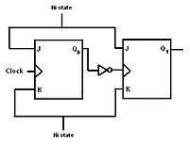
Q.4 what is asynchronous counter?

A4: - An asynchronous (ripple) counter is a single K-type flip-flop, with its J (data) input fed from its own inverted output. This circuit can store one bit, and hence can count from zero to one before it overflows (starts over from 0). This counter will increment once for every clock cycle and takes two clock cycles to overflow, so every cycle it will alternate between a transition from 0 to 1 and a transition from 1 to 0.

Notice that this creates a new clock with a 50% duty cycle at exactly half the frequency of the input clock. If this output is then used as the clock signal for a similarly arranged D flip-flop (remembering to invert the output to the input), you will get another 1 bit counter that counts half as fast

Q.5 make diagram of Asynchronous counter?

A5:-



Q.6 what is Synchronous counter?

A6:- A simple way of implementing the logic for each bit of an ascending counter (which is what is depicted in the image to the right) is for each bit to toggle when all of the less significant bits are at a logic high state. For example, bit 1 toggles when bit 0 is logic high; bit 2 toggles when both bit 1 and bit 0 are logic high; bit 3 toggles when bit 2, bit 1 and bit 0 are all high; and so on.

Synchronous counters can also be implemented with hardware finite state machines, which are more complex but allow for smoother, more stable transitions.

Q.7 what is the ring counter?

A7: - A ring counter is a shift register (a cascade connection of flip-flops) with the output of the last one connected to the input of the first, that is, in a ring. Typically a pattern consisting of a single 1 bit is circulated, so the state repeats every N clock cycles if N flip-flops are used. It can be used as a cycle counter of N states.

Q.8 what is the Johnson counter?

A8: - A Johnson counter (or switchtail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. A pattern of bits equal in length to twice the length of the shift register thus circulates indefinitely. These counters find specialist applications, including those similar to the decade counter, digital to analog conversion, etc. it can be established by D flip flop and JK flip flop

Q.9 what is the decade counter?

A9: - A decade counter is one that counts in decimal digits, rather than binary. A decade counter may have each digit binary encoded (that is, it may count in binary-coded decimal, as the 7490 integrated circuit did) or other binary encodings (such as the bi-unary encoding of the 7490 integrated circuit). Alternatively, it may have a "fully decoded" or one-hot output code in which each output goes high in turn; the 4017 is such a circuit. The latter type of circuit finds applications in multiplexers and demultiplexers, or wherever a scanning type of behavior is useful. Similar counters with different numbers of outputs are also common.

The decade counter is also known as a mod-counter.

Q.10 what do you mean by up down counter?

A10:- A counter that can change state in either direction, under the control of an up–down selector input, is known as an up–down counter. When the selector is in the up state, the counter increments its value; when the selector is in the down state, the counter decrements the count

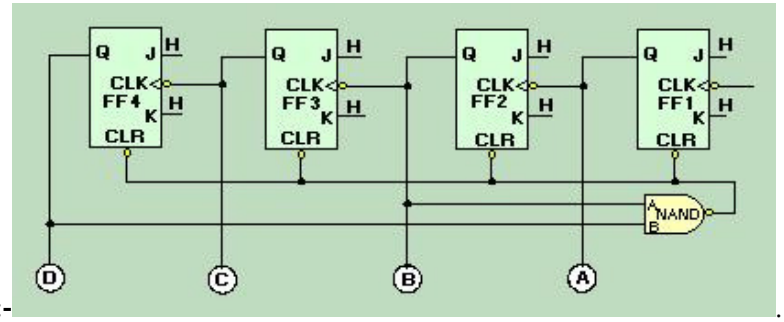
Machine cycle- the time taken by data/ opcode / operand from memory/ peripheral devices to acknowledge the external hardware. it takes 1to 6 T-state.

Title of the Practical: Design Decade Counter & verify truth table.

Q1. What is decade counter?

A1:- A decade counter is a binary counter that is designed to count to 10_{10}, or 1010_2. An ordinary four-stage counter can be easily modified to a decade counter by adding a NAND gate as shown in figure 3-25. Notice that FF2 and FF4 provide the inputs to the NAND gate. The NAND gate outputs are connected to the CLR input of each of the FFs.

Q2. Diagram of decade counter?

A2:- 

.

Q3 How many stages are required for a decade counter?

A3 Four.

Q4 In figure 3-25, which two FFs must be HIGH to reset the counter?

A4. FFs 2 and 4.

Q5 Which AND gate causes FF3 to reset?
A5 Three.

Q6 what causes the specified condition to shift position?
A6 the input or clock pulse.
Q7 If the specified state is OFF, how many FFs may be off at one time?

A7 One.
Q8 how many FFs are required to count down from 15_{10}?

A8 Four

Q9 what signal causes FF2 to toggle?

A9 Q output of FF 1 going LOW

Q10 How many stages are required to store a 16-bit word?

A10
16.

Title of the Practical: Design Shift Register & verify truth table

Q. what is the shift resistor?

A1 Shift resistor is a device which is used for storing and processing the bit in series or parallel.

Q.2- Types of shift resistor?

A2:-Serial-in/serial-out shift register (FIFO or LIFO)

Serial-in/parallel-out shift register

Parallel-in/parallel-out shift register

Parallel-in/serial-out shift register

.**Q3- In SISO resistor how many input cycles are required?**

A3 – it required n+1 clock pulse for input & n clock pulse for output.

Q4- In PISO resistor how many input cycles are required?

A4 - it required 1 clock pulse for input & n clock pulse for output

Q.5 In PIPO resistor how many input cycles are required?

A5 it required 1 clock pulse for input & 0 clock pulse for output

Q.6 In SIPO resistor how many input cycles are required?

A6: it required n+1 clock pulse for input & 0 clock pulse for output

Q.7what do you mean by clock enable?

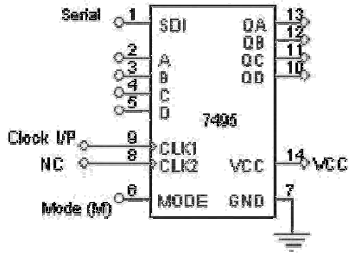
A7 When the Clock Enable input is High, the enabled load and shift actions take place on the next active Clock transition. When Clock Enable is Low, the register contents are unaffected by the Clock. Connections: Clock Enable is optional. Use this input when you need to disable the clock temporarily. If you do not use the Clock Enable input, the Clock is always enabled.

Q.8what is the clock?

A8 clock is a trigger. By Appling the clock the information proceeds.

Q.9 Pin diagram of SIPO shift resistor?

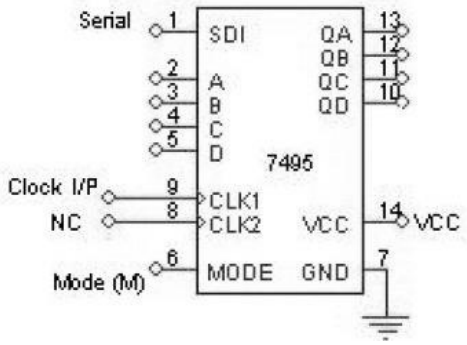
SIPO (Right Shift):-



A9

Q.10 Pin diagram of SISO shift resistor?

SISO:-



A10: