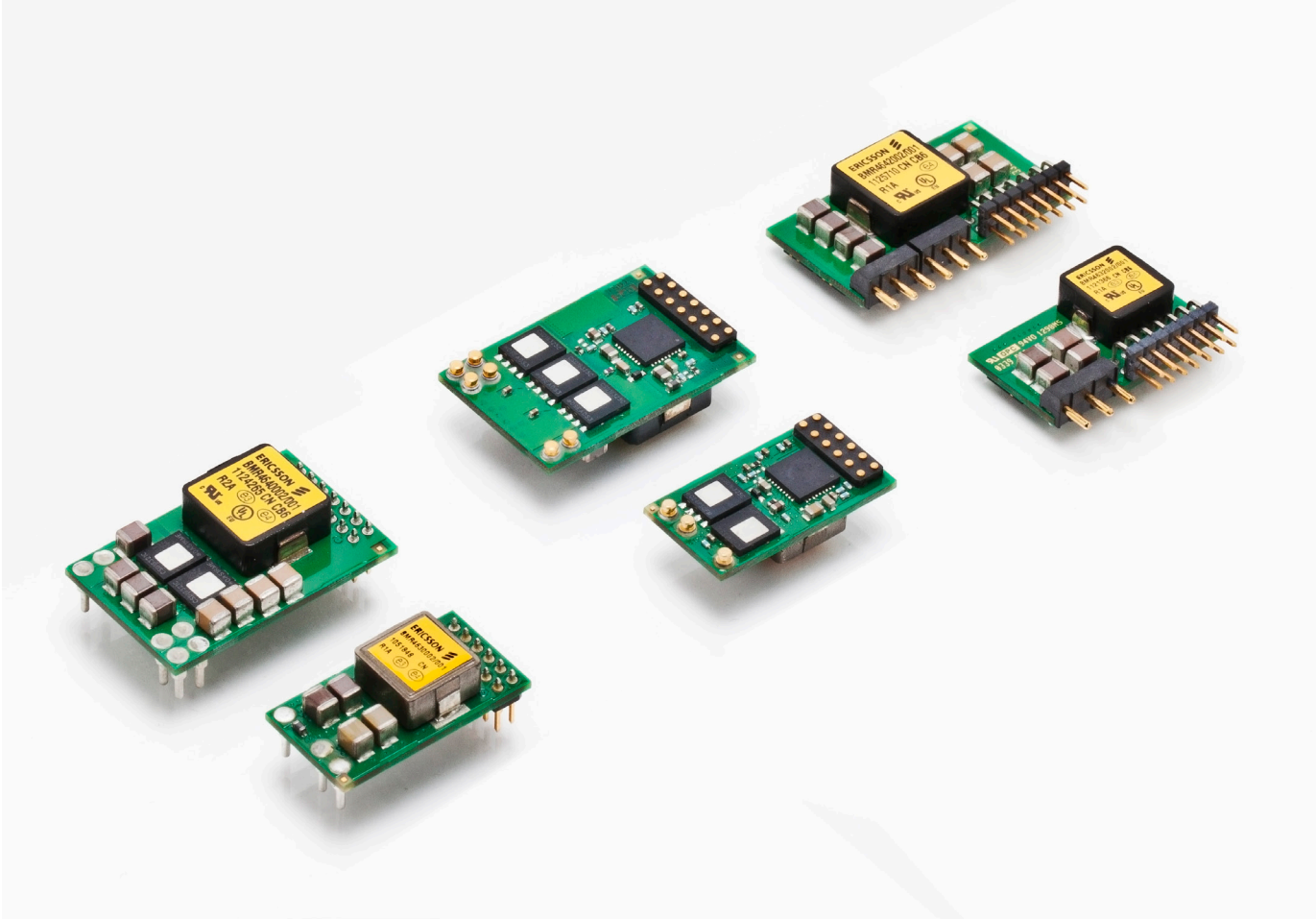
APPLICATION NOTE 307

Power Modules

ERICSSON



BMR463 AND BMR464 PARALLEL OPERATION WITH LOAD SHARING

ABSTRACT

The 3E Digital products can be configured, controlled and monitored through a digital serial interface using the PMBus™ power management protocol.

This application note provides information on how to parallel two or more 3E POL regulators.

The most common reason for paralleling Board Mounted Power Supplies are either to increase the power output capability above the rating of a single product or to provide redundancy so that a single product failure will not affect the system operation.

Other reasons for using products in parallel include distribution of thermal heat load over a larger board area and reducing the number of different product types used in a system design by implementing higher power requirements using products with lower output power in parallel.

INTRODUCTION

A current sharing group is two or more modules operating in parallel at the same frequency - that is their outputs are connected together and interleaved to multiply the ripple frequency by the number of paralleled products. Paralleling products in this manner has the added benefits of reducing the input filter stress, distributing the converter thermal load, reducing volume and weight and many other advantages.

Throughout this application note, the modules forming a current sharing group are sometimes referred to as phases. For example, a current sharing group of three paralleled modules has three phases. Similarly the current sharing group as a whole may also be referred to as a parallel rail.

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PARALLELING FEATURES & PHILOSOPHY

Master And Slaves Over The GCB Bus

Master and Slaves

At a high level, current sharing is a group of modules with their outputs tied together to form a single rail. The modules, acting as shared phases, require one phase to act as a master to continuously broadcast its inductor current to the other 'slave' phases using the GCB bus. This 'master' is typically the lowest-addressed device in the current sharing group. When a 'slave' phase receives the inductor current from the 'master', it trims its output voltage up or down until all products in the group supply the same current to the load. A maximum of 7 products or phases is allowed in a current sharing group, and must be of the same model.

If the master device faults during operation, the next device with the lowest member position will become the new current-sharing master. If the master is also sourcing the SYNC clock (as shown in Figure 1), it will continue to supply to clock if it faults even though it's become inactive.

Introducing the GCB (Global Communication Bus)

The Ericsson BMR 462-464 modules have a dedicated single wire serial bus (the GCB bus) to synchronize and communicate real-time events. This is an internal bus, such that it is only connected across BMR 462-464 modules and not the PMBus system host. Addressing individual modules across the GCB is done with a 5 bit GCB ID, yielding a theoretical total of 32 modules that can be shared with a single GCB bus. By default, the GCB ID is the lower five bits of a module's SMBus Address. Ensure that the GCB signal integrity is maintained when using a large product count.

During GCB events, all products will receive messages; however, only those products configured to respond will do so. GCB products can also transmit events if their programmed algorithm requires inter product communication. Some examples include fault spreading, sequencing, phase add/drop, broadcast margin and broadcast enable.

Multiple current sharing groups and power rails can communicate over the same GCB bus.

Active Droop Current Sharing

Current sharing with digital power has its share of advantages, but to understand this it's worth revisiting the fundamentals of current sharing and droop.

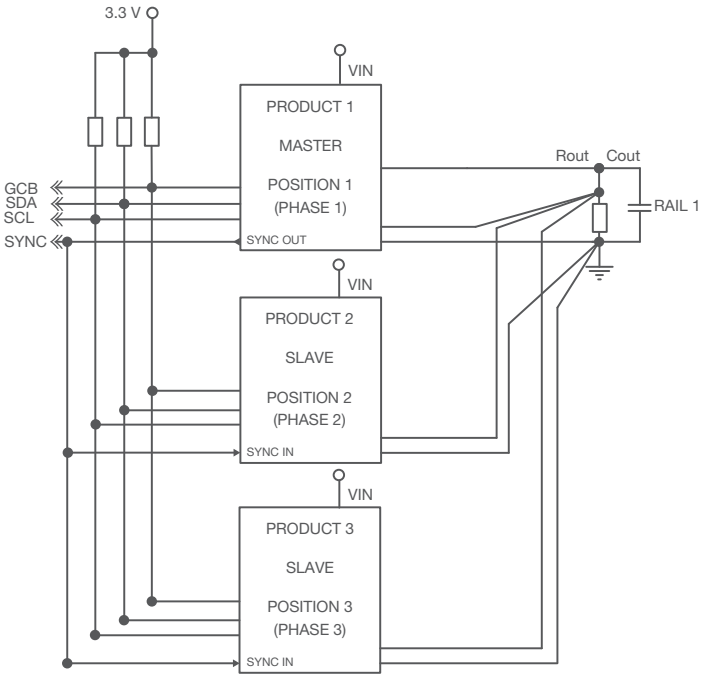

Figure 1. A three-phase current sharing group. The GCB line is common across all phases, and the common Sync clock is generated by the master phase.

Understanding Droop

In most load-sharing applications, there needs to be a way for the individual phases to share load in proportion to their capacity. Ideally, the voltages across phases would operate at exactly the same voltage at all times. In practice though, manufacturing variations and the board design can lead to small differences in the actual output voltage. These small differences, when applied to regulators operating in parallel, creates current loss where a regulator with a higher voltage is supplying current to the other regulator(s). Figure 2 shows a simple example where one voltage source has a slightly different voltage by 5 mV, which causes a current imbalance of over 4 Amps.

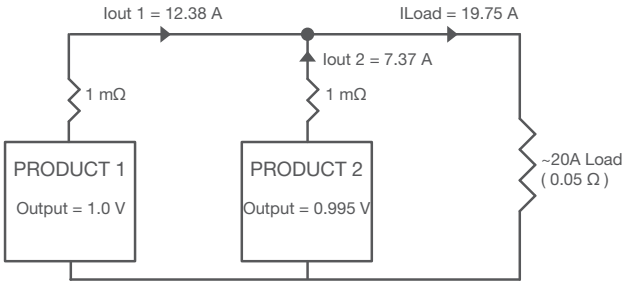

Figure 2. One scenario of current imbalance due to voltage differences.

Even if the regulators themselves are outputting the same voltage, there could be components between the regulator and the load that create variations of the

'loadline resistance', which also create a current imbalance. This can be due to the board layout, current-sense resistor differences, etc. Figure 3 below shows another simple example where a small difference in the loadline creates a current imbalance of nearly 4 Amps.

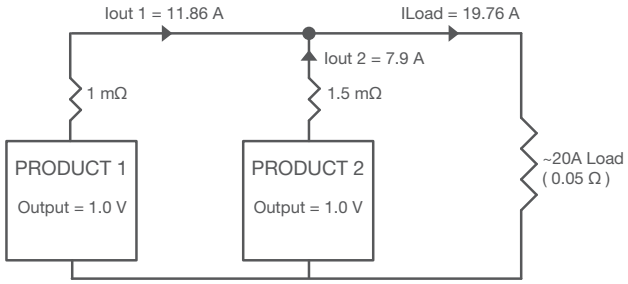

Figure 3. Another scenario where loadline imbalances can also cause current imbalance.

Across a range of loads, these imbalances change and can be visualized by plotting the individual loadlines (or droop) of each phase.

Because the BMR462-464 modules can sense their output voltage, output current while communicating with each other over the GCB bus, they can dynamically trim the output to reduce current imbalances, leading us to "Active Droop Current Sharing".

Current Sharing Algorithm

A specific droop is set based on the application. The droop is set to the same value for each product in the group - that is you assume that the loadline is the same across all phases. Figure 4 shows an example where each product's droop, or loadline, was set to 1 mV/A. Note that the graphs and the x axis represent the individual loadline of each product, not the loadline of the group. Due to differences in layout and component variances the actual loadlines contain slope differences and lead to a current imbalance; they are exaggerated in this example.

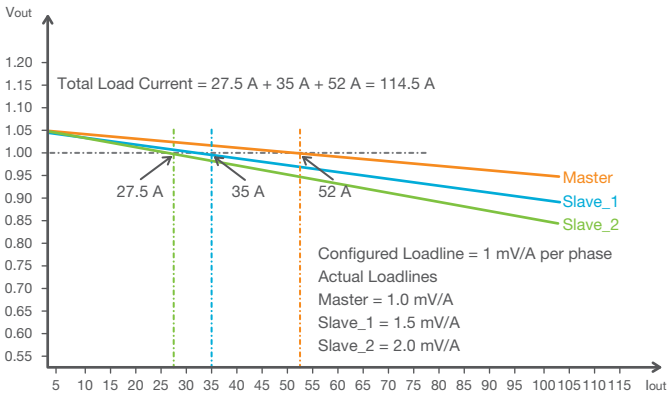

Figure 4. Unbalanced phase currents due to slope error.

The minor imbalance results in each phase contributing an unequal portion of the load current. With Active Droop Current Sharing, The imbalance is detected as the Master's load current is broadcast and each Slave's reference voltage is trimmed up or down until all products in the group carry an equal portion of the load current:

$$V_{Member} = V_{OUT} + Droop_{Phase} \times (I_{Reference} - I_{Member})$$

This effect is shown in Figure 5. Notice in this case the Master initially sourced the majority of the load current. Each Slave's reference voltage was trimmed in the positive direction until all phases source equal current to the load.

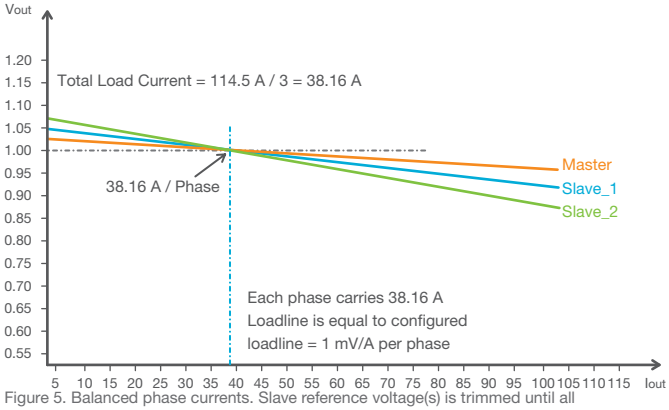

Figure 5. Balanced phase currents. Slave reference voltage(s) is trimmed until all products' currents equalize.

Current sharing equilibrium is shown in Figure 6 with a singular loadline being plotted that represents the actual static response for the sharing group. This loadline is maintained even when phases are added or dropped.

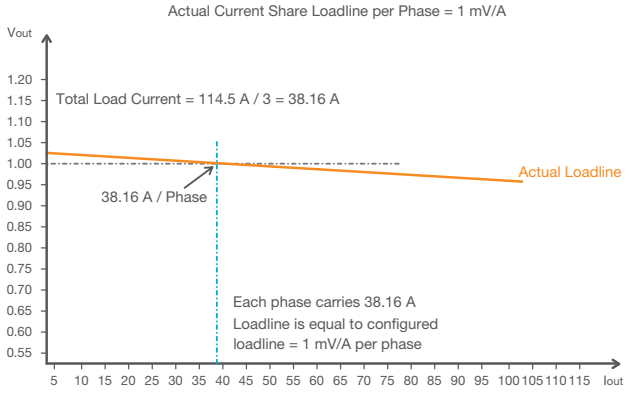

Figure 6. Current sharing phase balance is achieved.

Current Balance Accuracy

The actual current supplied by each product in a sharing group in steady state will not always be equal due to the current monitoring accuracy of each product. The current monitoring accuracy (see Technical Specification for each product) in turn will depend on the trimming of each product in production as well as varying with operating conditions such as input voltage, output voltage and temperature. The products have been designed to operate beyond rated output current in order to support 100% of rated output current from each product in a sharing group (e.g. three 40 A products in parallel support 120 A output current).

The current monitoring accuracy should be taken into account when considering the output current derating and thermal operating conditions of a current sharing group.

Turn-On and Turn-Off

Turn-on and turn-off of a current sharing group may be controlled in two ways.

1. CTRL pin. The CTRL pin of all products in the current sharing group should be connected and be controlled from the same source.

2. PMBus enable. Sending a PMBus Enable command to any of the products in the group will enable the whole group, as the module will 'broadcast' enable to phases over the GCB bus as shown in Figure 7.

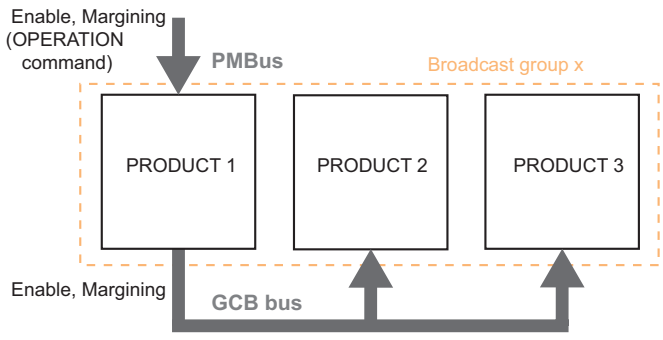

Figure 7. Enable or margining signal will broadcast on the GCB bus.

In either case, the products must be setup for Broadcast Enable and Margining (found in the MISC_CONFIG command), which is automatically set when using the Ericsson Power Designer software.

Ramp Synchronization

During turn-on and turn-off the voltage ramps of each phase are synchronized to start at the same time. This ensures that inter-phase circulating currents are minimized. Each product contains a separate digital controller that executes firmware. The individual controller firmware requires synchronization prior to ramp events to minimize circulating currents. This is accomplished by forcing the Master phase to wait at least one additional firmware cycle during ramping events by configuring it to have additional TON_DELAY time and TOFF_DELAY relative to the other group Slaves. This additional delay is automatically set when using Ericsson Power Designer.

When the sharing group receives a CTRL pin or PMBus enable, the Slaves initialize their registers but wait for the Master to send a message before enabling. Once the Master phase completes its extra timing delay it transmits a GCB Ramp Flag and all products of the group produce a sequenced PWM and begin their soft-start routine. Timing diagram shown in Figure 8.

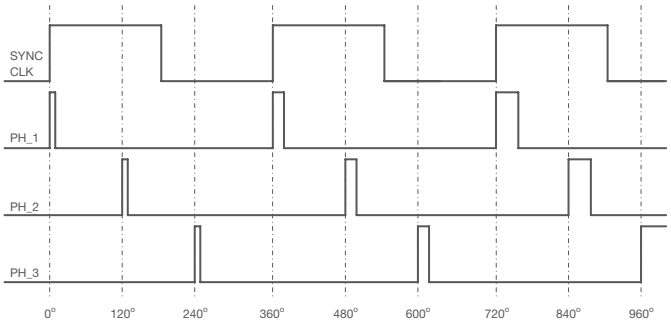

Figure 8. Start-up synchronization.

Minimum Duty Cycle

Current sharing groups can be comprised of 2 to 7 products. Each product contains its own digital PID controller. To ensure that each controller produces an identical pulse width at turn-on the products must be configured for minimum duty cycle in the USER_CONFIG register. This starts each product in the group with the same initial pulse width. The actual configured rise time is conserved as shown in Figure 9.

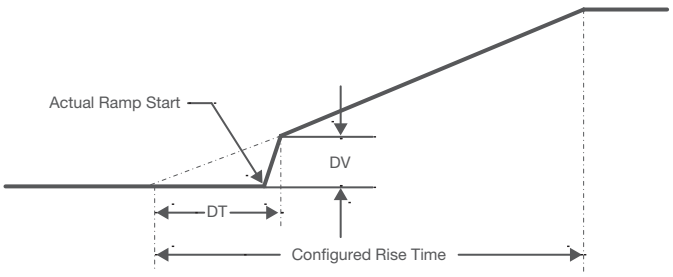

Figure 9. Turn-on rise time profile

The magnitude DV in the beginning of the ramp caused by the minimum duty cycle will increase with input voltage and switch frequency. The inrush current through the inductors may in some applications cause a small distortion in the beginning of the ramp as shown in Figure 10.

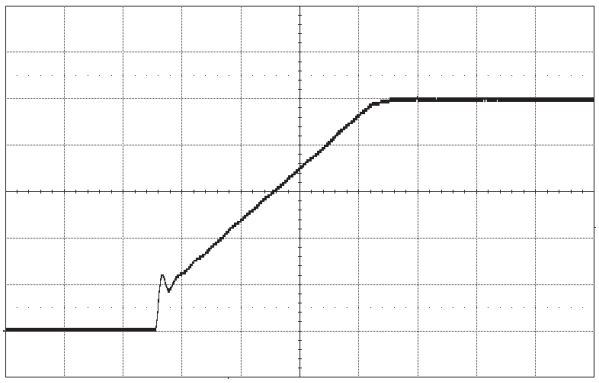

Figure 10. Effect of minimum duty cycle at ramp-up.

Ramp Behavior

The products use a unique ramping algorithm in current sharing configuration that results in near perfect current sharing while ramping. This is accomplished by deriving different compensator coefficients for ramping than those used for steady-state operation. The PID taps for ramps are not user configurable. The ramp compensation is derived from the configured rise/fall time, input voltage, output voltage and switching frequency. During ramp the loop bandwidth is intentionally set to a very low value so response to transients will be limited. The user should limit dynamic loading while ramping.

Once the ramp is completed the controllers of the products will switch to the configured compensator as defined in the used configuration. The switchover takes place at the moment when the PG (power good) signal is asserted. The user has control over the switchover by configuring the PG delay. While ramping down, the switch over takes place before the TOFF delay timer starts.

Ramp Time Accuracy

The unique ramping algorithm used in current sharing restricts the rise and fall times to a maximum value. The low bandwidth ramp technique limits the resolution of the rise and fall times. The ramp time accuracy and the maximum limit will depend on the configured switch frequency, input voltage and output voltage. The maximum limit is automatically calculated and handled within Ericsson Power Designer.

Fault Handling

If one or more products in a current sharing group fault, the remaining phases will continue to operate (the product with the next lowest position becomes the new Master). Automatically adding back faulted phases into the group, i.e. restarting of individual products in the group due to a fault, is not supported. If the products in the group have one or more fault responses configured for restart (which is the default setting for BMR462-464), a synchronized restart of the whole group will occur only after all phases have shut down due to faults.

Automatic Phase Distribution

Common SYNC Clock

As mentioned earlier, a current sharing group requires a common SYNC clock across all phases, as shown earlier in Figure 1. This SYNC clock can be provided internally by one of the products in the group (typically the master phase) or by an external source. The SYNC output can be configured as push-pull or open-drain. All other products connected to the SYNC source must be configured as SYNC inputs. If using an external source, the switching frequency of each product must be configured to the same value as the external source.

Phase Distribution

By default, a current sharing group's phases are evenly distributed over a maximum phase offset of 360 degrees. This method is used when the INTERLEAVE command is set to all 0's on all member phases.

For example, if we evenly distribute the phase offsets of a 3-phase current sharing group (shown in Figure 1), the offset between each phase will ideally be 120 degrees. The actual phase offset is represented by a 4 bit binary number, which provides 16 possible offset values in 22.5° steps. The real phase displacement will be rounded to the closest 22.5° increment. The actual offsets for the 3-phase rail are in Table 1, and all possible phase displacements are shown in Figure 11.

In cases where multiple parallel rails are part of the power system, one may want to customize the phase offsets. The Ericsson Power Designer makes phase spreading simple to customize and visualize, as discussed later in the section "Parallel Rail Customization".

	Ideal Offset	Actual Offset
Position_1	0°	0°
Position_2	120°	112.5°
Position_3	240°	247.5°

Table 1. Ideal vs actual phase offset.

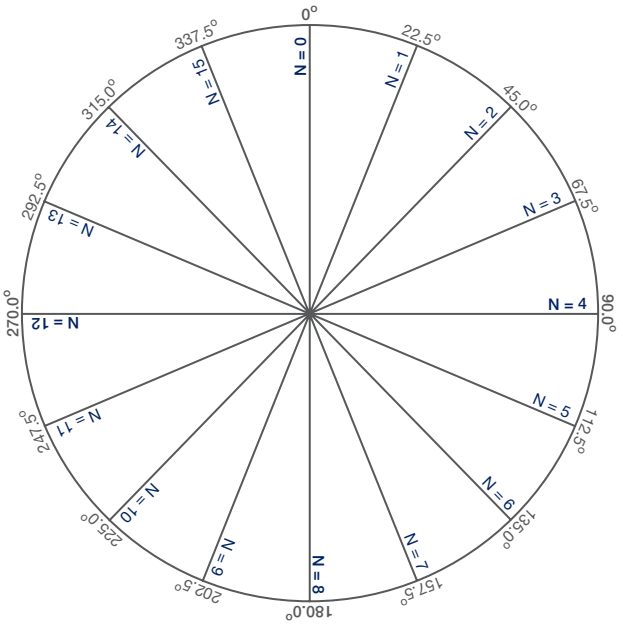

Figure 11. Phase offset resolution wheel.

Phase Add/Drop

When products are configured in a current sharing group, individual products are capable of (dynamically) dropping out and adding back to the group. Phases are typically dropped or added to improve efficiency or to process a fault. Phases can be added or dropped on the fly using a separate power management host controller by invoking the PHASE_CONTROL command (and setting Phase Control Select in the MISC_CONFIG command to use the PHASE_CONTROL command). Even though a dropped product stops switching the operation status of the product will be Enabled and the duty cycle read (command READ_DUTY_CYCLE) will be unchanged.

Phase Drop

If the dropped phase was the group Master a new master will be reassigned based on the lowest sharing group position number of the existing operational products. However if the dropped Master was supplying the SYNC clock it will continue to do so. The group position is defined by the angular offset relative to the SYNC clock and will autonomously redistribute based on the standing phases.

Figure 12 shows an example of a functional 3-phase current sharing group prior to the dropping of the Master (Product 1). Figure 13 illustrates the new 2-phase configuration after the Master phase is dropped. Product 2 becomes the new Master for current sharing. Product 1 supplying the SYNC clock continues to do so. The timing diagram is shown in Figure 14. After the Master phase is dropped the remaining two phases are redistributed and the phase displacement changes from 120° to 180°.

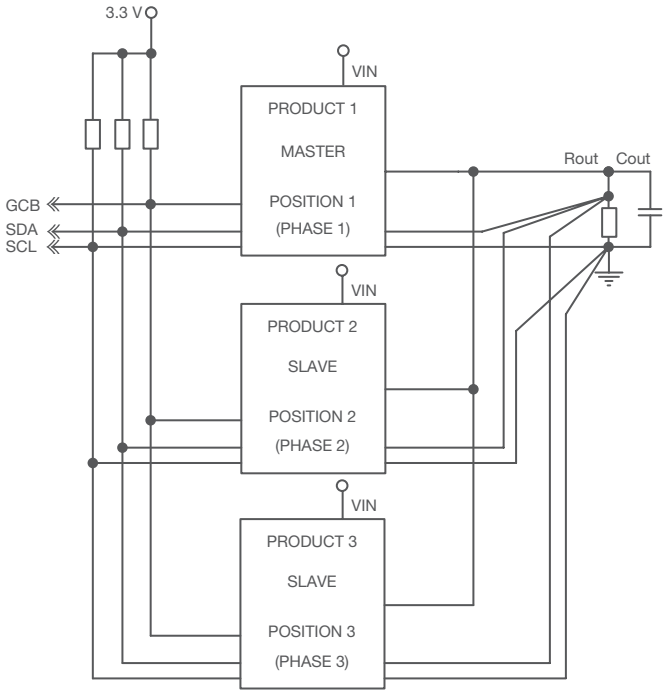

Figure 12. 3-phase converter showing master, slave and position number.

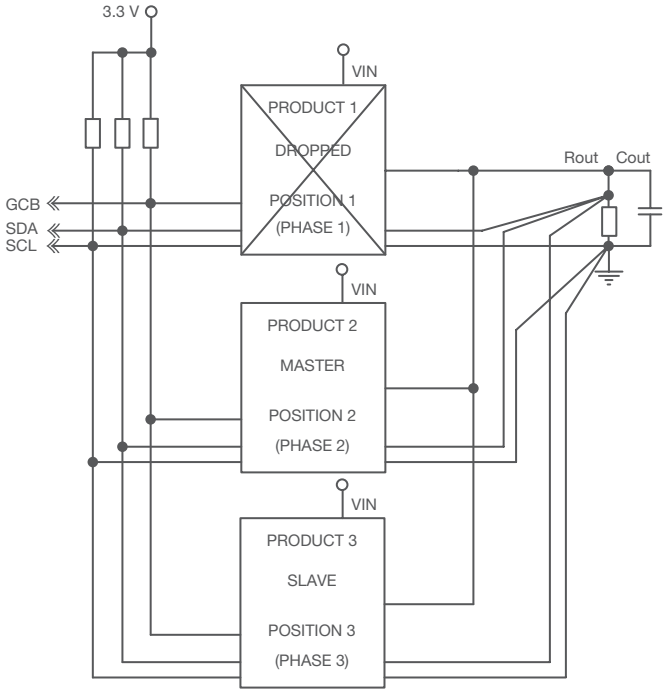

Figure 13. 3-phase converter after master phase is dropped.

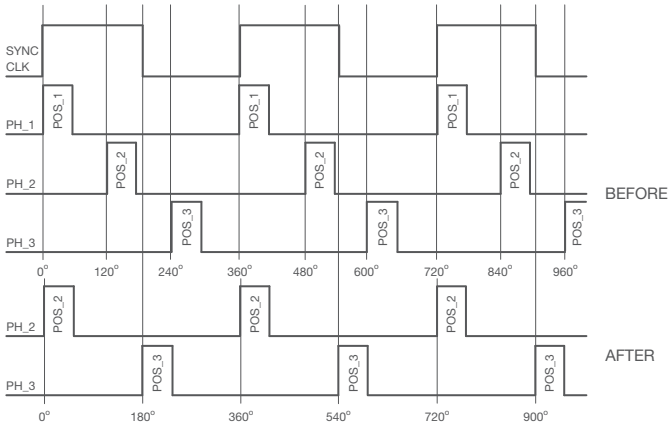

Figure 13. 3-phase converter after master phase is dropped.

Phase Add

The phase that was previously dropped may be added back into the group as determined by the power management host. When the adding is performed, the event is coordinated with the active group products over the GCB bus and the previously inactive product is added back into the group. In this example, Product 1 (from figure 12) was made active and resumed the role of being Master. The phase offset of each group product was automatically redistributed from 180° to 120° - essentially the reverse action of Figure 13.

Dropped Phase and SYNC Clock

If the dropped group product was supplying the SYNC clock it will continue to do so even though it has become inactive. If the product supplying the SYNC clock dropped from the group and is no longer capable of supplying the clock, the remaining members will detect the absence of SYNC and respond according to their fault spreading configuration. If a host or power system manager is monitoring SALERT, the PMBus can be read and the products will respond with the appropriate fault management alarm as described in the PMBus Power System Mgt Protocol Specification – Part II.

Output Voltage at Phase Add/Drop

When adding or dropping a phase there will be a small deviation to the output voltage due to the droop change. Since the effective droop value for the whole group is maintained the individual droop of each phase must change. For example in a sharing group of four phases and an effective droop of 0.25 mΩ, each phase has an individual droop of 1 mΩ. When dropping one of the phases the individual droop of the still active products is maintained at 1 mΩ for a short period of time, resulting in an actual effective droop of 0.33 mΩ. Figure 14 shows the example when the output current is 100 A, giving a deviation of 8 mV. When adding a phase back to the group there will be a deviation due to the same reason but in that case the output voltage will increase instead of decrease. In any case, the deviation will always be within the voltage drop range defined by the configured total droop. Note that the output voltage is also affected by the load step that occurs for active products during a phase add or drop.

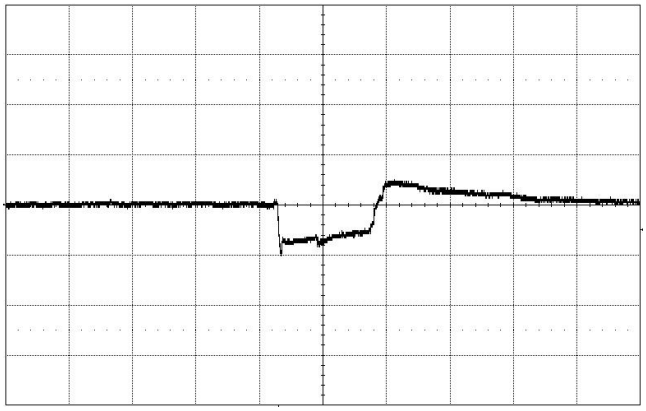
Figure 14. Example of output voltage deviation during drop (10 mV/div, 10 ms/div)

NLR Threshold Scaling

When multiple products are configured in a current sharing group, the effective output ripple is (ideally) divided by the number of active group products. This means when all products in the group are operating, the NLR (Non Linear Response) thresholds can be set to a smaller value just above the minimum ripple amplitude. When a phase is dropped the ripple amplitude will increase.

In order to avoid spurious NLR activity the products automatically adjust the NLR thresholds according to the ratio of active group products to total products of the group:

$$Threshold_{Drop} = Threshold_{Config} \times \frac{N_{All}}{N_{Active}}$$

Where $Threshold_{Drop}$ is the NLR inner threshold setting used when some group products are dropped.
$Threshold_{Config}$ is the NLR inner threshold setting configured for the group products.
N_{All} is the total number of products in the sharing group.
N_{Active} is the number of products active in the group (products not faulted or intentionally deactivated).

N_{All} and N_{Active} are determined automatically from the group configuration parameters. No additional programming or configuration is required. Since the available thresholds are quantized to multiples of 0.5% of the configured output voltage, the next higher available threshold is used if the result of the above formula is fractional.

PARALLELING WITH ERICSSON POWER DESIGNER

Introduction

Paralleling BMR 462-464 modules requires setting up a number of parameters. While this can be done manually by setting individual commands, it is significantly easier to use the Ericsson Power Designer software to quickly create parallel rails. The software is available for download at digitalpowerdesigner.com.

Creating a Parallel Rail

This section walks through creating a parallel rail using the Ericsson Power Designer. No hardware is required, but this walkthrough project can be loaded onto two BMR 463's using the POL paralleling test board (ROA 128 5077).

Step 1. Open the Ericsson Power Designer and create a new project.

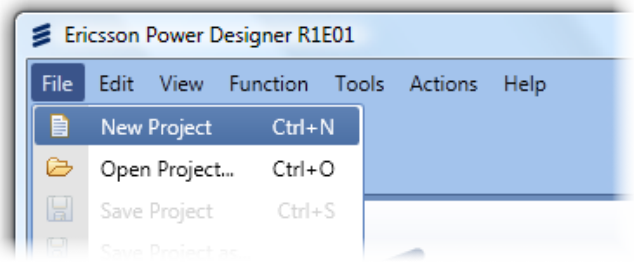

Figure 15. Starting a new project.

Step 2. Add a parallel rail and member phases. Right-click on the "Rails" item in the Configuration Browser.

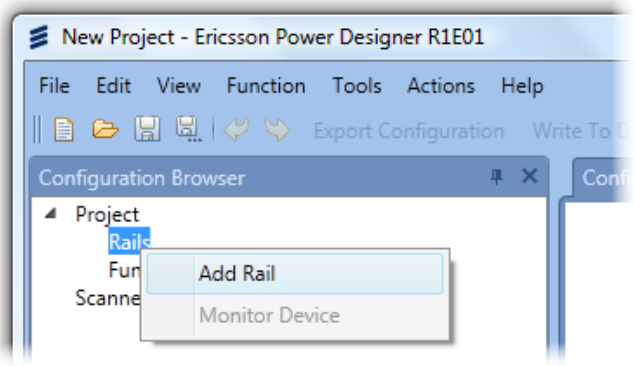

Figure 16. Starting a new project.

After adding the rail, add the phases. In the "Select Product:" field, select a BMR 463 device. Then click the "Add Parallel device" button to add another phase. For this example, we've set the addresses of the phases to 0x58 and 0x59, which are the first two addresses on the POL parallel test board.

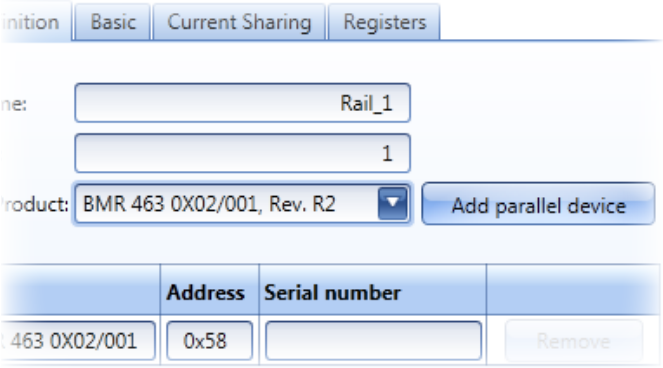

Figure 17. Adding parallel phases with the "Add parallel device" button.

After adding the parallel devices, your rail's configuration should look as shown below.

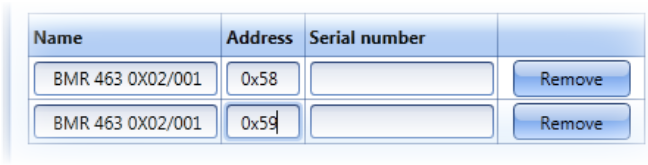

Figure 18. Configuring parallel phase addresses.

Step 3. Now that the parallel rail is defined, we just need to configure its settings. First, while droop is usually configured automatically, you may optionally change the droop, which is automatically calculated evenly across phases and adjusted during phase add/drop events.

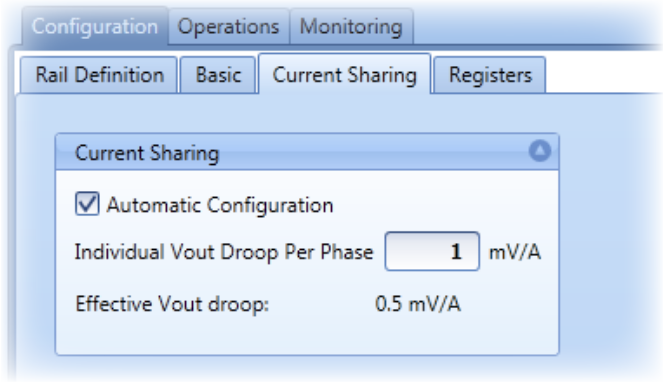

Figure 19. Current sharing droop settings.

Step 4. Outside of the optional droop setting, all we need to set in this example is the Rail's VSET resistor, which is 3.3V (the POL parallel board default across all phases). The setting is found on the 'Basic' configuration tab as shown in Figure 20. You may also configure custom voltages, timing, and fault settings here as well.

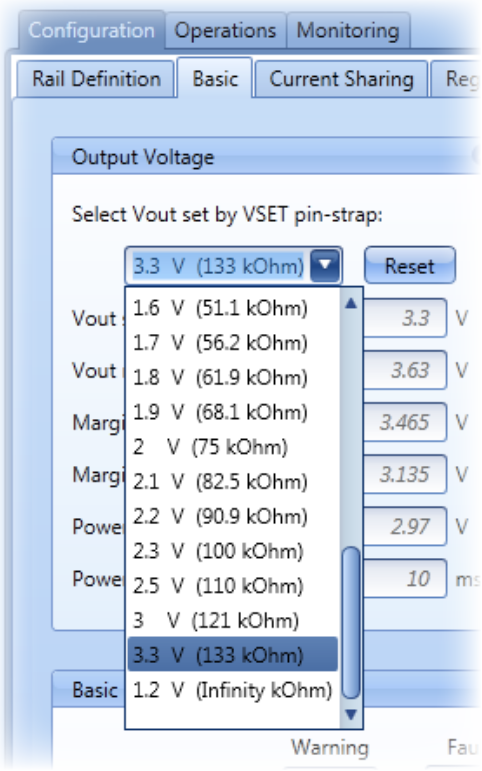

Figure 20. Setting the default voltage expected from the VSET pin. PMBus set voltages/ faults/timings can also be set on this tab.

Step 4. If you are going through this walkthrough with a POL parallel test board, you can load the project onto the devices. Setup the board as shown in Figure 21 below, then power it and connect the USB-PMBus Adapter to the board.

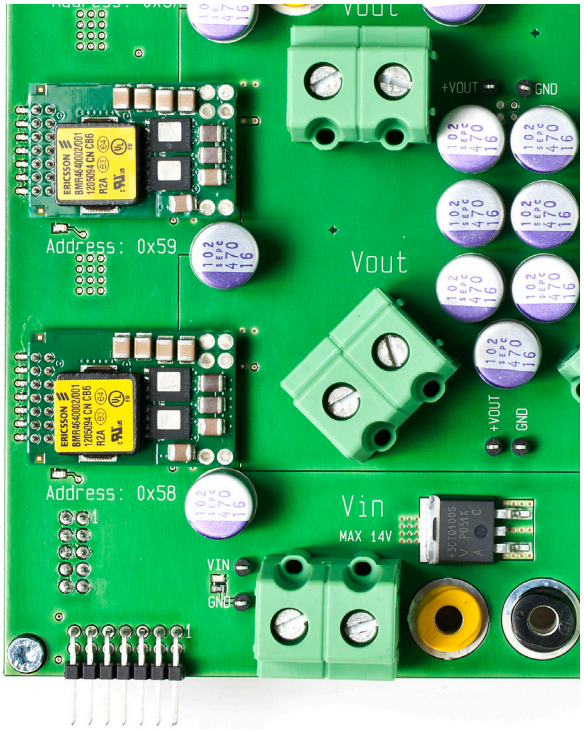

Figure 21. POL parallel test board setup for this example - two BMR463 modules at addresses 0x58 and 0x59.

After the board is powered and connected, ensure that the CTRL switch is off. Then write the project to devices by first selecting the “Project” in the Configuration Browser, then click the “Export Configuration” button in the toolbar. After doing this, use the export menu to ‘export’ the project to devices using the USB Adapter.

Paralleling Made Simple

The previous example only took a few steps with an entirely new project. This is because the software automatically sets the commands required for parallel operation. You can see which commands have been automatically set by either going to the registers tab, or by going to the Export menu and previewing the commands sent to the parallel rail. The command preview for this example is shown in Figure 22.

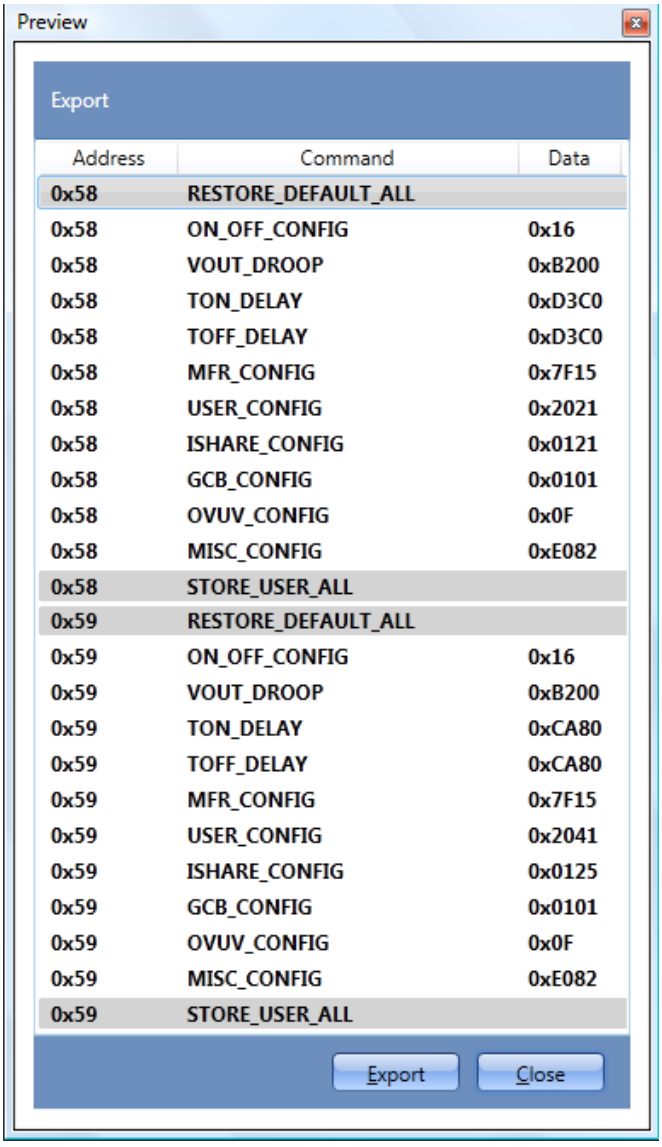

Figure 22. Settings automatically set by Ericsson Power Designer for the parallel example.

A full explanation of the automatically set commands is provided in Appendix I.

PARALLEL RAIL CUSTOMIZATION

While the Ericsson Power Designer sofware takes care of a number of steps in setting up a parallel rail, there are a few custom scenarios where you will need to modify settings.

This section covers the scenarios of optimizing phase offsets when having multiple parallel rails, configuring a parallel rail to track an output voltage, and optimizing loop compensation.

Optimizing Phase Offset with Multiple Parallel Rails

Earlier in the section “Automatic Phase Distribution” we covered how parallel rails can have its phases evenly distributed. In cases with multiple parallel rails however, one may want to optimize phase spreading further to reduce input ripple.

Example: Interleaving two two-phase parallel rails

In the example shown in Figure 24, we have two two-phase parallel rails with a shared VIN. If we left phase-spreading to be automatic, we will have two phases operating at a 0 degree offset, and two phases at a 180 degree offset, as shown in Figure 25.

Ideally we want all phases evenly spread across the parallel rails, such that each phase operates at a 90 degree offset. To do this, we’ll introduce a 90-degree phase offset to the second parallel rail, which will result in the timing shown in Figure 26.

Doing this is very simple with Ericsson Power Designer. Let’s assume we’ve already created two two-phase current sharing rails, as shown in Figure 23 below:

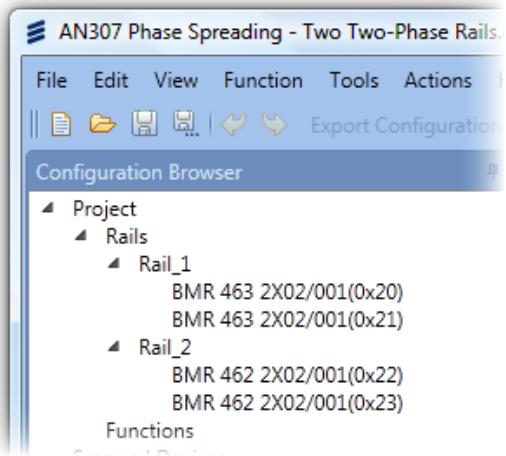

Figure 23. Example of 2 x 2-phase current sharing groups in Ericsson Power Designer.

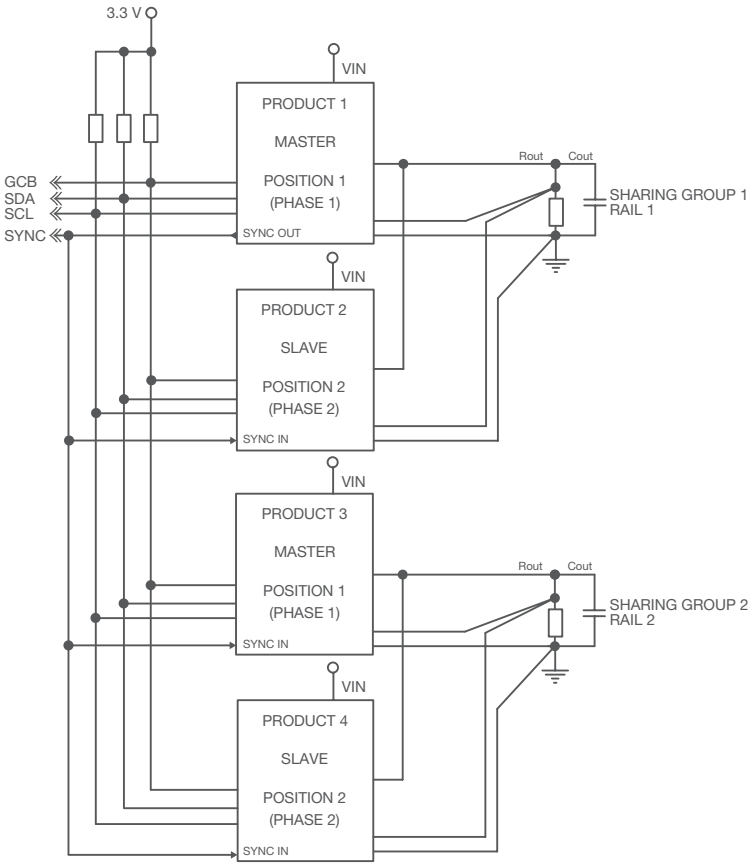

Figure 24. Example of 2 x 2-phase current sharing groups using the same SYNC clock.

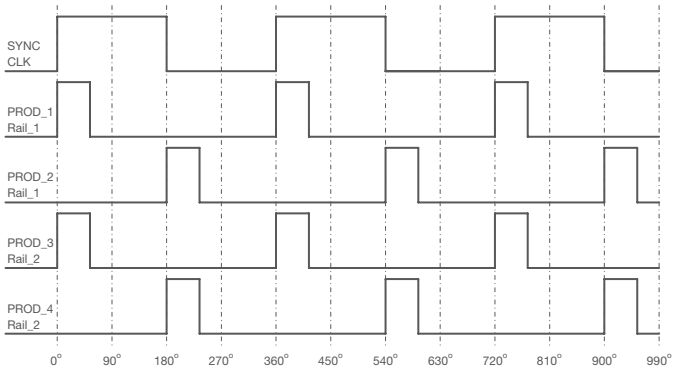

Figure 25. Timing diagram for a 2 rail x 2-phase current sharing example.

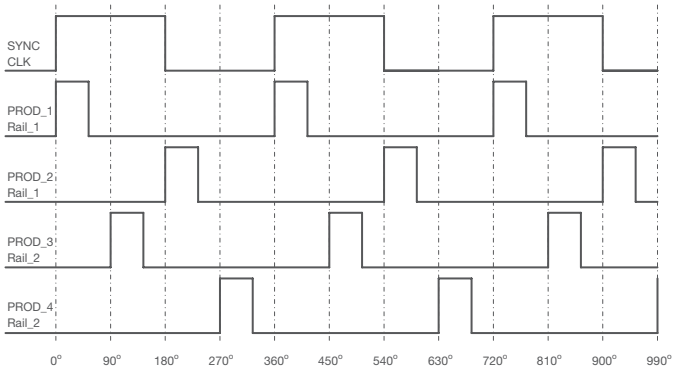

Figure 26. 2 x 2-phase current sharing groups now equally offset using the INTERLEAVE command.

Now, to change the phase spreading setup, add a phase spreading function by right-clicking in the functions item, as shown in Figure 27.

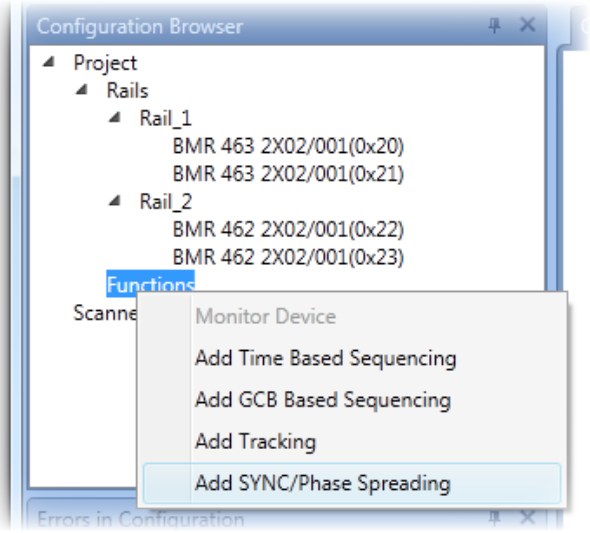

Figure 27. Adding a phase spreading function to the EPD project.

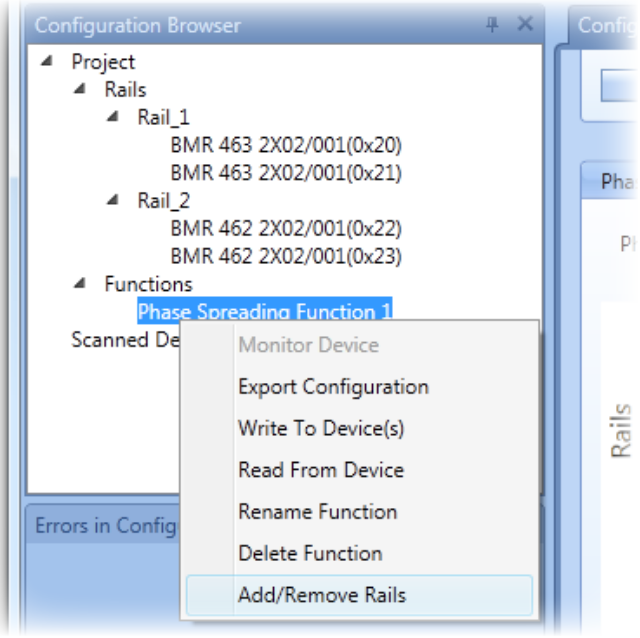

Figure 28. Adding rails to the phase spreading function

Then add the two current sharing rails to the phase spreading function, as shown in Figure 28.

Adding both rails will show phase spread settings as shown in Figures 29 & 30X

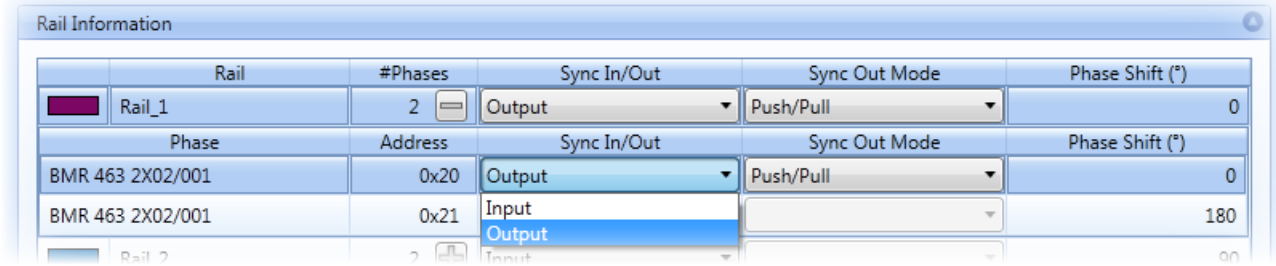

Figure 29. Changing the first rail's master phase to be the common sync output.

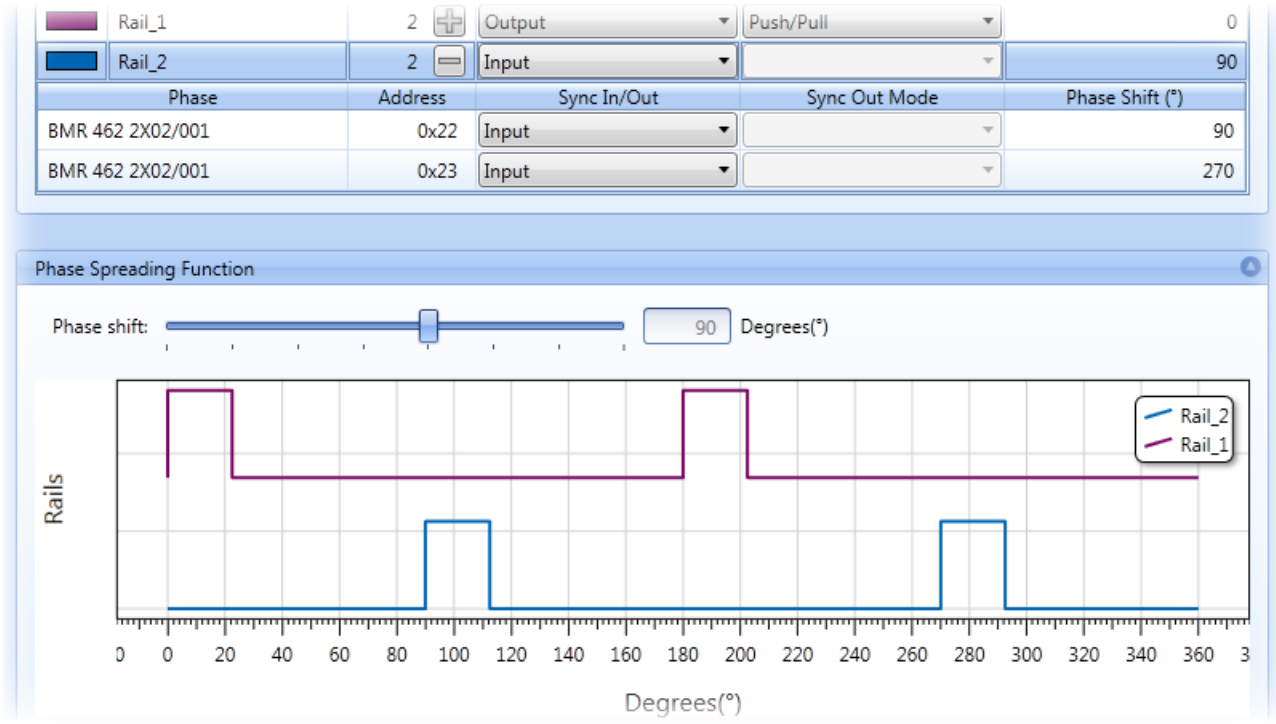

Figure 30. Adding a 90-degree phase offset to the second rail to have balanced interleaving.

Phase spreading, just like current sharing, depends on a common sync signal. In this case we make the first phase of the first rail the SYNC signal output. This is done by expanding the first rail's phases (by clicking the '+' button), and changing the first phase's Sync to be a Push-Pull output, as shown in Figure 29. All other phases in this system are setup as SYNC inputs.

After this, we introduce the 90 degree phase offset by selecting the second rail, then moving the "Phase shift" slider to be 90 degrees (seen in Figure 30). If you expand the second rail's phases, you will notice that EPD will shift both phases by 90 degrees, resulting in the second rail's first phase with a 90 degree phase shift, and the second phase with a 270 degree phase shift.

NOTE: When making sync-related changes, it is recommended that you power-cycle the modules after writing their new settings. Never attempt to change sync related settings while the device is regulating.

Behind the scenes, EPD is introducing the phase offset by modifying the INTERLEAVE command. For this example, the INTERLEAVE command is modified such that the number of group members is set to 0, which translates to 16 on the BMR462-464, to make phase positions serve as 360/16 = 22.5 phase increments. It also sets INTERLEAVE's 'position in group' setting to 4, which creates a 22.5 * 4 = 90 degree phase offset. The INTERLEAVE setting can be found inside the registers tab.

Optimizing Compensation

compensation analysis and divide the resulting total capacitance by the number of phases. The resultant filter consists of the phase output inductor and the equivalent phase capacitance. Consider the 3-phase example shown in Figure 31. This schematic is drawn symmetrically with identical phase filters; considering any one of the phases plus any common output capacitance divided by the number of phases. The resultant 3-phase compensation model reduces to the configuration shown in Figure 32.

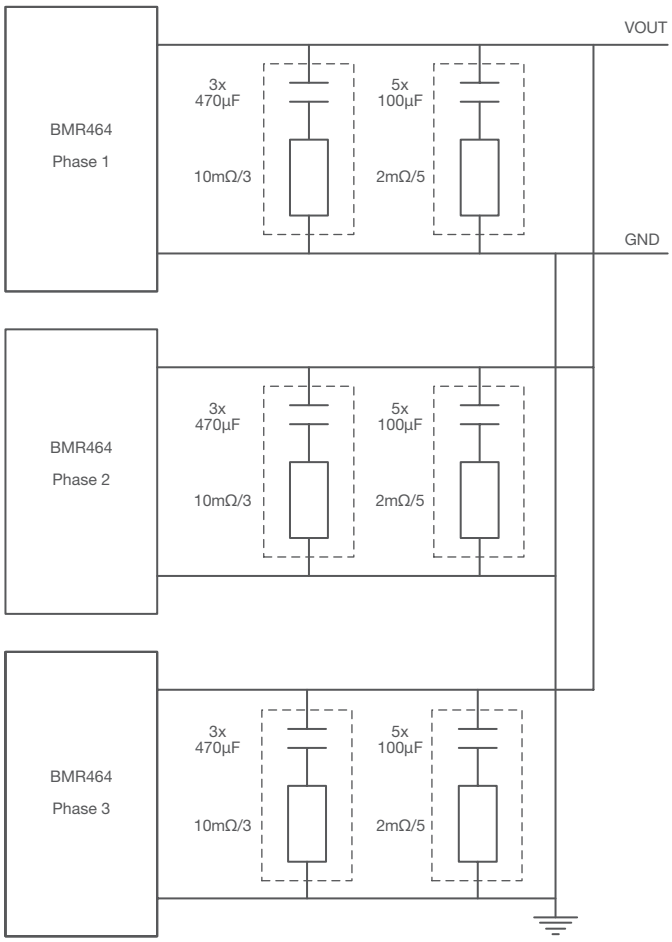

Figure 31. 3-phase current sharing example.

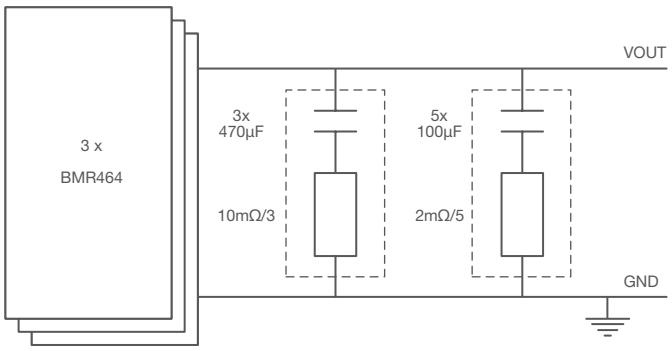

Figure 32. Current sharing compensation model.

Voltage Tracking

For current sharing groups voltage tracking is emulated by configuring the output ramp to match the ramp of the VTRK voltage. Doing this affects how the Rise/Fall times should be set along with the power-up delay times.

NOTE: Voltage tracking with a pre-bias voltage at the output is not recommended since there is risk of phase currents to drift apart.

Setting Delay Times

The power-on delay time for the reference (i.e. tracking master) voltage needs to be long enough for the tracking rail (i.e. tracking slave) to be ready for the ramp-up. The power-on delays should follow this formula:

$$Ton\ Delay_{TrMstr} \geq Ton\ Delay_{TrSlave} + 7ms$$

For power-off, the delay times should be set such that the tracking slaves follow the entire rampdown of the tracking master, using the following formula:

$$Toff\ Delay_{TrSlave} \geq Toff\ Delay_{TrMstr} + Toff\ Fall_{TrMstr} + 7ms$$

Setting Rise/Fall Times

The rise/fall times should be set following this formula:

$$T_{RISE/FALL} = 1.1 \times T_{RISE/FALL\_VTRK} \times \frac{V_{OUT}}{VTRK} \times \frac{1}{Tracking\_ratio}$$

Note that the formula allows configuring of any tracking ratio, simply by adjusting the rise/fall time (tracking ratio should always be set to 100% in TRACK_CONFIG). Example: To configure a 1.2 V current sharing rail to track a 3.3 V voltage with ramp time 5 ms, by tracking ratio 50%, the ramp time of the products in the current sharing group should be set to 1.1 x 5ms x (1.2V / 3.3V) x (1 / 0.50) = 4 ms.

The ramp time can be adjusted upwards to improve the current sharing balance during the ramp, or downwards to improve the accuracy of the tracking ratio.

Voltage Tracking Example

Let's assume we have a 2-phase current sharing rail created in Ericsson Power Designer, and also have a Rail serving as a tracking master,
as shown in Figure 33.

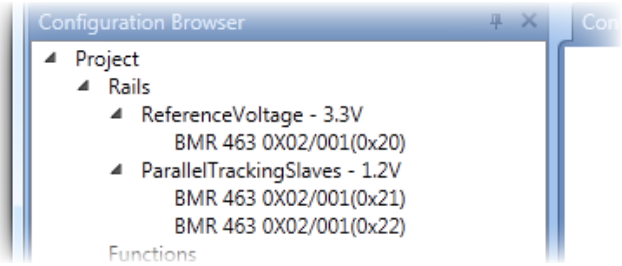

Figure 33. Power System with a parallel rail that will track a reference voltage.

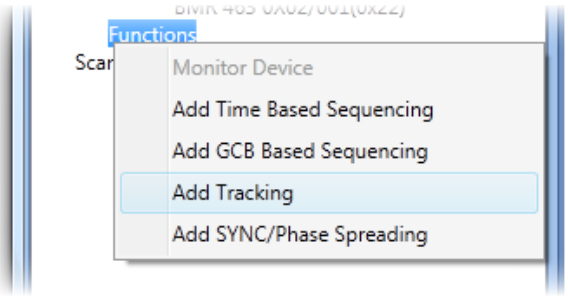

Figure 34. Adding the voltage tracking function.

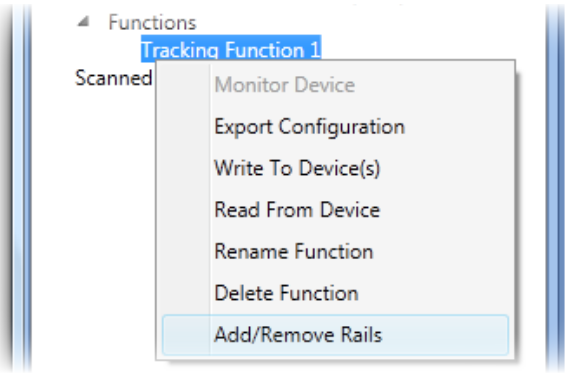

Figure 35. Adding rails to tracking function.

To add voltage tracking, use the functions menu to add a the tracking function (shown in Figure 34). Then add both rails to the tracking function (see Figure 35). Once this is done, the timings of the tracking setup can be set.

In this example, we follow the delay equations in the previous section such that the reference Ton Delay = 22ms = 15ms + 7ms. For the tracking rail's Toff Delay, we have 17ms = 0ms + 10ms + 7ms.
Finally, for the rise/fall times, we have 8ms = 1.1 x 10ms x (1.2V / 3.3V) x (1 / 0.50).

Rail	Is Master	Scale	Uplimit Voltage	Track Sag Always	On Delay [ms]	On Rise [ms]	Off Delay [ms]	Off Fall [ms]
ReferenceVoltage - 3.3V	◉	100%	Target	☐	22	10	0	10
ParallelTrackingSlaves - 1.2V	○	50 %	Target	☐	15	8	17	8

Figure 36. Tracking function configuration.

LAYOUT CONSIDERATIONS

The PWB layout and placement of output capacitances should be made as symmetrical as possible between the products in a current sharing group, as illustrated in Figure 37. This is to minimize loadline differences, improve ripple cancelling and even up the control loop response of each phase. For the same reason VOUT connections should be as low impedance as possible.

Each product in a current sharing group must use the same point for voltage sense. It is recommended that the traces for the voltage sense lines are routed as a differential pair in order to minimize the sensitivity to disturbances. Adding a small decoupling capacitor between the voltage sense lines close to the products is a good design practice.

Output capacitances should be placed close to the load while input capacitances should be placed close to the product.

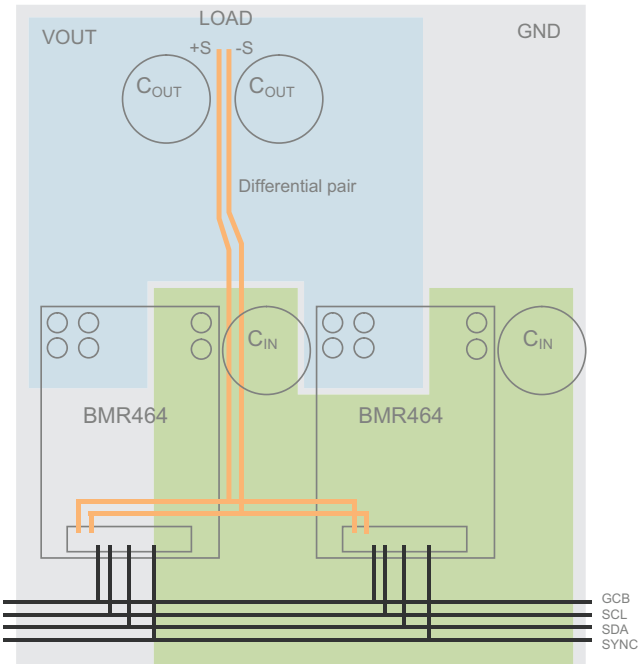

Figure 37. Layout example, two products.

APPENDIX 1: PARALLEL SETTINGS AUTOMATICALLY CONFIGURED BY ERICSSON POWER DESIGNER

The Ericsson Power Designer software automatically does the following steps when setting up a parallel rail. These steps are done across all phases in the parallel rail unless otherwise noted.

If one is configuring modules without Ericsson Power Designer, these steps should serve as a checklist with more command information provided in Appendix 2.

1. Enable ramp-down during disable (i.e. Set bit 0 in ON_OFF_CONFIG to 0).

2. Disable crowbarring from occurring during an OV FAULT (i.e. Set bit 7 in OVUV_CONFIG to 0).

3. Enable Alternate Ramp Control (i.e. Set bit 2 in MFR_CONFIG to 1).

4. Enable a Minimum Duty Cycle of FSW/256 (i.e. In USER_CONFIG, set bit 13 to 1, and set bits 15:14 to 00).

5. Designate and configure SYNC source for the group. By default, the software configures the master phase to output SYNC, and slave phases to be SYNC inputs. Products not sourcing SYNC must be configured as SYNC inputs (all products in the group must use the same SYNC signal) (affects MFR_CONFIG bit 0, USER_CONFIG bits 6 & 5).

6. Disable Precise Ramp Up Delay (i.e. Set bit 7 MISC_CONFIG to 1).

7. In ISHARE_CONFIG,
   - Assign the same “group number” setting.
   - Enumerate the member position across phases, the master phase will be set to Member Position 1.
   - Assign the same “number of devices” setting.

8. Ensure that the TON_DELAY and TOFF_DELAY times for the Master are at least 10 ms greater than the corresponding delay parameters of each Slave, with a minimum required delay of 15ms. Delay parameters must be greater than 5 ms. Delay parameters should be the same value across all slave phases. If using tracking, please check the section “XXXX” for more information on how TON_DELAY and TOFF_DELAY should be set.

9. Set Broadcast Enable and Broadcast Margin to both be enabled (i.e. Set bits 15 & 14 in MISC_CONFIG to 1).

10. Ensure that the Broadcast Group set in GCB_CONFIG is the same across all devices. It should typically be set to 0 across all rails.

11. Set INTERLEAVE to all 0’s. This enables automatic phase-spreading for current-sharing groups. In cases where custom phase-spreading is needed, this value should be changed as guided in section “Parallel Rail Customization” of this app note.

12. Ensure that the following values are the same across all phases. The software ensures these values are the same by restricting the user from changing values on individual phases.
    - Ramp Timing (TON_RAMP & TOFF_FALL).
    - Fault Thresholds and Responses.
    - Droop/Loadline resistance settings (VOUT_DROOP).
    - Compensation-related parameters (PID_TAPS, NLR_CONFIG).
    - Broadcast Group in GCB_ID.
    - INTERLEAVE.
    - Switching Frequency (FREQUENCY_SWITCH).

APPENDIX 2: PARALLEL COMMAND REFERENCE

The tables below give a detailed description of the configurations required by or related to current sharing modules. Refer to AN302 for a detailed specification of each command.

GCB_CONFIG

Bits	Purpose	Configuration
15:13	Reserved	These bits are not used and should be set to 0.
12:8	Broadcast Group	Typically set to 0 for all devices. For a current sharing group that shall be enabled by the PMBus, the Broadcast Group value must be set the same of each product in the group. If there are other products connected to the same GCB bus, they must also have the same Broadcast Group if any sequencing of fault-spreading functions are used. For more information, see section Broadcast Enable and Margining.
7:6	Reserved	These bits are not used and should be set to 0.
5	GCB TX Inhibit	Set this bit to 0 (default value) for each product in the group to enable GCB communication.
4:0	GCB ID	Sets the rail's GCB ID for sequencing and fault spreading. Assign the same rail GCB ID to each product in the current sharing group. If there are other non-current sharing products connected to the same GCB bus, make sure that those rails have a unique rail GCB ID. This ID value must be the same as the IShare GCB ID set in ISHARE_CONFIG.

Examples:

GCB_CONFIG = 0x0000	GCB_ID = 0, Broadcast Group = 0
GCB_CONFIG = 0x0407	GCB_ID = 7, Broadcast Group = 4

ISHARE_CONFIG

Bits	Purpose	Configuration
15:8	IShare GCB ID	Set to the same GCB ID as in GCB_CONFIG for each product in the current sharing group.
7:5	Number of Member	For each product in the current sharing group, set to the number of products in the group - 1. Example: 3 products in the group use 3 – 1 = 2.
4:2	Member position	Defines position of product in the group. The master with position 1 is assigned value 0 and the slaves are assigned values 1, 2, 3, …
1	Reserved	This bit is not used and should be set to 0.
0	IShare control	Set this bit to 1 for each product in the current sharing group. This enables current sharing.

Examples:
ISHARE_CONFIG = 0x0721 GCB_ID = 7, Position 1 in a group of 2 products
ISHARE_CONFIG = 0x0725 GCB_ID = 7, Position 2 in a group of 2 products

USER_CONFIG

Bits	Purpose	Configuration
15:13	Minimum Duty Cycle	The minimum allowable duty cycle must be enabled to ensure that each phase starts the turn-on ramp with the same pulse width. For each product in the group, enable a minimum duty cycle of FSW / 256, i.e. bits 15:13 = 001.
12	Alternate Ramp Down	Set according to system design requirements. Normally set to 0 for each product in the current group (default value).
11	SYNC Time-out Enable	
10	Reserved	
9	PID Feed-forward Control	
8	Fault spreading mode	If fault spreading shall be used for the current sharing rail, set this bit to 1 for each product in the current sharing group.
7	Reserved	This bit is not used and should be set to 0.
6	Sync Utilization Control	For each product in the current sharing group, except the one that possibly will be used to generate sync clock, this bit shall be set to 1 (force the SYNC pin to be input). For a product that shall be used to output sync clock this bit shall be set to 0.

5	Sync Output Control	Set to 1 for products in the current sharing group that shall be used to output sync clock from the SYNC pin. Make sure the SYNC Output Mode bit in MFR_CONFIG is set according to the system design requirements for these products. For each product in the group that uses the SYNC pin as an input the Sync Output Control bit shall be set to 0 (default).
4:3	Reserved	Set to 0 for each products in the current group (default value).
2	OFF low-side control	
1:0	Standby Mode	Monitoring must be enabled for all products in the current sharing group (bits 1:0 = 01 = default value). This ensures that the firmware is initialized prior to enabling the output voltage.

Examples:
USER_CONFIG = 0x2031 SYNC pin as clock output, fault spreading disabled
USER_CONFIG = 0x2051 SYNC pin as clock input, fault spreading disabled
USER_CONFIG = 0x2151 SYNC pin as clock input, fault spreading enabled

MFR_CONFIG

Bits	Purpose	Configuration
15:11	Current Sense Blanking Delay	This delay parameter controls the blanking time (ns) after switching the top or bottom FET, preventing switch noise from disturbing the current measurement circuit. Normally the default value used for each product will be enough but in some applications an increased value might be needed.
10:8	Current Sense Fault Count	Set according to system design requirements. Normally the default values shall be used for each product in the current sharing group.
7:6	Reserved	
5:4	Current Sense Control	
3	NLR During Ramp	Shall be set to 0 (default) for each product in the current group.
2	Alternate Ramp Control	Shall be set to 1 (alternate ramp enabled) for each product in the current sharing group.
1	Reserved	This bit is not used and should be set to 0.
0	SYNC Pin Output Control	Set according to system requirements (open drain or push-pull output) for products in the group that is configured to output sync clock. For products using the SYNC pin as input this bit can be set to either 0 or 1.

Examples:
MFR_CONFIG = 0x8F14 SYNC pin output as open-drain
MFR_CONFIG = 0x8F15 SYNC pin output as push-pull

If the Current Sense Blanking Delay is increased the read READ_IOUT value will be affected by a small offset. To compensate for this the existing IOUT_CAL_OFFSET value can be changed according to the approximate formula below (it is assumed that bits 5:4 Current Sense Control is unchanged = down slope sense).

$$IOUT\_CAL\_OFFSET_{NEW} = IOUT\_CAL\_OFFSET_{OLD} - \frac{V_{OUT} \times (BlankDelay_{NEW} - BlankDelay_{OLD})}{2 \times L}$$

Where *L* = Output inductor value of the product (model dependent).

MISC_CONFIG

Bits	Purpose	Configuration
15	Broadcast Margin	If broadcast margining or enable shall be used (see GCB_CONFIG) for the current sharing group these bits must be set accordingly. The same setting must be used for each product in the group. Note that Broadcast Enable can be used only when PMBus on/off control is used. If using on/off control by the CTRL pin, the CTRL pin of each product in the group must be connected to the enable signal.
14	Broadcast Enable	
13	Adaptive Compensation	Use default values for each product in the current sharing group.
12	Reserved	
11:10	Current Sense Gain Factor	
9:8	Reserved	
7	Precise Ramp-Up Delay	Shall be set to 1 (=Precise Ramp-up Delay disabled) for each product in the current sharing group.
6	Diode Emulation	Set according to system design requirements. Normally the default values shall be used for each product in the current sharing group. Diode Emulation and Adaptive Frequency is not supported with current sharing and shall be disabled.
5:3	Reserved	
2	Minimum GL Pulse	
1	Snapshot	
0	Adaptive Frequency	

Examples:
MISC_CONFIG = 0x2082 No broadcast functions
MISC_CONFIG = 0x6082 Broadcast Enable activated
MISC_CONFIG = 0xA082 Broadcast Margining activated

VOUT_COMMAND

Each current sharing phase must be set to the same output voltage. Since the droop/current sharing algorithm will need headroom to adjust the output voltage, it is recommended to keep VOUT_COMMAND below 0.96 x VOUT_MAX.

The user might want to increase the nominal output voltage by an offset in order to compensate for the load-line droop. Typically an offset magnitude of 0.5 x I_{MAX} x R_{DROOP} would be used.

VOUT_TRIM

Writing this command will have no effect for products in a current sharing group since the command is used by the current sharing algorithm. The Master phase will always retain a zero VOUT_TRIM value, while each Slave phase will adjust its VOUT_TRIM value until all phases carry equal load current

VOUT_CAL_OFFSET

The VOUT_CAL_OFFSET parameter contains a calibration value from production and should not be changed. If an offset voltage is desired to overcome the effects of droop, the value of VOUT_COMMAND should be adjusted.

VOUT_DROOP

Droop resistance is used as part of the current sharing algorithm. Each product in the group shall be assigned the same VOUT_DROOP value, which will be the effective droop (or loadline) of the whole group. Since the total current is shared between the products in the group, the droop of each individual phase will be set higher than the configured VOUT_DROOP value.

Example for a current sharing group with four products:

VOUT_DROOP value assigned to all four products	0.25 mV/A
Effective droop or loadline of the group output	0.25 mV/A
Effective droop or loadline for each individual phase with all phases active	0.25 x 4 = 1.0 mV/A

The assigned effective droop is maintained even when phases are added or dropped which means the individual droop of each phase is automatically adjusted.

It is recommended to assign a VOUT_DROOP value that gives an *individual* droop between 0.5 and 1.5 mV/A per phase. In general current sharing balance is improved with higher droop. A too high droop may cause instability at high loads. The highest possible droop for stable operation decreases as temperature and output load increases. The graphs in Figure 38 and Figure 39 show the recommended maximum individual droop per phase vs output voltage and maximum output current, assuming operation at a maximum temperature of +95ºC.

In order not to affect the configured over current protection (OCP) threshold; the maximum output current used when defining maximum droop should be equal to the configured OCP threshold.

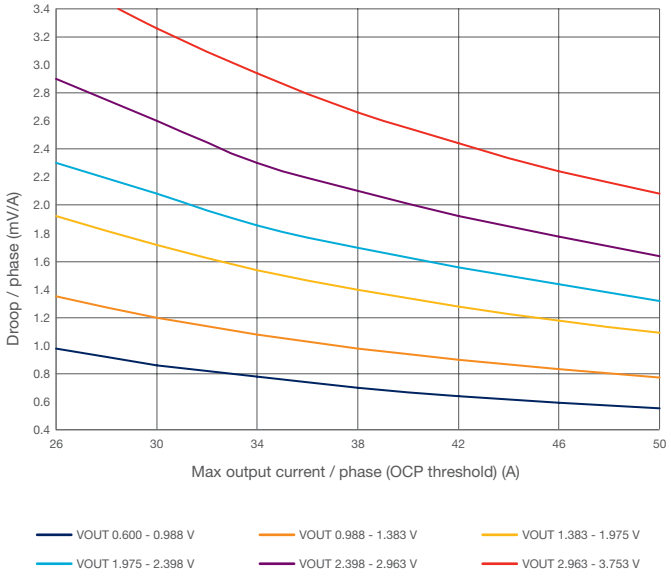

Figure 38. Recommended maximum individual droop per phase vs VOUT and max IOUT for BMR464.

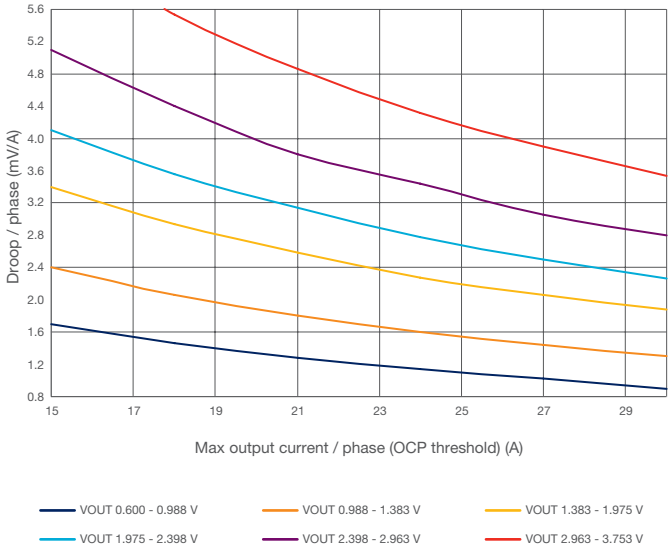

Figure 39. Recommended maximum individual droop per phase vs VOUT and max IOUT for BMR463.

TON_DELAY

For each Slave phase the TON_DELAY parameter shall be set equal and to 5 ms or higher. For the Master phase TON_DELAY shall be set at least 10 ms greater than the TON_DELAY value used for each Slave phase. The resulting delay times used for the common output will be the one set for the Master phase.

TOFF_DELAY

Same configurations rules as for TON_DELAY.

TON_RISE, TON_FALL

The TON_RISE and TON_FALL values must be equal for each phase in the group. For a current sharing group there is an upper limit to the ramp time that can be used. The limit will depend on the used switch frequency, input voltage and output voltage. Figure 40 shows the approximate maximum ramp time when considering the whole input voltage range 4.5-14 V. It is recommended to use ramp times in the range 5 to 10 ms.

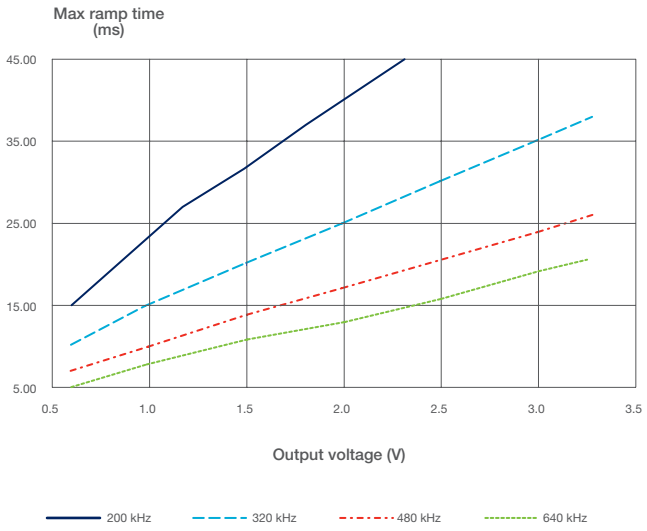

Figure 40. Max ramp time vs output voltage and switch frequency

FREQUENCY_SWITCH

If the current sharing group uses an external clock, the FREQUENCY_SWITCH value shall be set to the frequency value of the external clock. The FREQUENCY_SWITCH value shall be equal for each product in a current sharing group.

ON_OFF_CONFIG

The configuration of ON_OFF_CONFIG must be equal for each product in a current sharing group. Ramping down the output at turn-off is mandatory which means bit 0 in ON_OFF_CONFIG must be set to 0. Note that if enabling by the PMBus is used, Broadcast Enable must be activated in MISC_CONFIG and GCB_CONFIG

Examples:

ON_OFF_CONFIG = 0x16	Enable by CTRL pin, active high polarity
ON_OFF_CONFIG = 0x14	Enable by CTRL pin, active low polarity
ON_OFF_CONFIG = 0x1A	Enable by PMBus command OPERATION

OVUV_CONFIG

For products in a current sharing group the crowbar function must be turned off, i.e. bit 7 in OVUV_CONFIG must be cleared.

Example:
OVUV_CONFIG = 0x0F

POWER_GOOD_DELAY

In order for the switching of compensator coefficients (see Ramp Behavior) to not occur before ramp-up has finished, the POWER_GOOD_DELAY value should fulfill the equation below.

$$POWER\_GOOD\_DELAY > 1.3 \times TON\_RISE \times \frac{(VOUT\_COMMAND - POWER\_GOOD\_ON)}{VOUT\_COMMAND}$$

The POWER_GOOD_DELAY value shall be equal for each product in the group.

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